

IRHNA7064 (JANSR2N7431U)

PD-91416G

Radiation Hardened Power MOSFET Surface Mount (SMD-2) 60V, N-channel, Rad Hard HEXFET™ Technology

Features

- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Surface mount
- Light weight
- ESD rating: Class 3B per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Summary

- BV_{DSS} : 60V
- I_D : 75A*
- $R_{DS(on),max}$: 15 mΩ
- $Q_{G,max}$: 270nC
- REF: MIL-PRF-19500/664



Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

Description

IR HiRel rad hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNA7064	SMD-2	COTS	100krad(Si)
IRHNA7064SCS	SMD-2	S-Level	100krad(Si)
JANSR2N7431U	SMD-2	JANS	100krad(Si)
IRHNA3064	SMD-2	COTS	300krad(Si)
JANSF2N7431U	SMD-2	JANS	300krad(Si)
IRHNA5064	SMD-2	COTS	500krad(Si)
JANSF2N7431U	SMD-2	JANS	500krad(Si)

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Radiation Hardened Power MOSFET (SMD-2)

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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^{\circ}C$	Continuous Drain Current	75*	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^{\circ}C$	Continuous Drain Current	56	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	300	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.4	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	500	mJ
I_{AR}	Avalanche Current ¹	75*	A
E_{AR}	Repetitive Avalanche Energy ¹	30	mJ
dv/dt	Peak Diode Reverse Recovery ³	2.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Package Mounting Surface Temperature	300 (for 5sec)	
	Weight	3.3 (Typical)	g

*Current is limited by package

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, $L = 0.17mH$, Peak $I_L = 75A$, $V_{GS} = 12V$ ³ $I_{SD} \leq 75A$, $di/dt \leq 220A/\mu s$, $V_{DD} \leq 60V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.015	Ω	$V_{GS} = 12V, I_{D2} = 56A^1$
		—	—	0.018		$V_{GS} = 12V, I_{D1} = 75A^1$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1mA$
G_{fs}	Forward Transconductance	18	—	—	S	$V_{DS} = 15V, I_{D2} = 35A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 48V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	270	nC	$I_{D1} = 75A$
Q_{GS}	Gate-to-Source Charge	—	—	60		$V_{DS} = 30V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	110		$V_{GS} = 12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	27	ns	$I_{D1} = 75A^{**}$
t_r	Rise Time	—	—	120		$V_{DD} = 30V$
$t_{d(off)}$	Turn-Off Delay Time	—	—	120		$R_G = 2.35\Omega$
t_f	Fall Time	—	—	100		$V_{GS} = 12V$
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	4900	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	2800	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	860	—		$f = 1.0MHz$

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	75	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	300	A	
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 75A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	360	ns	T _J = 25°C, I _F = 75A, V _{DD} ≤ 50V di/dt = 100A/μs ²
Q _{rr}	Reverse Recovery Charge	—	2.1	—	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta J-PCB}$	Junction-to-PC board (Soldered to a 1" sq. copper-clad board)	—	1.6	—	

2.4 Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	100krad (Si) ⁵		300k- 500k rad (Si) ⁶		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	60	—	V	$V_{GS} = 0\text{V}$, $I_D = 1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.25	4.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100	—	-100		$V_{GS} = -20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	25	—	50	μA	$V_{DS} = 48\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	0.015	—	0.025	Ω	$V_{GS} = 12\text{V}$, $I_{D2} = 56\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-2) ²	—	0.015	—	0.025	Ω	$V_{GS} = 12\text{V}$, $I_{D2} = 56\text{A}$
V_{SD}	Diode Forward Voltage	—	1.5	—	1.5	V	$V_{GS} = 0\text{V}$, $I_F = 75\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$
³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 48\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part number(s) : IRHNA7064 (JANSR2N7431U)

⁶ Part numbers(s) : IRHNA3064 (JANSF2N7431U) and IRHNA5064 (JANS62N7431U)

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Radiation Hardened Power MOSFET (SMD-2)

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)				
			V _{GS} = 0V	V _{GS} = -5V	V _{GS} = -10V	V _{GS} = -15V	V _{GS} = -20V
38 ± 5%	310 ± 5%	39 ± 5%	60	60	45	40	30
61 ± 5%	345 ± 5%	32 ± 5%	40	35	30	25	20

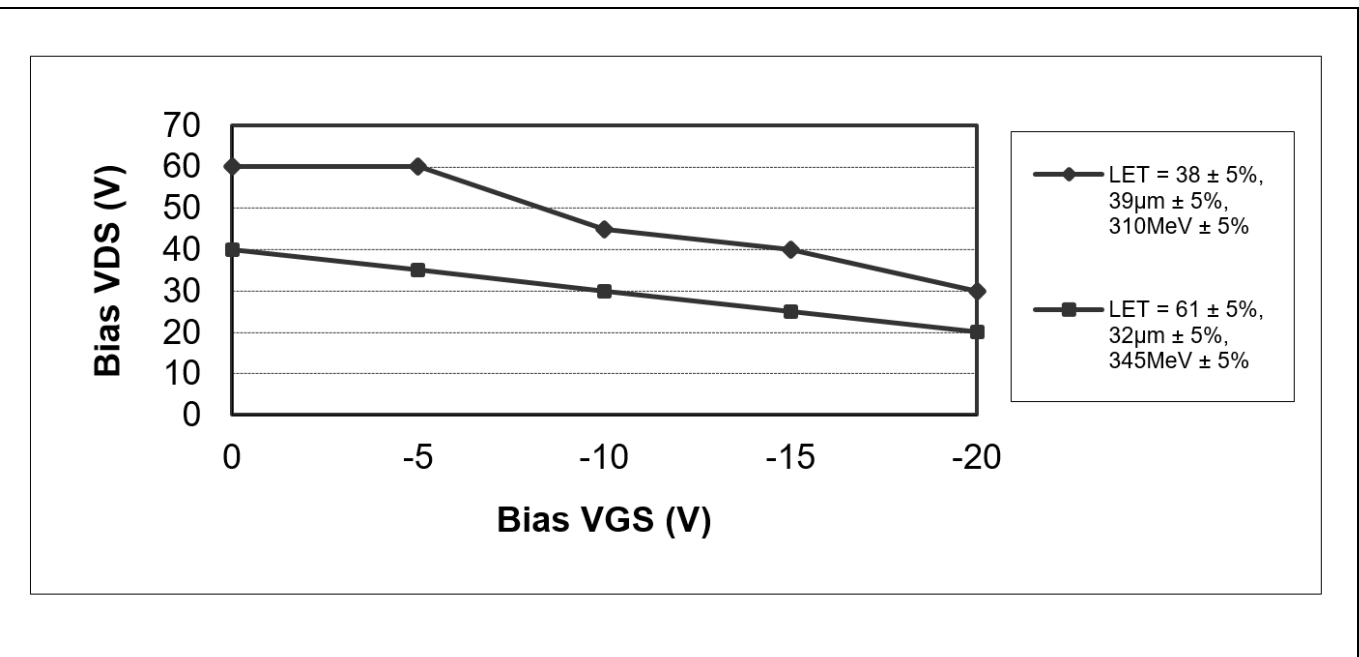


Figure 1 Typical Single Event Effect, Safe Operating Area

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Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

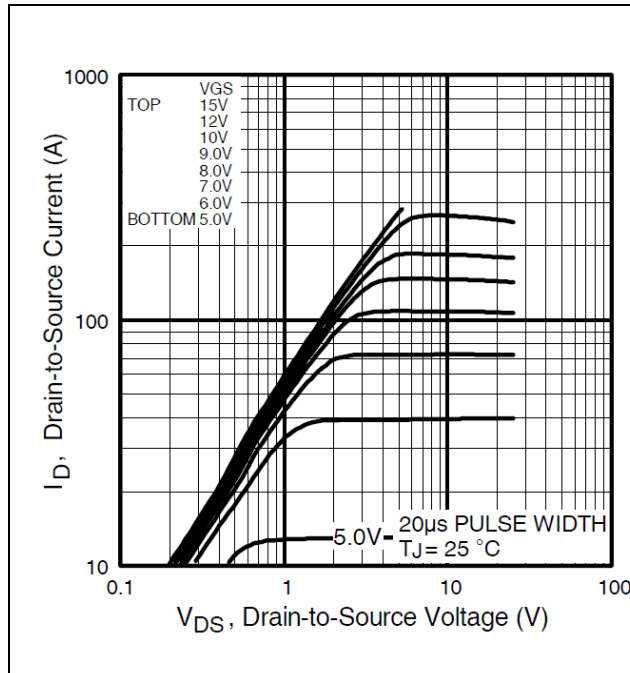


Figure 2 Typical Output Characteristics

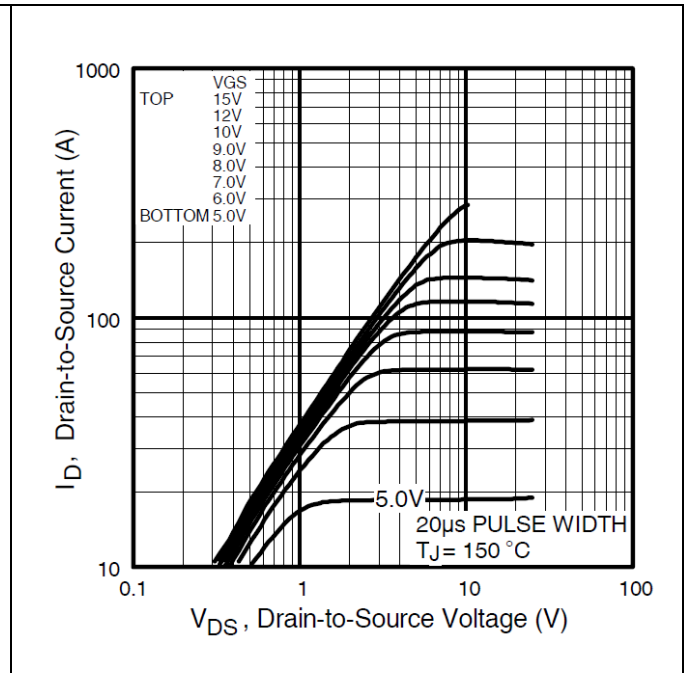


Figure 3 Typical Output Characteristics

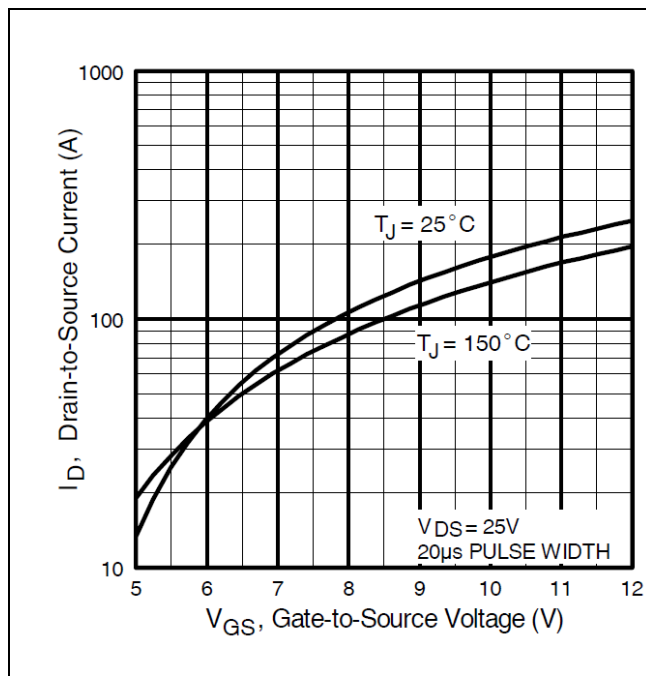


Figure 4 Typical Transfer Characteristics

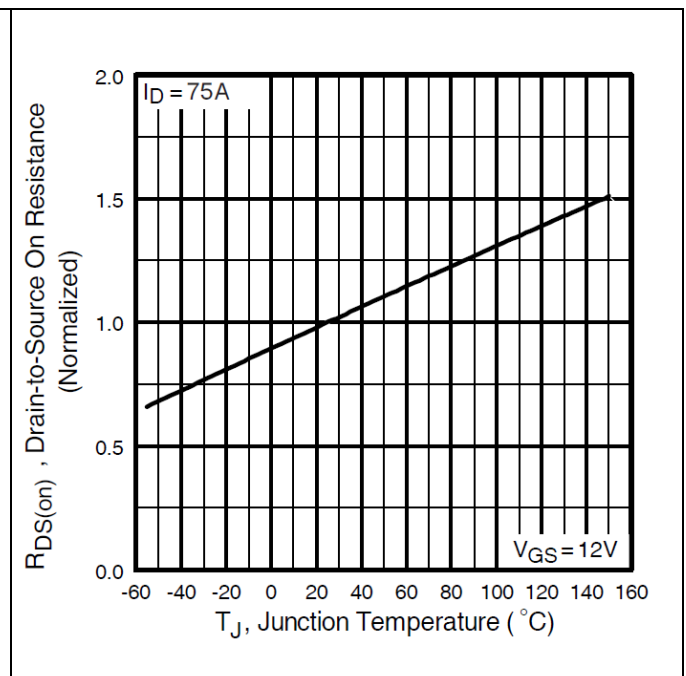


Figure 5 Normalized On-Resistance Vs. Temperature

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Radiation Hardened Power MOSFET (SMD-2)

Electrical Characteristics Curves (Pre-irradiation)

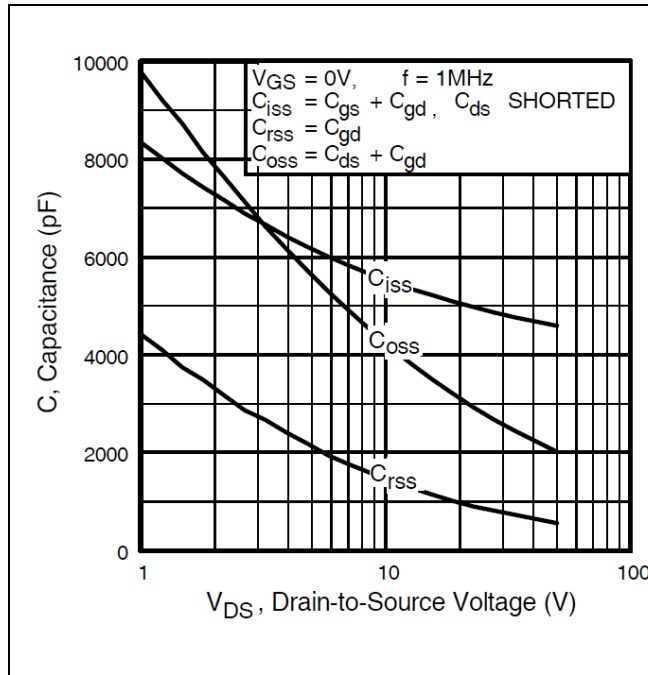


Figure 6 Typical Capacitance Vs. Drain-to-Source Voltage

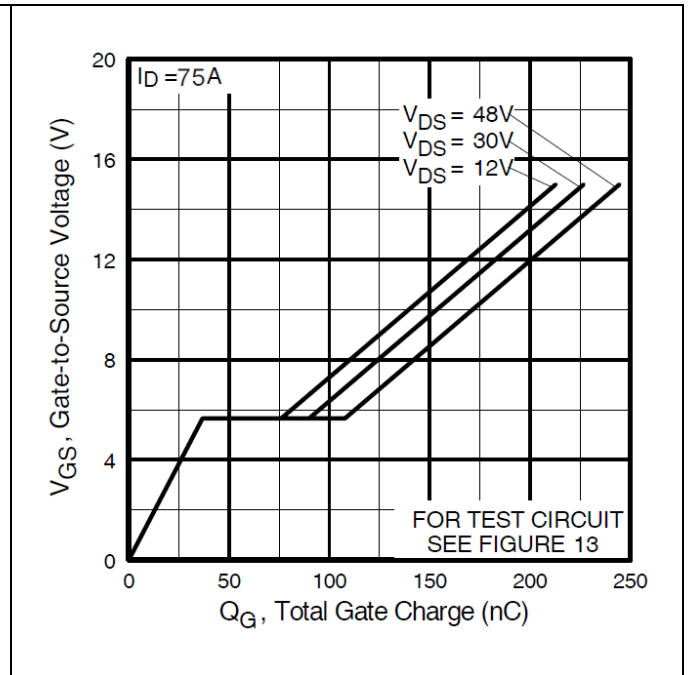


Figure 7 Gate-to-Source Voltage Vs. Typical Gate Charge

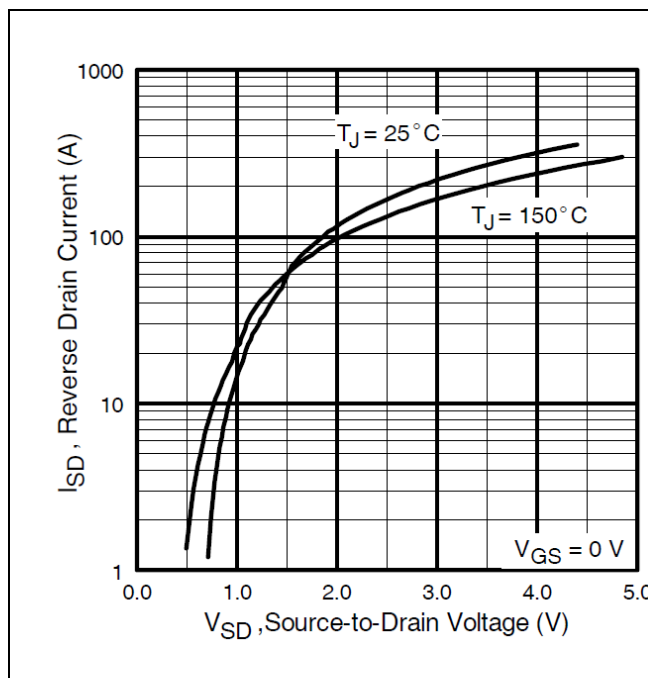


Figure 8 Typical Source-Drain Current Vs. Diode Forward Voltage

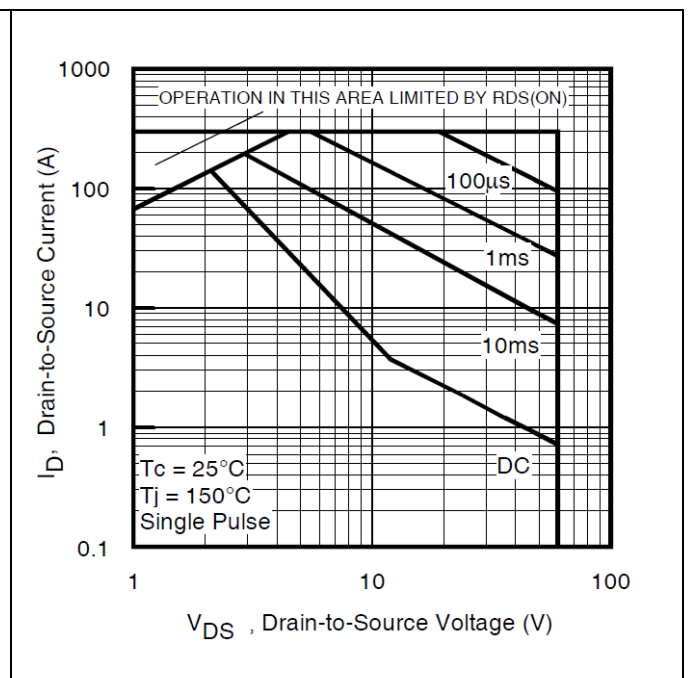


Figure 9 Maximum Safe Operating Area

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Electrical Characteristics Curves (Pre-irradiation)

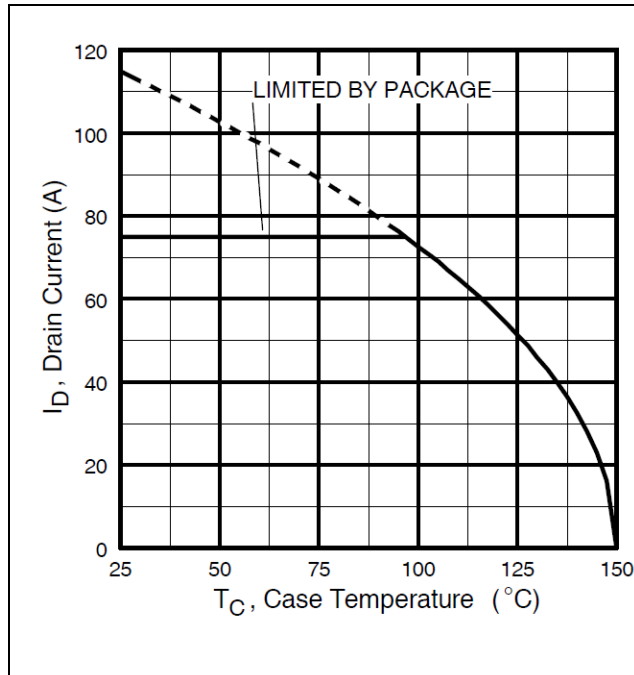


Figure 10 Maximum Drain Current Vs. Case Temperature

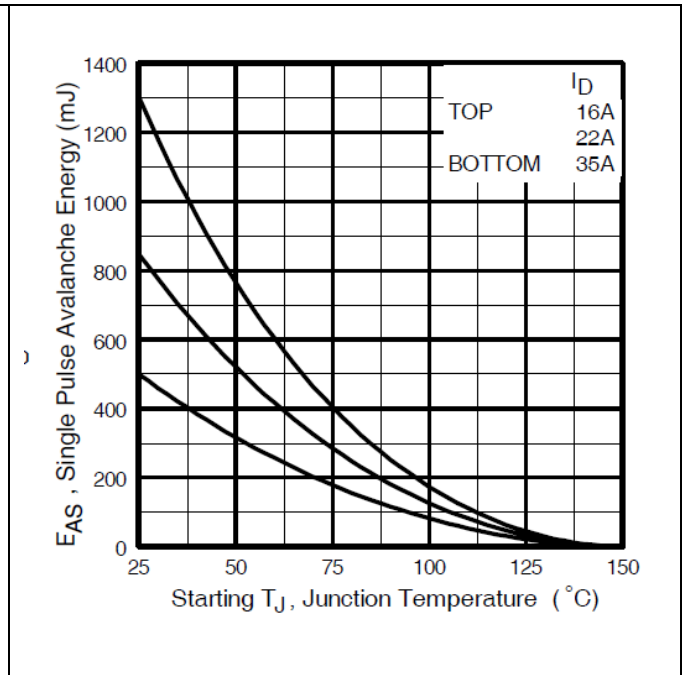


Figure 11 Maximum Avalanche Energy Vs. Junction Temperature

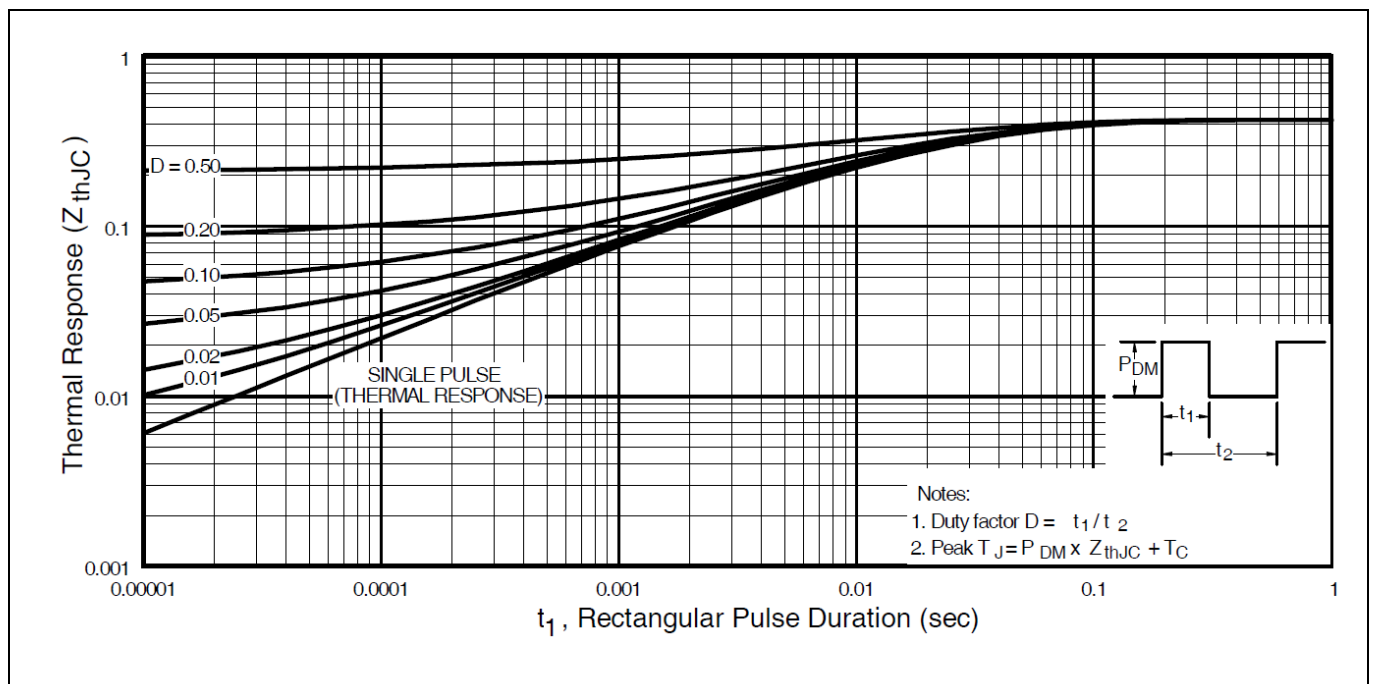


Figure 12 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Radiation Hardened Power MOSFET (SMD-2)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

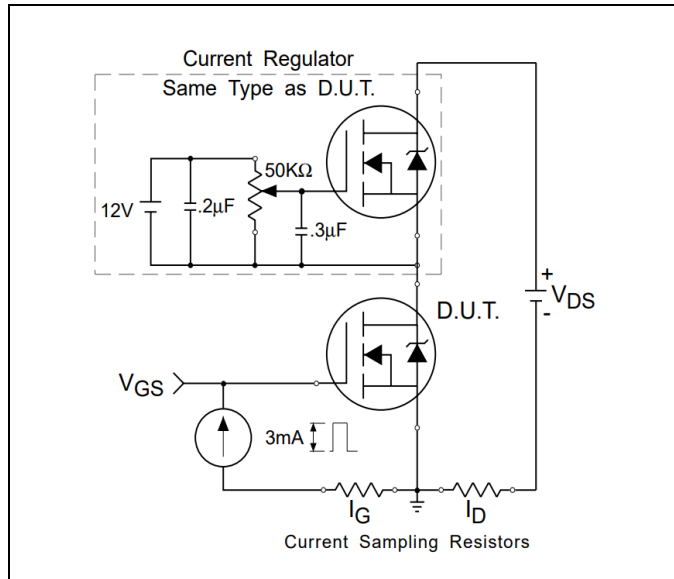


Figure 13 Gate Charge Test Circuit

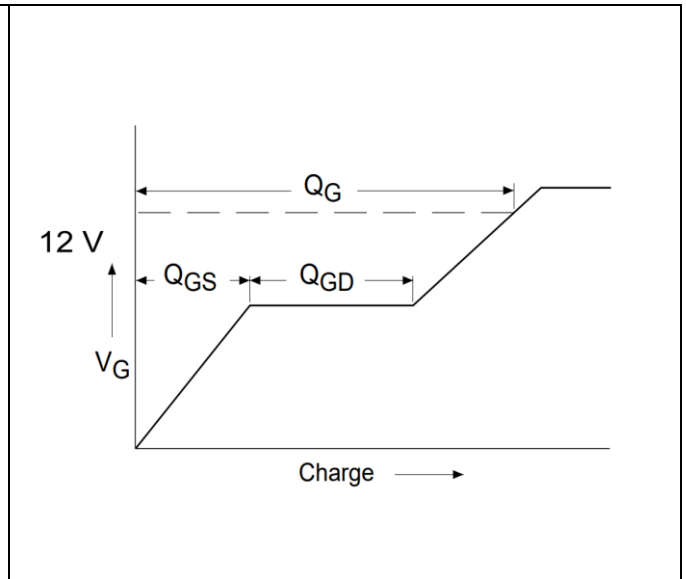


Figure 14 Gate Charge Waveform

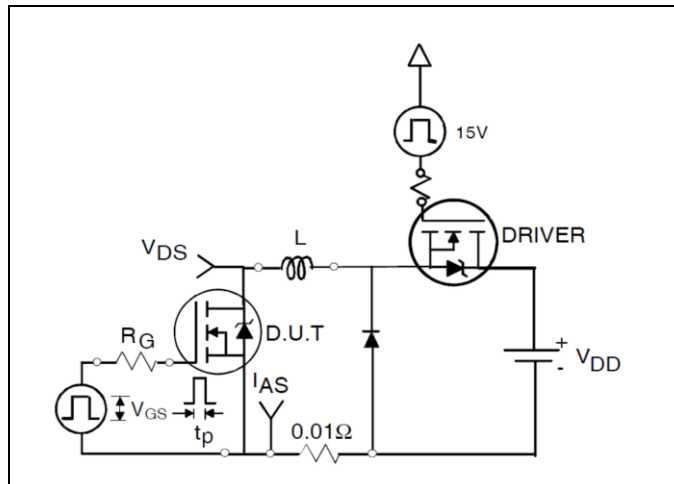


Figure 15 Unclamped Inductive Test Circuit

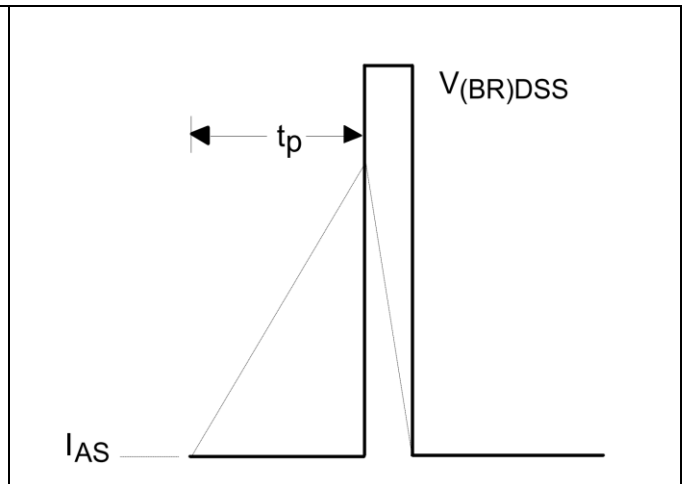


Figure 16 Unclamped Inductive Waveform

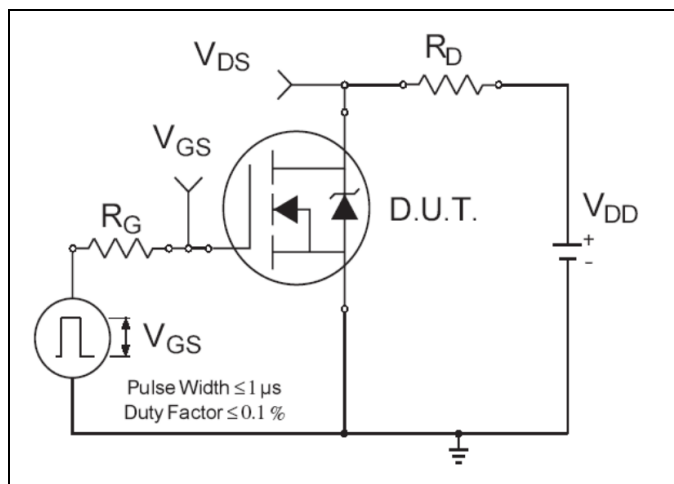


Figure 17 Switching Time Test Circuit

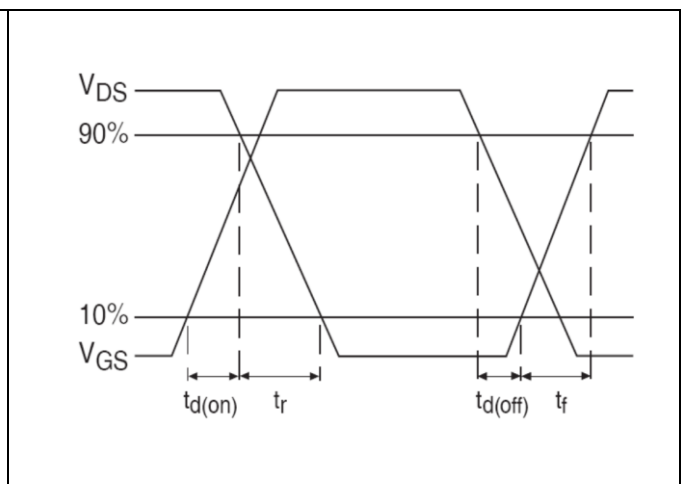


Figure 18 Switching Time Waveforms

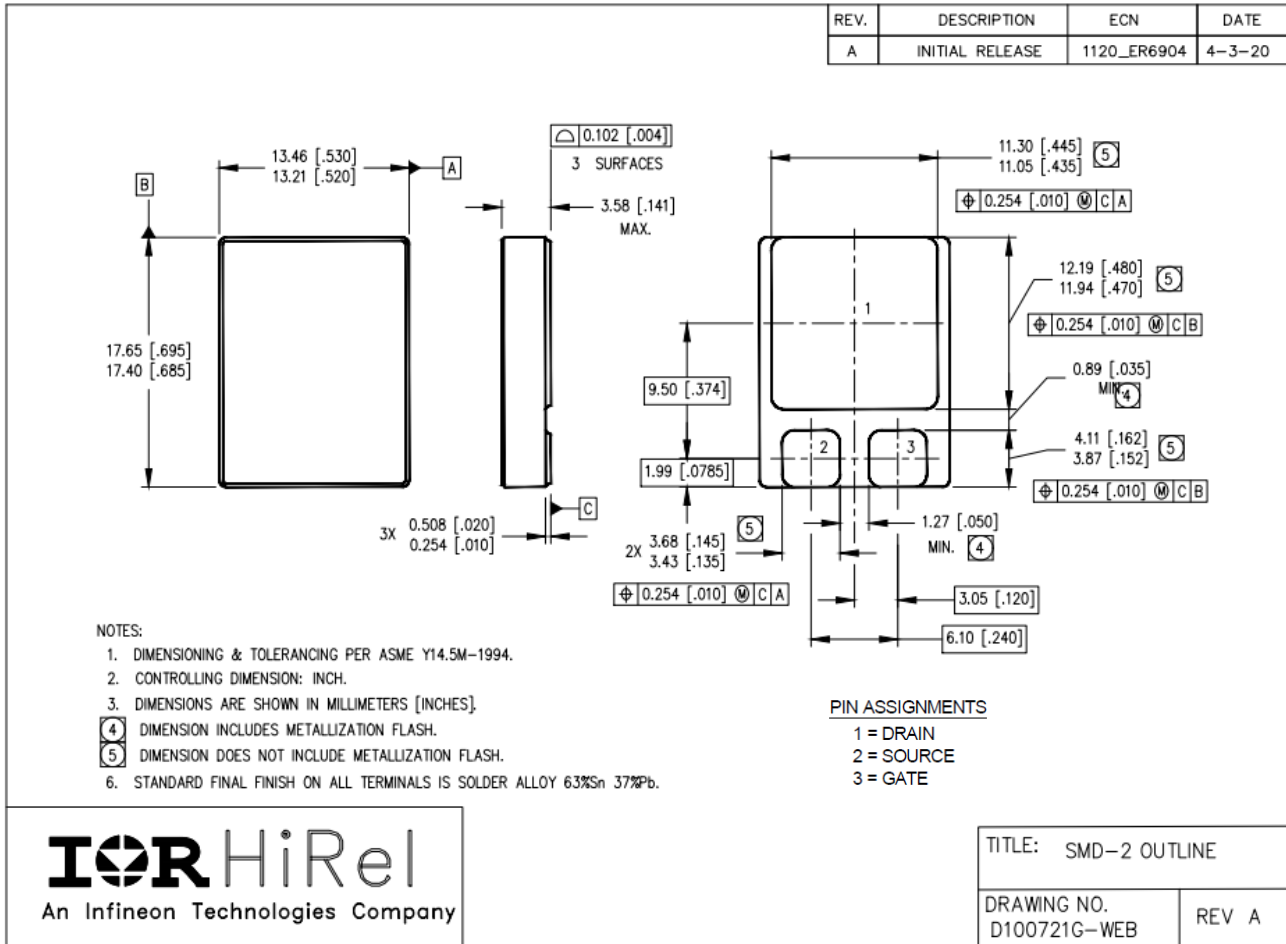
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Radiation Hardened Power MOSFET (SMD-2)

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SMD-2](#)



Revision history**Revision history**

Document version	Date of release	Description of changes
Rev A	08/25/1998	Datasheet (PD-91416A)
Rev B	12/04/2001	Updated Switching test condition VGS =12V-page2
Rev C	05/16/2006	Updated 600Krad(si) to 500Krad(si) page1
Rev D	02/14/2007	Updated based on ECN-14645
Rev E	03/28/2014	Updated based on ECN-1120_02161
Rev F	06/24/2021	Updated based on ECN-1120_08610
Rev G	11/12/2024	Updated based on ECN-1120_10126

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