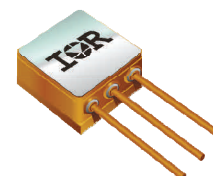


**RADIATION HARDENED
POWER MOSFET
THRU-HOLE (Low Ohmic Tabless - TO-254AA)**
60V, P-CHANNEL
REF: MIL-PRF-19500/733

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number
IRHMB597064	100 kRads(Si)	0.018Ω	-45A*	JANSR2N7524D4
IRHMB593064	300 kRads(Si)	0.018Ω	-45A*	JANSF2N7524D4


TO-254AA
Low Ohmic Tabless
Description

IRHMB597064 is a part of the International Rectifier HiRel family of products. IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Fast Switching
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Light Weight
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings
Pre-Irradiation

Symbol	Parameter	Value	Units
I _D @ V _{GS} = -12V, T _C = 25°C	Continuous Drain Current	-45*	A
I _D @ V _{GS} = -12V, T _C = 100°C	Continuous Drain Current	-45*	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	-180	
P _D @ T _C = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	890	mJ
I _{AR}	Avalanche Current ①	-45	A
E _{AR}	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-3.8	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in./1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	

*Current is limited by package

For Footnotes refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.064	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.018	Ω	V _{GS} = -12V, I _D = -45A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
G _{fs}	Forward Transconductance	39	—	—	S	V _{DS} = -15V, I _D = -45A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-10	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-25		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _G	Total Gate Charge	—	—	160	nC	I _D = -45A
Q _{GS}	Gate-to-Source Charge	—	—	60		V _{DS} = -30V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	65		V _{GS} = -12V
t _{d(on)}	Turn-On Delay Time	—	—	35	ns	V _{DD} = -30V
t _r	Rise Time	—	—	150		I _D = -45A
t _{d(off)}	Turn-Off Delay Time	—	—	100		R _G = 2.35Ω
t _f	Fall Time	—	—	35		V _{GS} = -12V
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance	—	8040	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	2780	—		V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	310	—		f = 1.0MHz
R _G	Internal Gate Resistance	—	2.2	—		f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-45*	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-180		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _J = 25°C, I _S = -45A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	110	ns	T _J = 25°C, I _F = -45A, V _{DD} ≤ -25V
Q _{rr}	Reverse Recovery Charge	—	—	460	nC	di/dt = -100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	0.6	°C/W
R _{θCS}	Case-to-Sink	—	0.21	—	
R _{θJA}	Junction-to-Ambient (Typical Socket Mount)	—	—	48	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = -30V, starting T_J = 25°C, L = 0.88mH, Peak I_L = -45A, V_{GS} = -12V
- ③ I_{SD} ≤ -45A, di/dt ≤ -417A/μs, V_{DD} ≤ -60V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ **Total Dose Irradiation with V_{GS} Bias.** -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.** -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	100 kRads (Si) ¹		300 kRads (Si) ²		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	-60	—	V	V _{GS} = 0V, I _D = -1.0mA
V _{GS(th)}	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100	nA	V _{GS} = 20V
I _{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	V _{DS} = -48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.017	—	0.017	Ω	V _{GS} = -12V, I _D = -45A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-254AA)	—	0.018	—	0.018	Ω	V _{GS} = -12V, I _D = -45A
V _{SD}	Diode Forward Voltage ④	—	-5.0	—	-5.0	V	V _{GS} = 0V, I _D = -45A

1. Part number IRHMB597064, JANSR2N7524D4

2. Part number IRHMB593064, JANSF2N7524D4

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
			@ VGS = 0V	@ VGS =5V	@ VGS =10V	@ VGS =15V	@ VGS =20V
38 ± 5%	270 ± 7.5%	35 ± 7.5%	-60	-60	-60	-60	-60
61 ± 5%	330 ± 7.5%	31 ± 7.5%	-60	-60	-60	-45	-25
84 ± 5%	350 ± 7.5%	28 ± 7.5%	-60	-60	-60	—	—

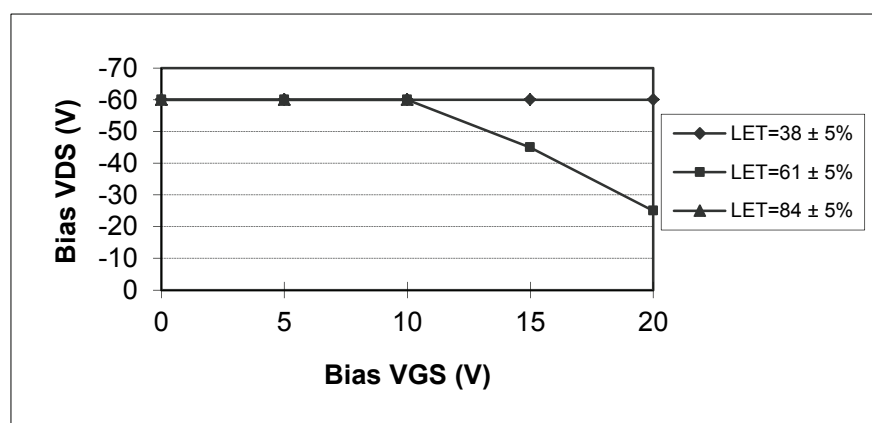


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

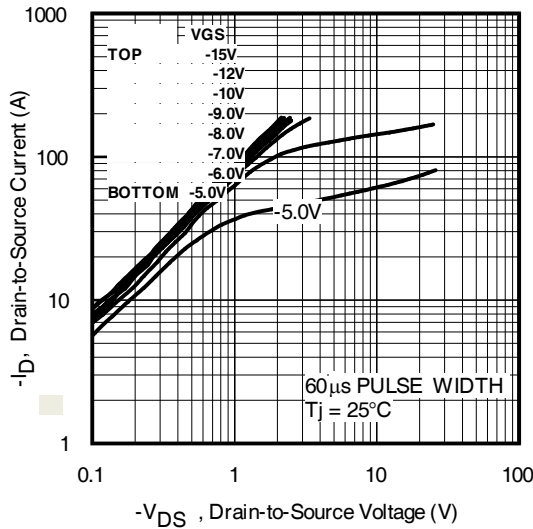


Fig 1. Typical Output Characteristics

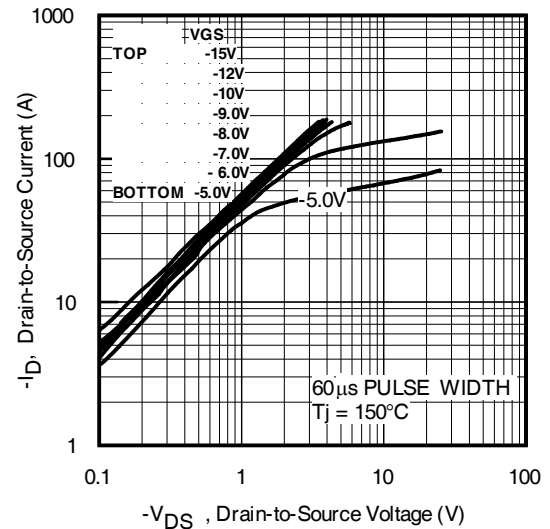


Fig 2. Typical Output Characteristics

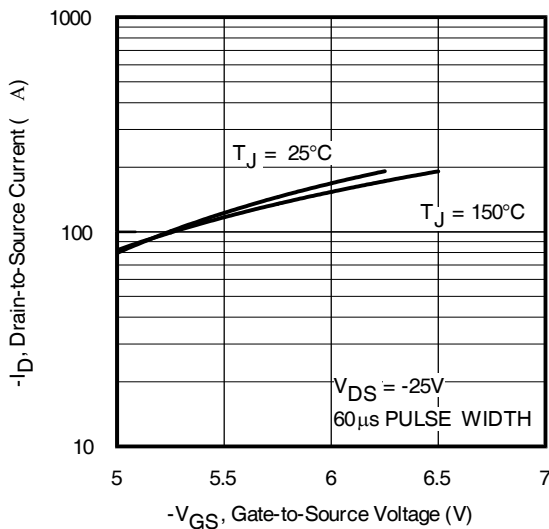


Fig 3. Typical Transfer Characteristics

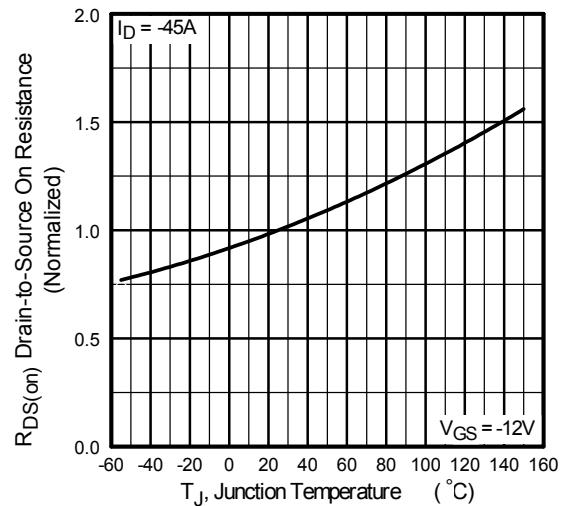


Fig 4. Normalized On-Resistance Vs. Temperature

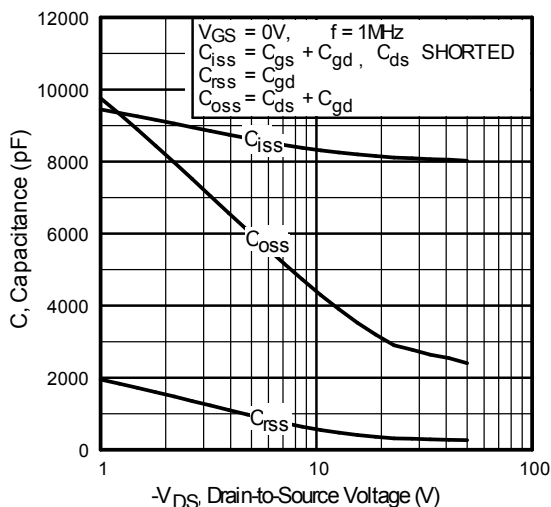


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

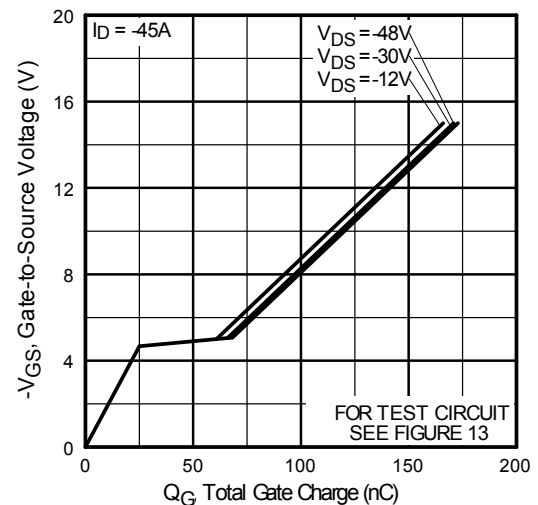


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

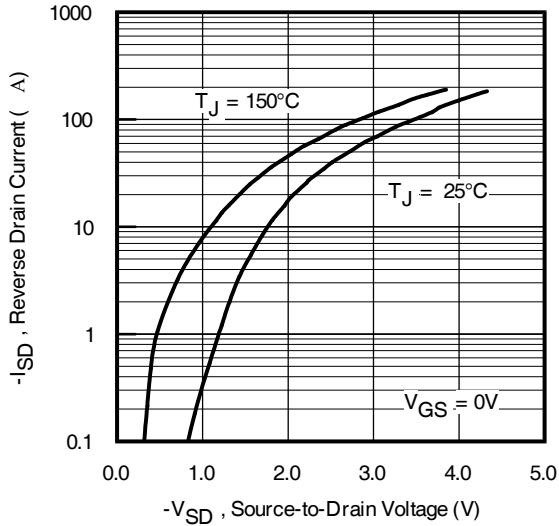


Fig 7. Typical Source-Drain Diode Forward Voltage

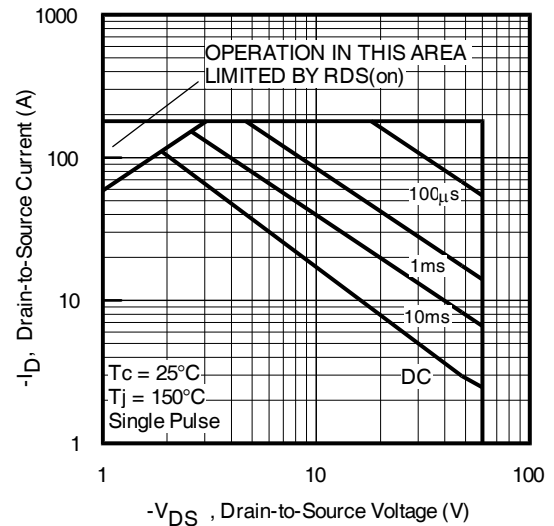


Fig 8. Maximum Safe Operating Area

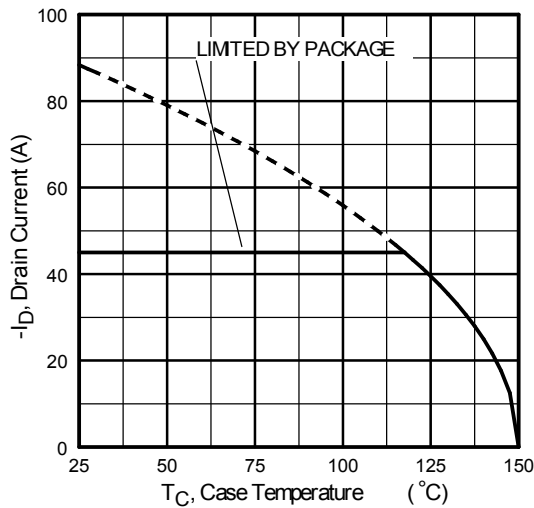


Fig 9. Maximum Drain Current Vs. Case Temperature

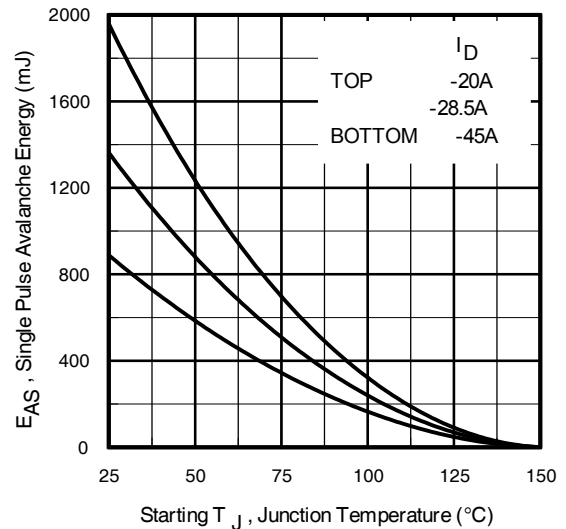


Fig 10. Maximum Avalanche Energy Vs. Drain Current

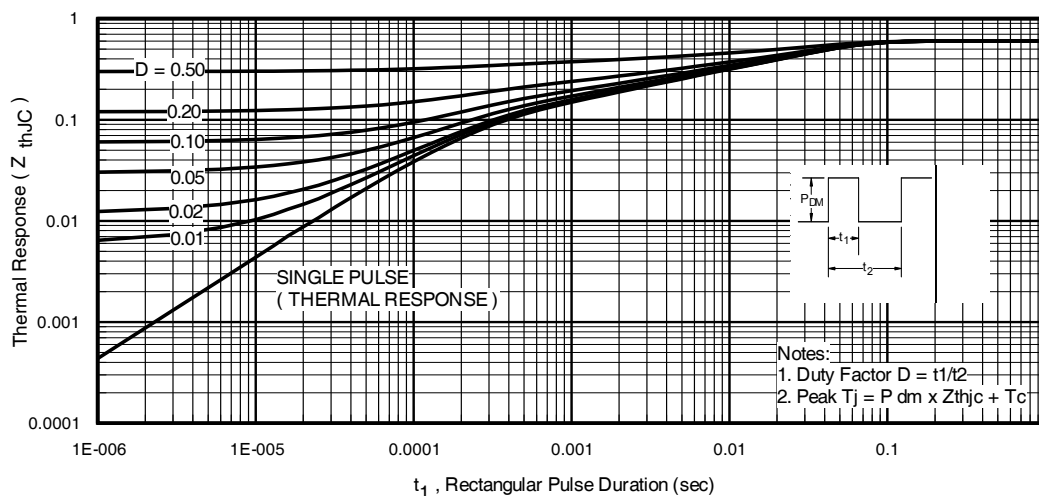


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

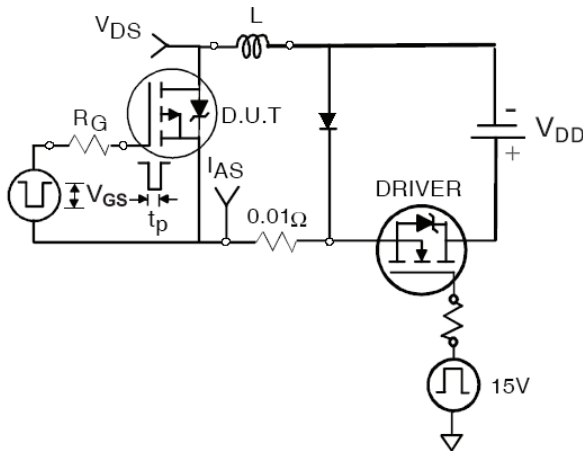


Fig 12a. Unclamped Inductive Test Circuit

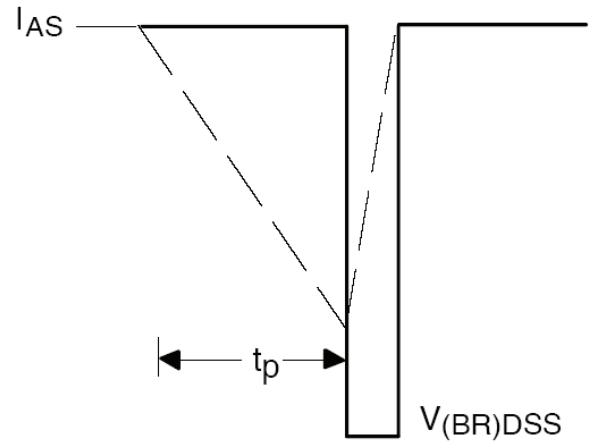


Fig 12b. Unclamped Inductive Waveforms

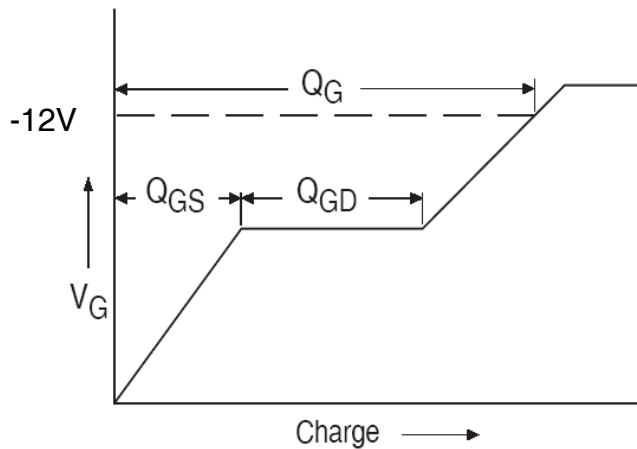


Fig 13a. Basic Gate Charge Waveform

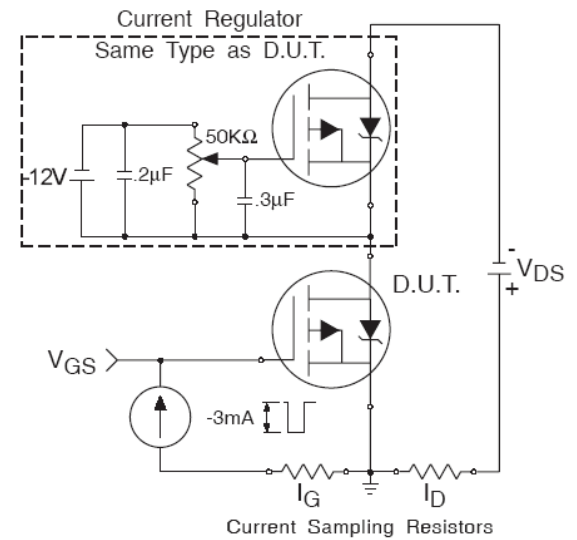


Fig 13b. Gate Charge Test Circuit

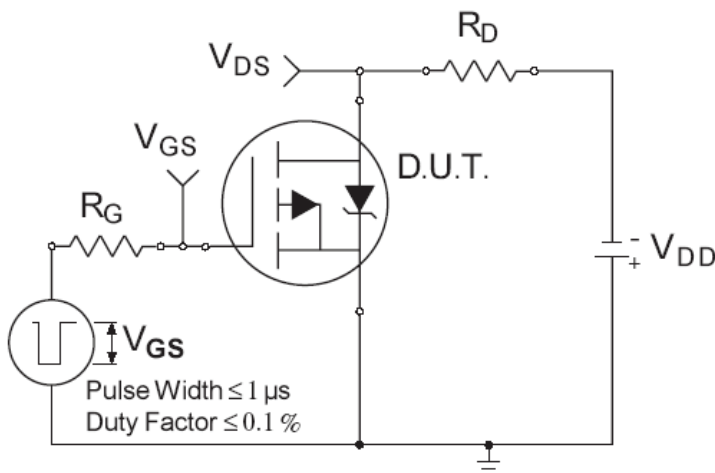


Fig 14a. Switching Time Test Circuit

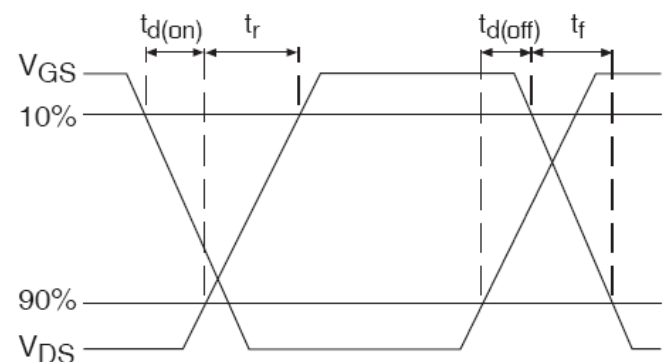
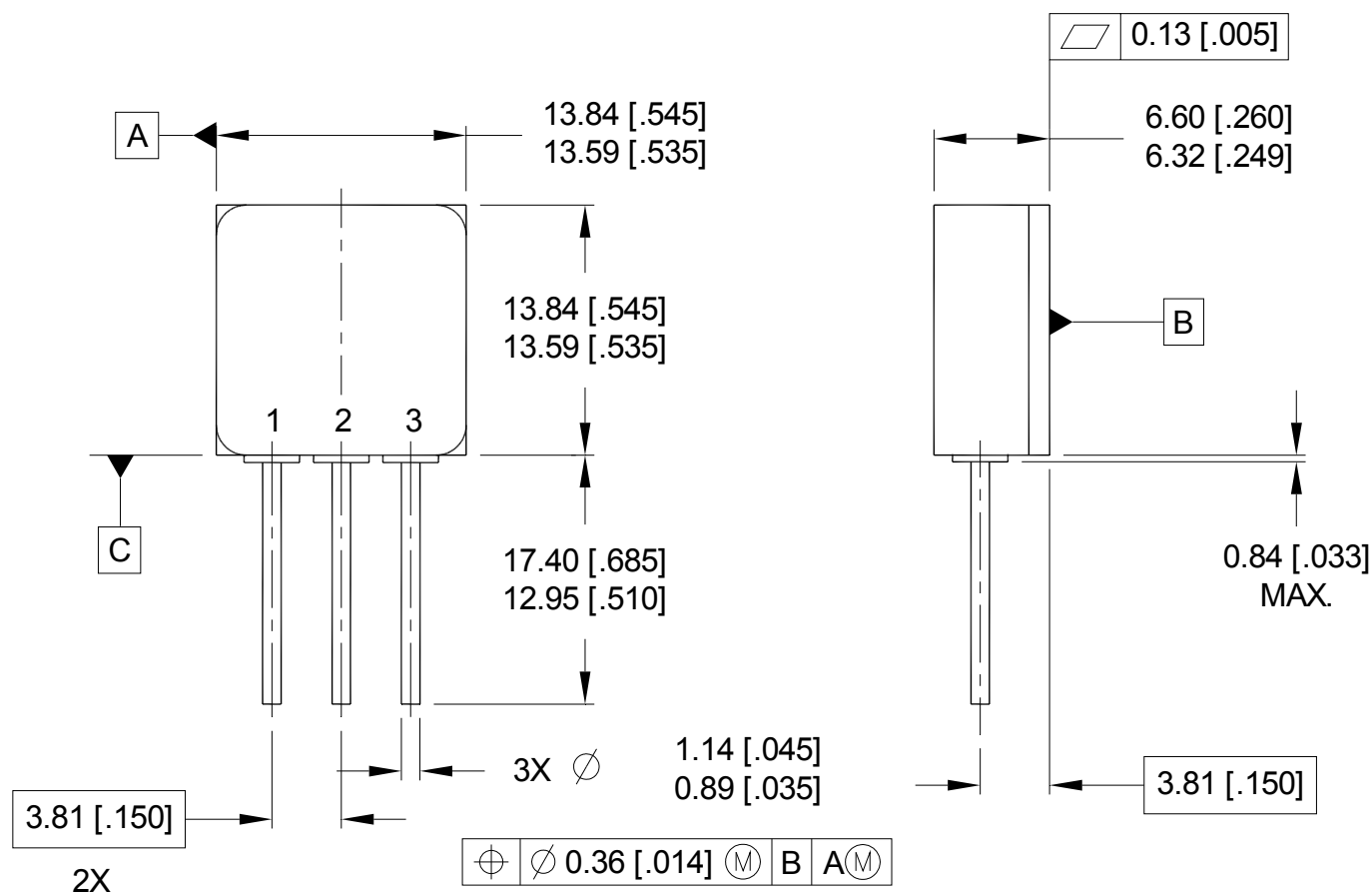


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — Low Ohmic Tabless - TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. THIS OUTLINE IS A MODIFIED TO-254AA JEDEC OUTLINE.
5. AVAILABLE WITH EITHER GLASS OR CERAMIC SEALS.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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