

IRHLUC7970Z4

PD-97574C

Radiation Hardened Logic Level Power MOSFETs Surface Mount (LCC-6) -60V, -0.65A, Dual P-channel, R7 Technology

Features

- 5V CMOS and TTL compatible
- Low $R_{DS(on)}$
- Single event effect (SEE) hardened
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Light weight
- Surface mount
- ESD rating: Class 0B per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHLUC7970Z4	LCC-6	COTS	100 krad(Si)
IRHLUC7970Z4SCS	LCC-6	S-Level	100 krad(Si)
IRHLUC7930Z4	LCC-6	COTS	300 krad(Si)

Product Summary

- BV_{DSS} : -60V
- I_D : -0.65A
- $R_{DS(on), max}$: 1.6Ω
- Q_G, max : 3.6nC



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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = -4.5V, T_C = 25^{\circ}C$	Continuous Drain Current	-0.65	A
$I_{D2} @ V_{GS} = -4.5V, T_C = 100^{\circ}C$	Continuous Drain Current	-0.41	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	-2.6	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	1.0	W
	Linear Derating Factor	0.01	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ²	34	mJ
I_{AR}	Avalanche Current ¹	-0.65	A
E_{AR}	Repetitive Avalanche Energy ¹	0.1	mJ
dv/dt	Peak Diode Reverse Recovery ³	-5.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Lead Temperature	300 (for 5s)	
	Weight	0.2 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = -25V$, starting $T_J = 25^{\circ}C$, $L = 161mH$, Peak $I_L = -0.65A$, $V_{GS} = -10V$ ³ $I_{SD} \leq -0.65A$, $di/dt \leq -150A/\mu s$, $V_{DD} \leq -60V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics (P-Ch Die) @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temp. Coefficient	—	-0.06	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.6	Ω	$V_{GS} = -4.5V, I_{D2} = -0.41A^1$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
$\Delta V_{GS(th)}/\Delta T_j$	Gate Threshold Voltage Coefficient	—	3.6	—	mV/ $^\circ\text{C}$	
G_{fs}	Forward Transconductance	0.6	—	—	S	$V_{DS} = -15V, I_{D2} = -0.41A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	$V_{DS} = -48V, V_{GS} = 0V$
		—	—	-20		$V_{DS} = -48V, V_{GS} = 0V, T_j = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -10V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 10V$
Q_G	Total Gate Charge	—	—	3.6	nC	$I_{D1} = -0.65A$
Q_{GS}	Gate-to-Source Charge	—	—	1.5		$V_{DS} = -30V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.8		$V_{GS} = -4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	—	23	ns	$I_{D1} = -0.65A^{**}$ $V_{DD} = -30V$ $R_G = 24\Omega$ $V_{GS} = -5.0V$
t_r	Rise Time	—	—	22		
$t_{d(off)}$	Turn-Off Delay Time	—	—	32		
t_f	Fall Time	—	—	26		
$L_s + L_D$	Total Inductance	—	33	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	147	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	46	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	8.1	—		$f = 1.0\text{MHz}$
R_G	Gate Resistance	—	52	—	Ω	$f = 1.0\text{MHz}$, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.65	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	-2.6	A	
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _J = 25°C, I _S = -0.65A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	35	ns	T _J = 25°C, I _F = -0.65A, V _{DD} ≤ -25V di/dt = -100A/μs ²
Q _{rr}	Reverse Recovery Charge	—	—	9.8	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JA}$	Junction-to-Ambient	—	—	125	$^\circ\text{C}/\text{W}$
$R_{\theta JL}$	Junction-to-Lead	—	—	40	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 300 krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	$V_{GS} = 0\text{V}$, $I_D = -250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	$V_{GS} = -10\text{V}$
	Gate-to-Source Leakage Reverse	—	100		$V_{GS} = 10\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	$V_{DS} = -48\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-39) ²	—	1.4	Ω	$V_{GS} = -4.5\text{V}$, $I_{D2} = -0.41\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (LCC-6) ²	—	1.6	Ω	$V_{GS} = -4.5\text{V}$, $I_{D2} = -0.41\text{A}$
V_{SD}	Diode Forward Voltage	—	-5.0	V	$V_{GS} = 0\text{V}$, $I_F = -0.65\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = -10\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = -48\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers: IRHLUC7970Z4 and IRHLUC7930Z4

IRHLUC7970Z4

Radiation Hardened Logic Level Power MOSFET Surface-Mount (LCC-6)

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)					
			V _{GS} = 0V	V _{GS} = 2V	V _{GS} = 4V	V _{GS} = 5V	V _{GS} = 6V	V _{GS} = 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	—
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	—	—

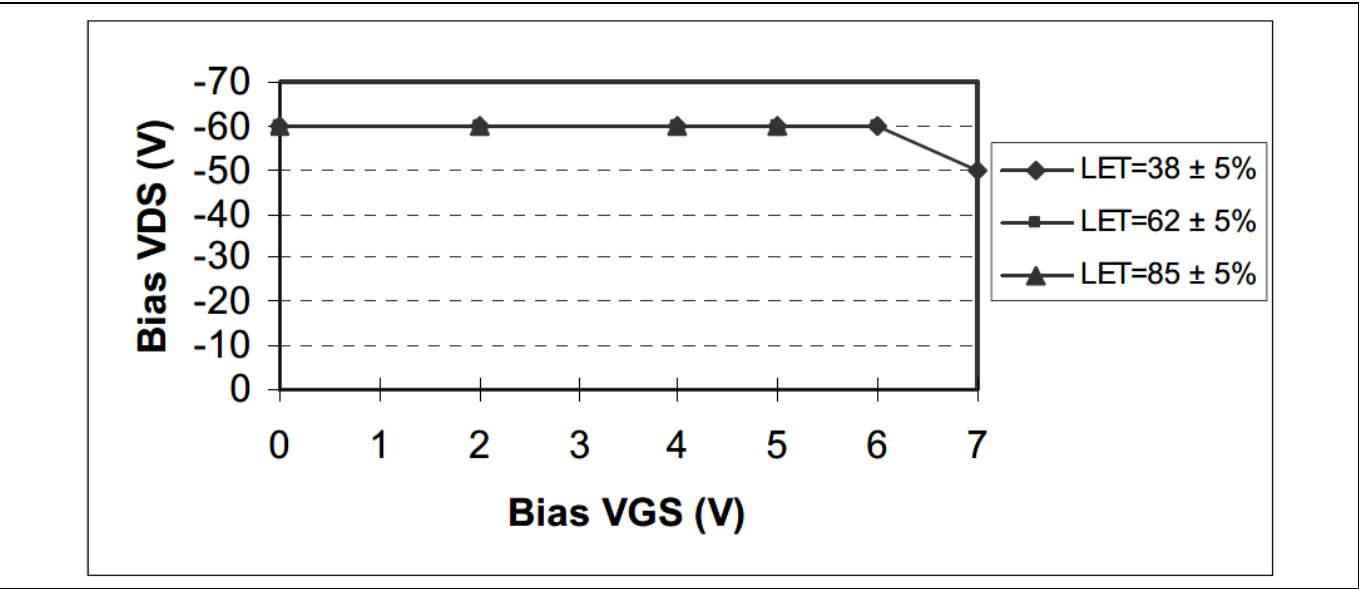


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

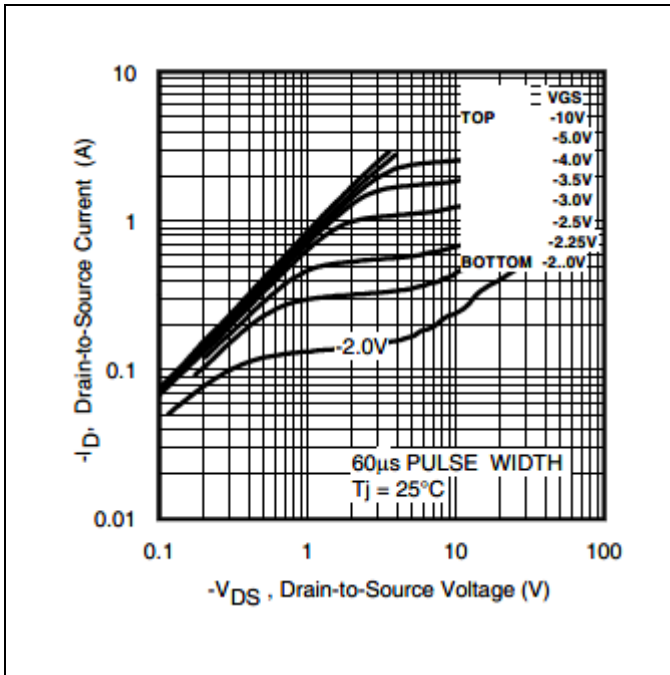


Figure 2 Typical Output Characteristics

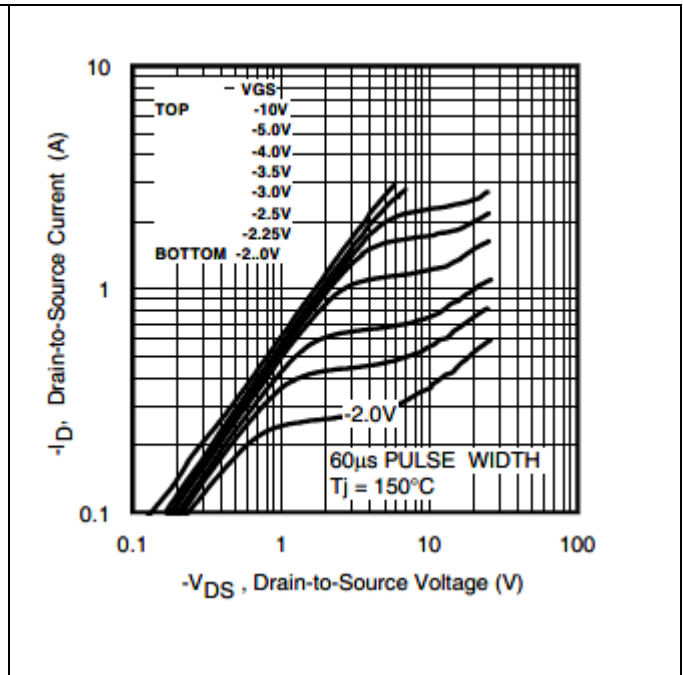


Figure 3 Typical Output Characteristics

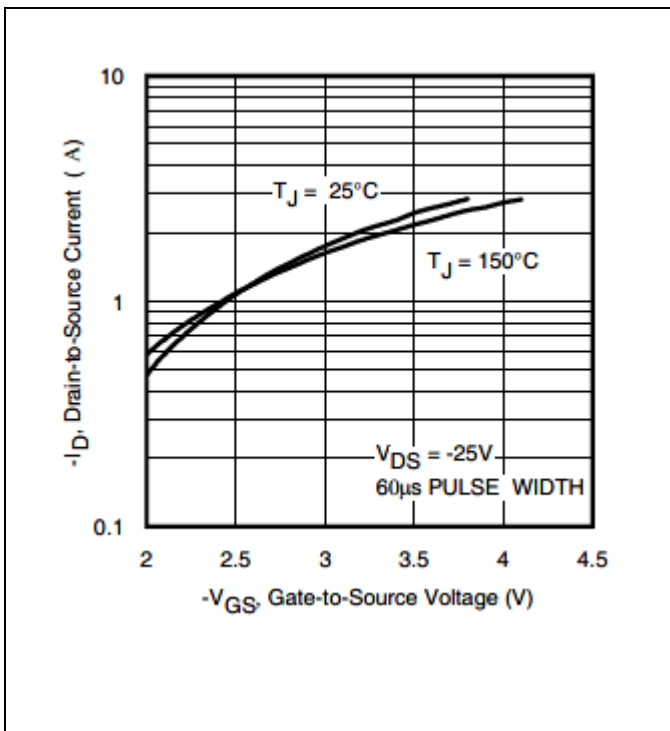


Figure 4 Typical Transfer Characteristics

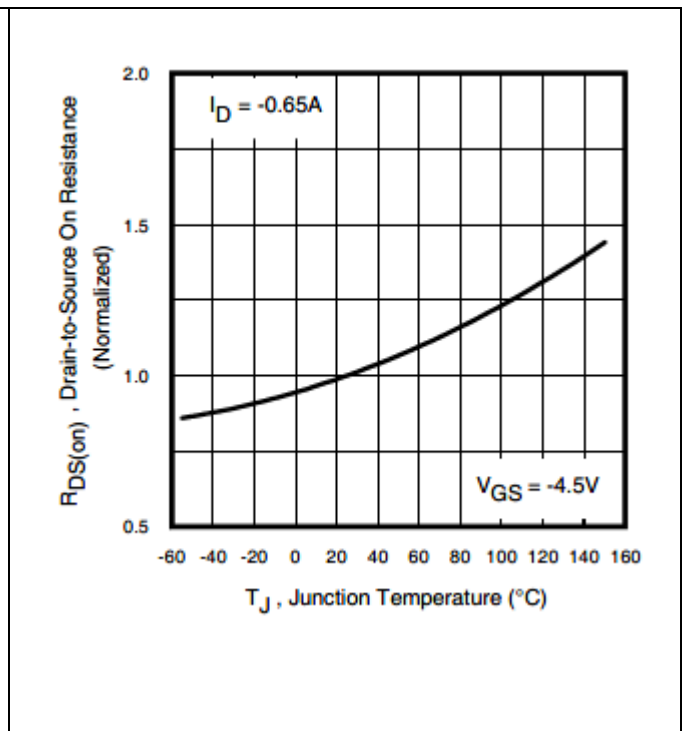


Figure 5 Normalized On-Resistance Vs. Temperature

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (LCC-6)

Electrical Characteristics Curves (Pre-irradiation)

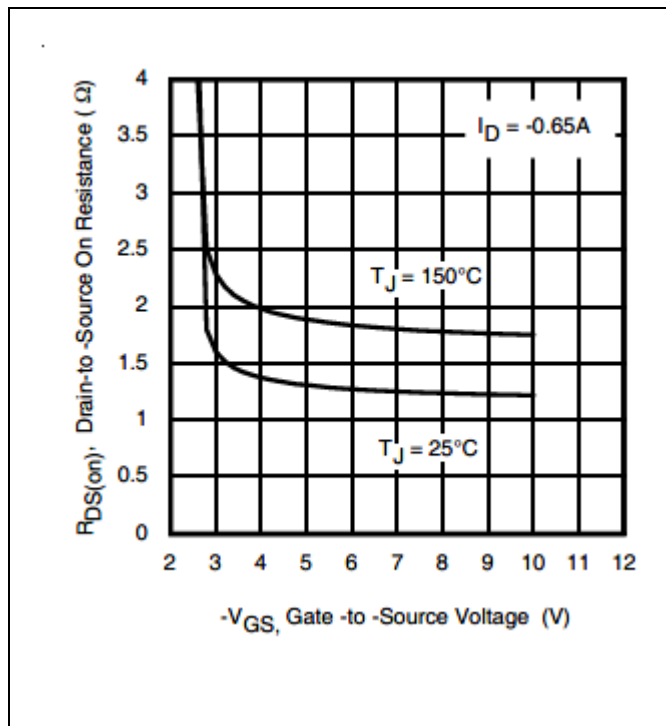


Figure 6 Typical On-Resistance Vs. Gate Voltage

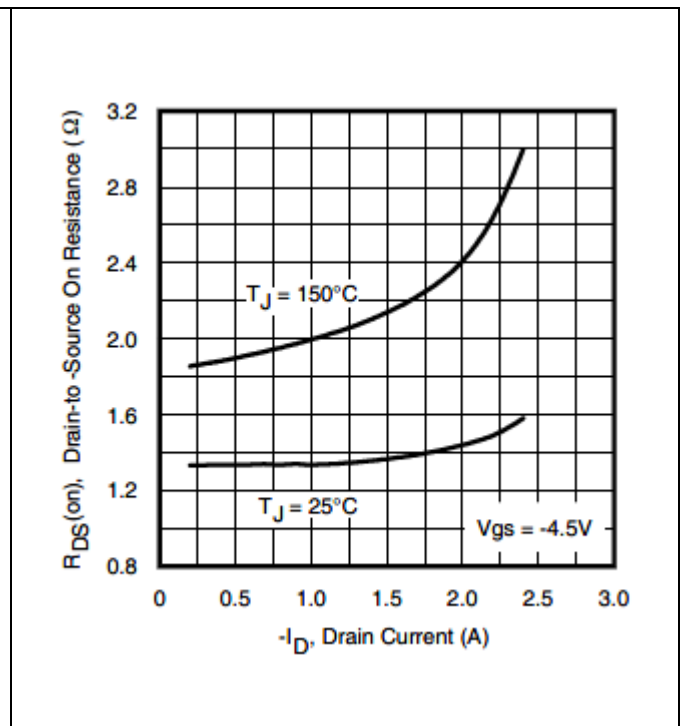


Figure 7 Typical On-Resistance Vs. Drain Current

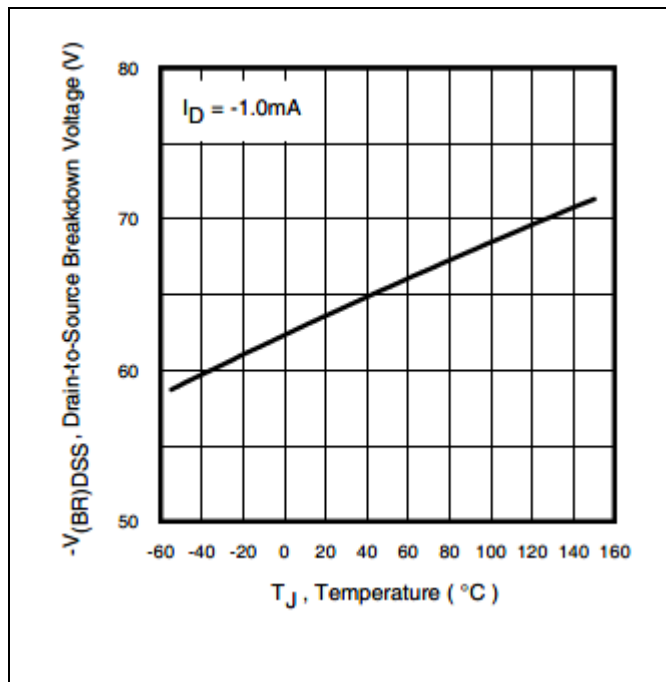


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

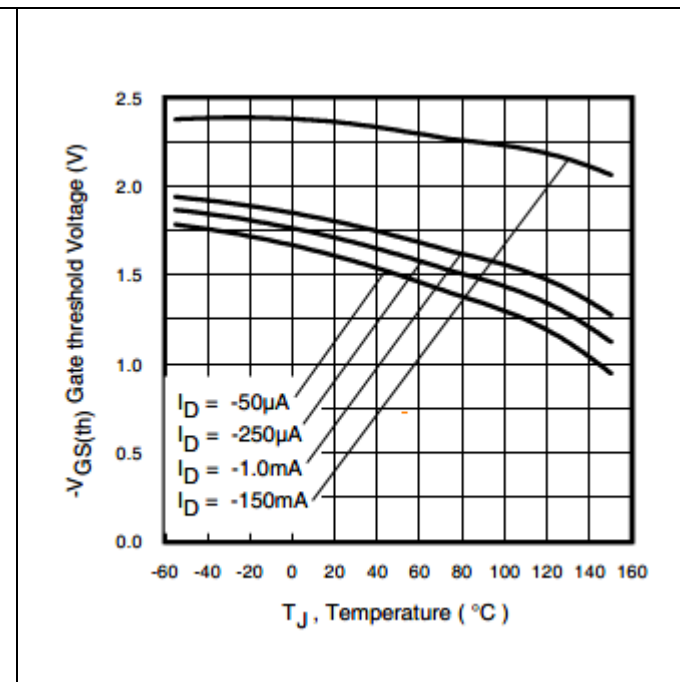


Figure 9 Typical Threshold Voltage Vs. Temperature

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (LCC-6)

Electrical Characteristics Curves (Pre-irradiation)

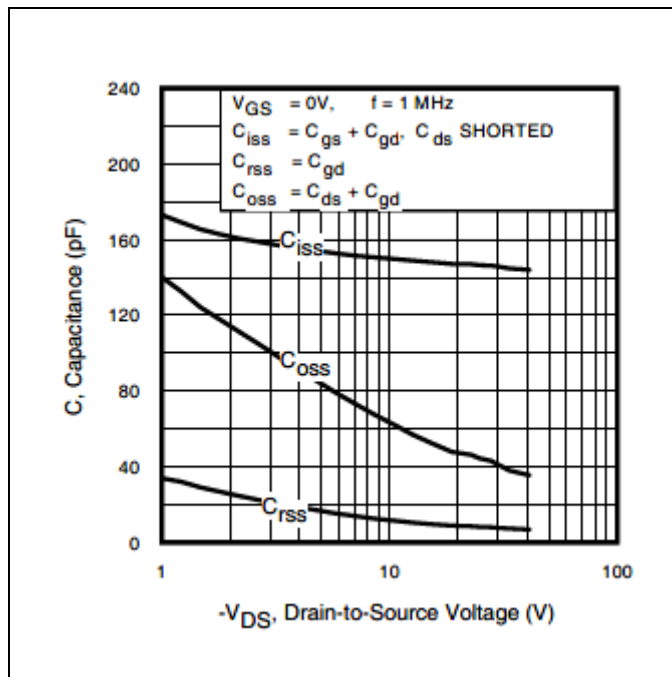


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

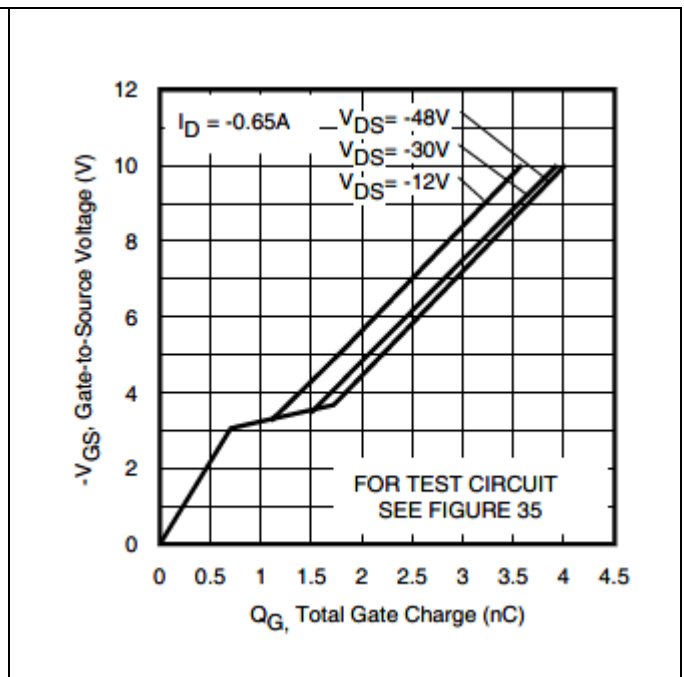


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

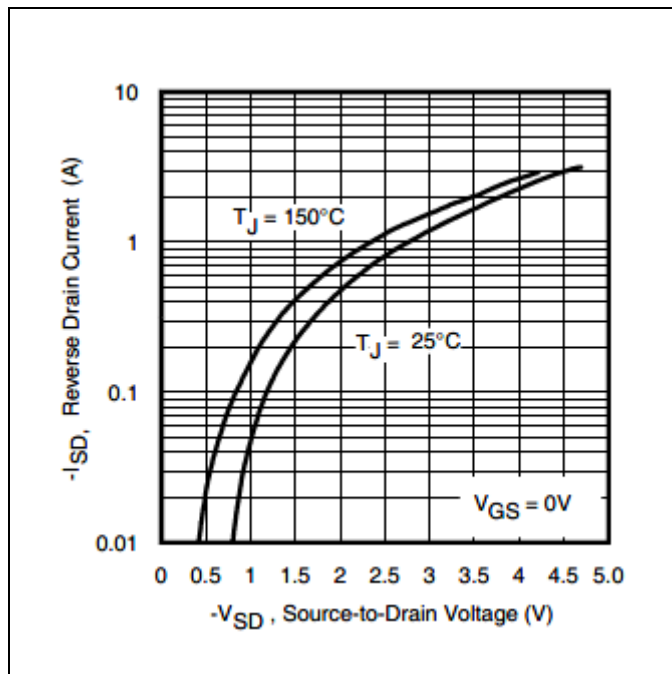


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

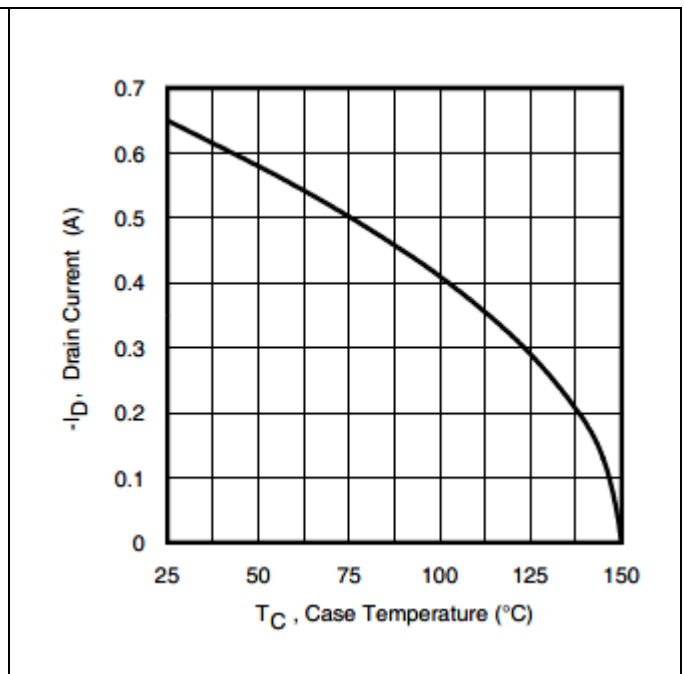


Figure 13 Maximum Drain Current Vs. Case Temperature

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (LCC-6)

Electrical Characteristics Curves (Pre-irradiation)

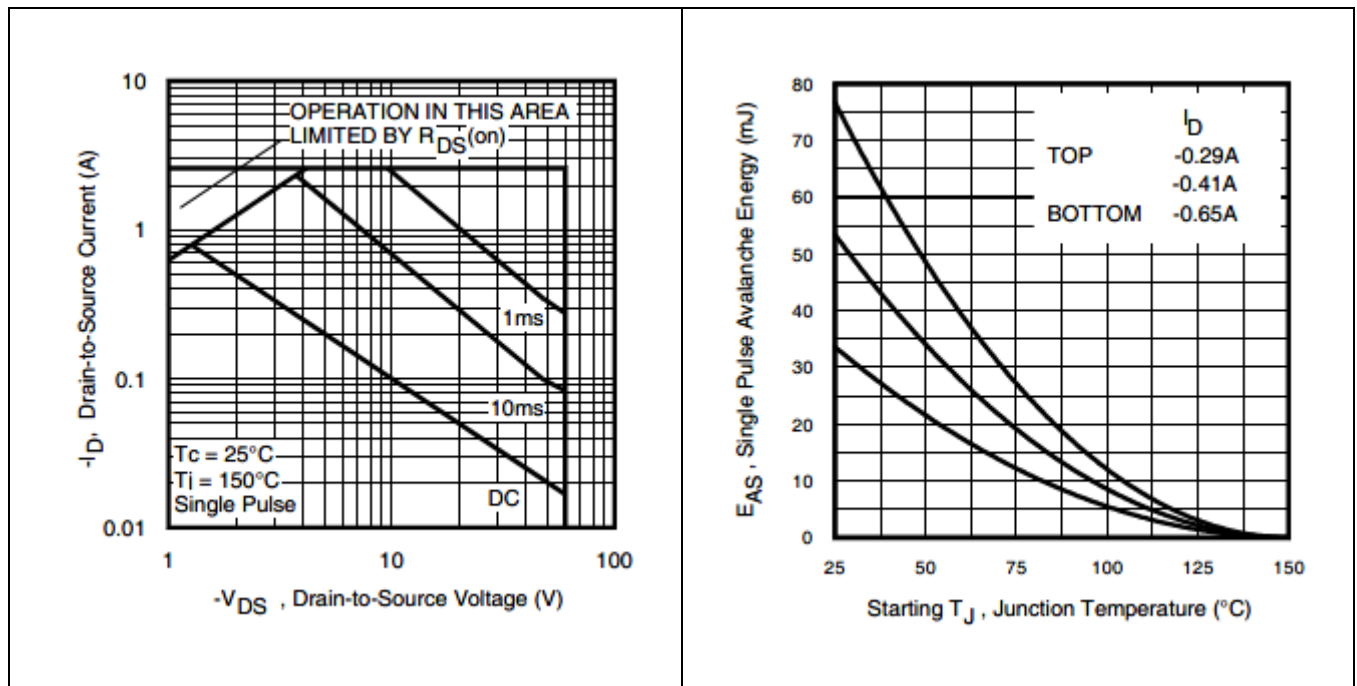


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

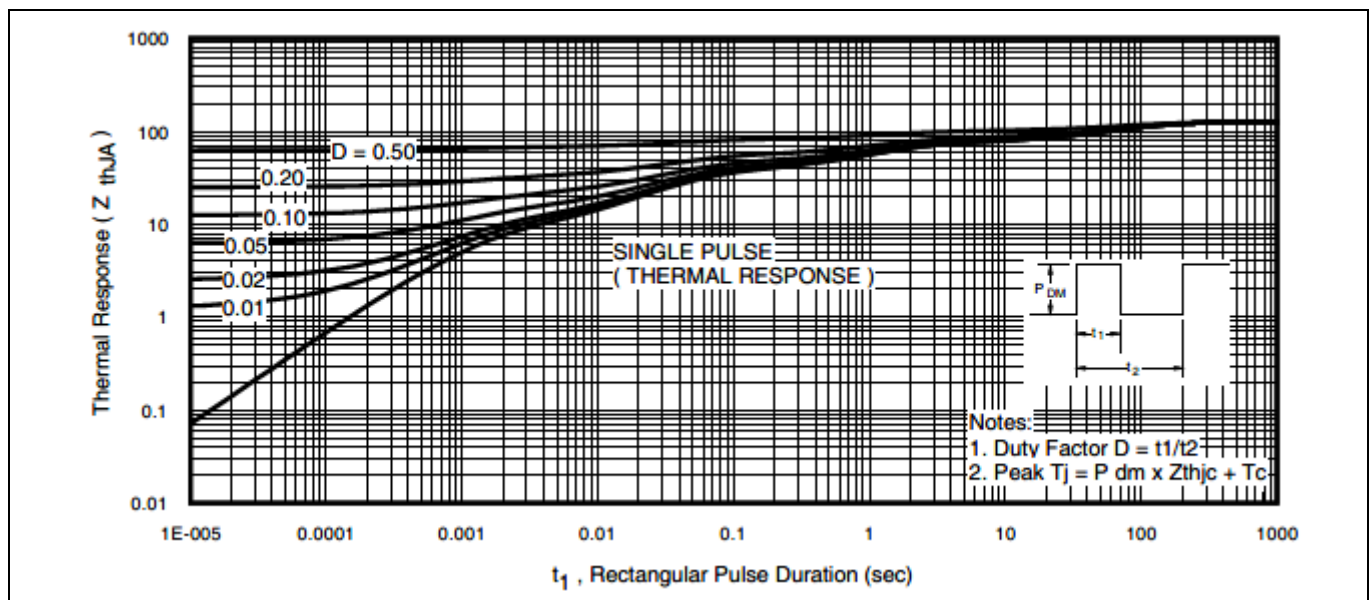


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (LCC-6)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

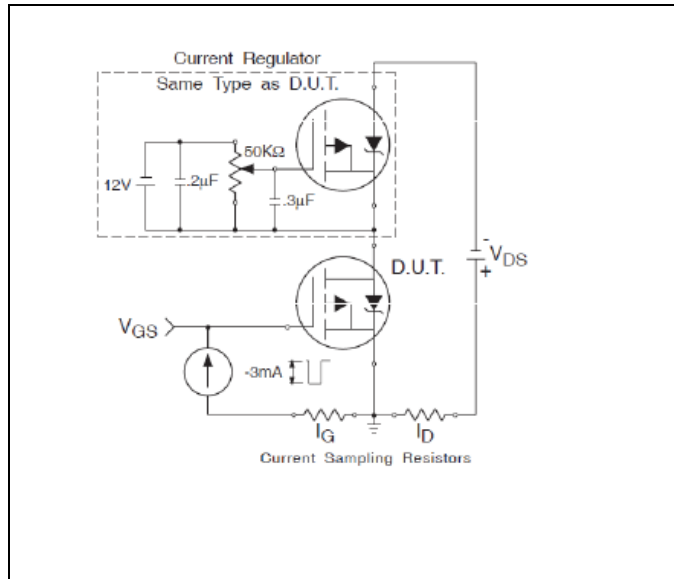


Figure 17 Gate Charge Test Circuit

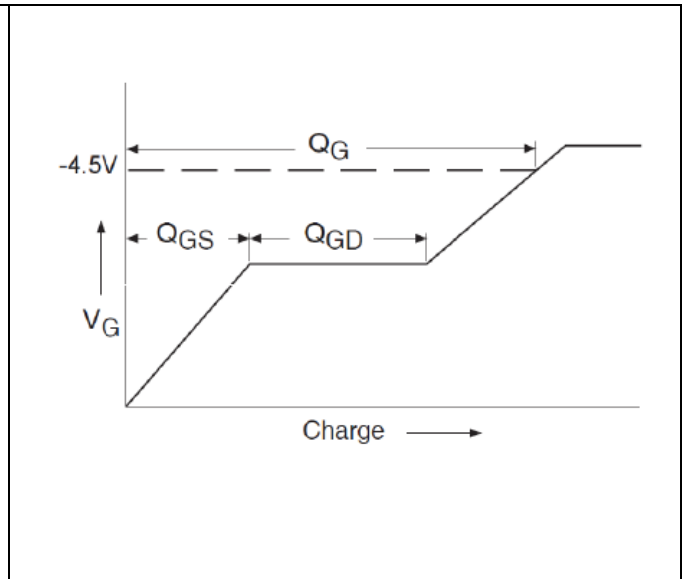


Figure 18 Gate Charge Waveform

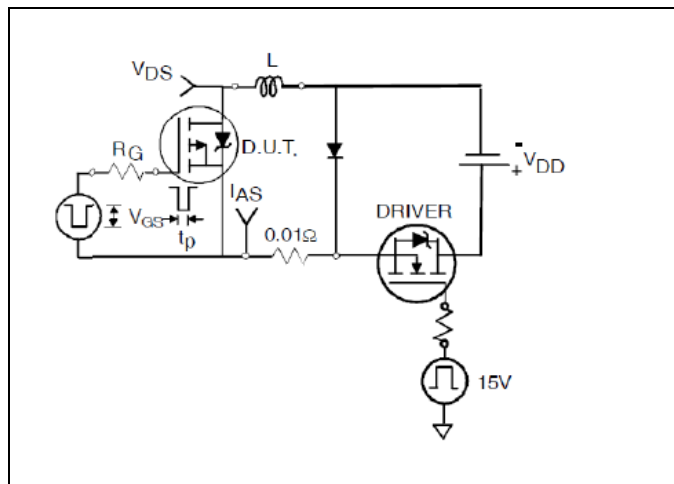


Figure 19 Unclamped Inductive Test Circuit

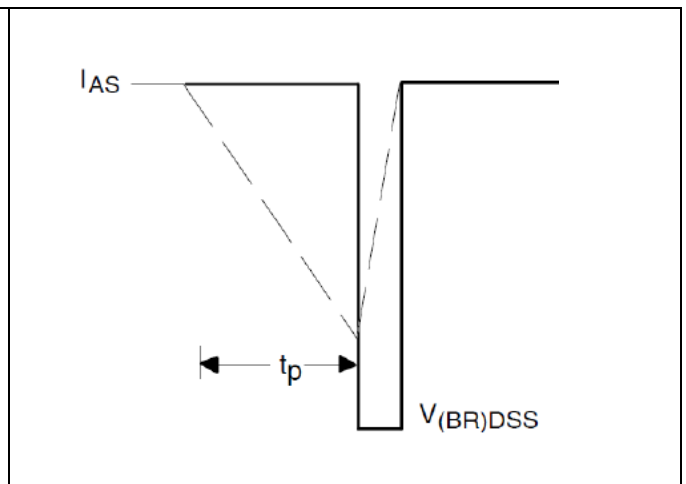


Figure 20 Unclamped Inductive Waveform

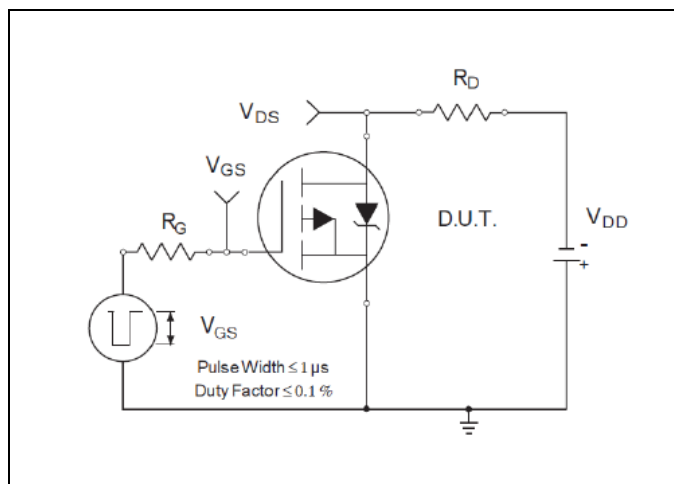


Figure 21 Switching Time Test Circuit

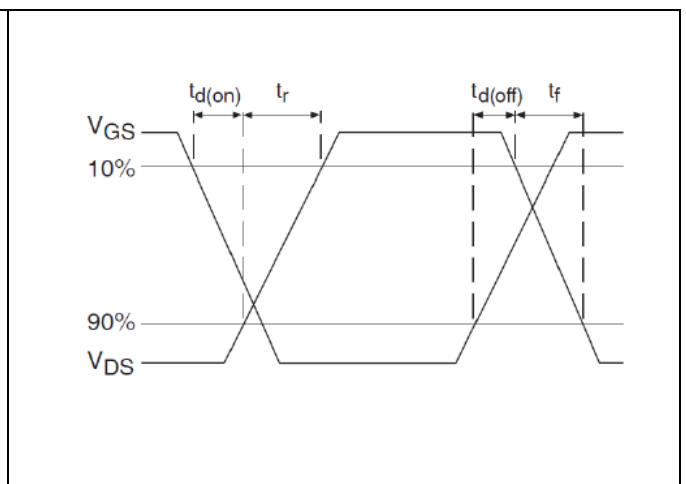


Figure 22 Switching Time Waveforms

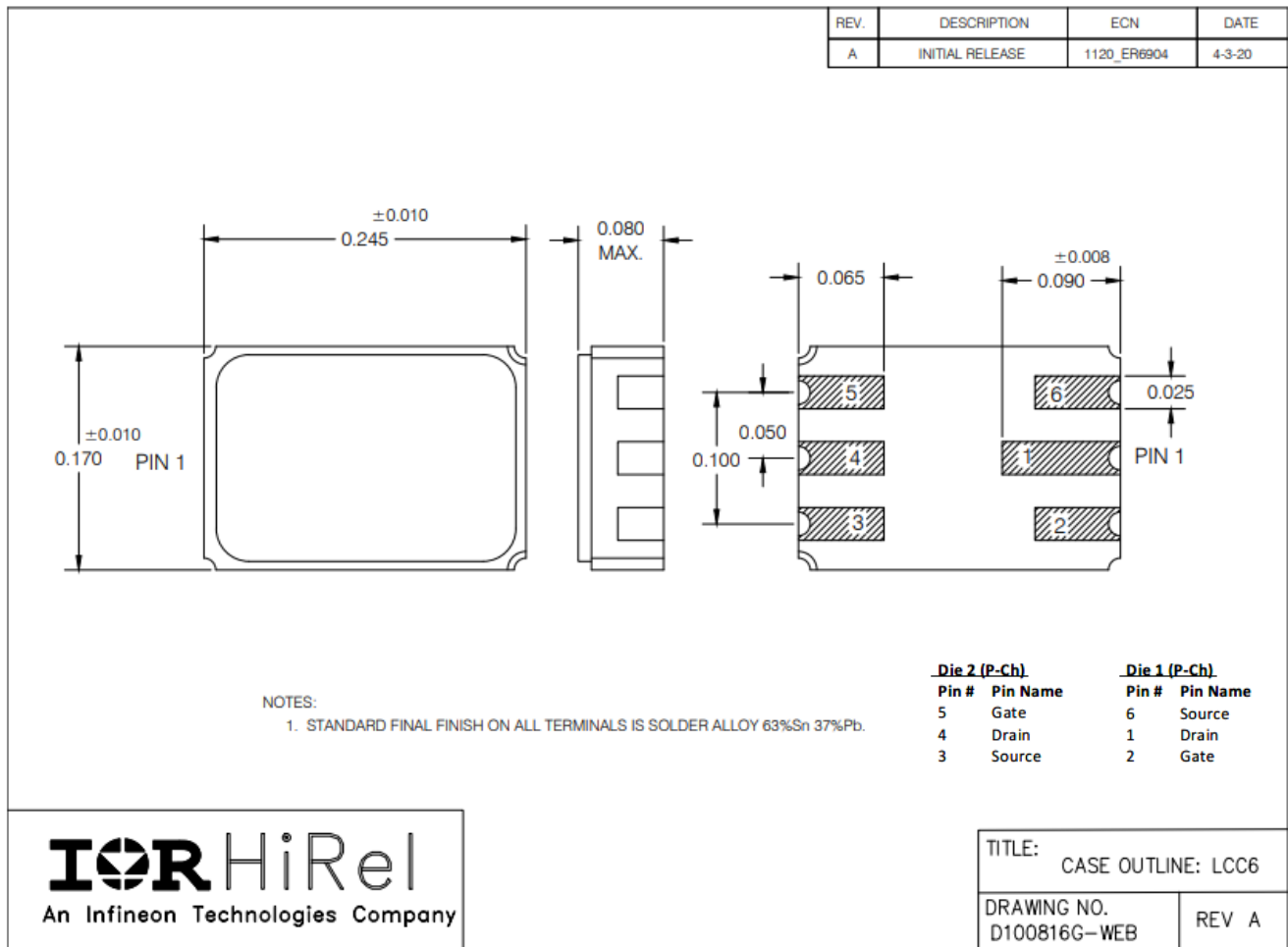
IRHLUC7970Z4

Radiation Hardened Logic Level Power MOSFET Surface-Mount (LCC-6)

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [LCC-6](#)



Revision history**Revision history**

Document version	Date of release	Description of changes
	10/20/2010	Datasheet (PD-97574)
Rev A	10/22/2018	Updated based on ECN-1120_06664
Rev B	09/26/2019	Updated based on ECN-1120_07458
Rev C	08/12/2022	Updated based on ECN-1120_09174

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