

# IRHLNME77110(JANSR2N7609U8CE)

PPD-98021

**Radiation Hardened Logic Level Power MOSFET**  
**Surface Mount (SMD-0.2e Ceramic Lid)**  
**100V, 6.5A, N-channel, R7 Technology**

## Features

- 5V CMOS and TTL compatible
- Single event effect (SEE) hardened
- Reduced CTE mismatch with PCB
- Hermetically sealed
- Ceramic package
- Drop-in replacement to SMD-0.2 package
- Light weight
- ESD rating: Class 1A per MIL-STD-750, Method 1020

## Product Summary

- **$BV_{DSS}$** : 100V
- **$I_D$** : 6.5A
- **$R_{DS(on), max}$** : 0.29 $\Omega$
- **$Q_G$** : 11nC

## Potential Applications

- Isolated DC-DC converters
- Motor drives
- Electric propulsion
- Thermal management



## Product Validation

Qualified according to MIL-PRF-19500 for space applications

## Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available. The enhanced package has the ability to withstand the thermal expansion difference between the package and PCB, maintaining the hermetic integrity of the package as well as the solder joint.

## Ordering Information

**Table 1**      **Ordering options**

| Part number     | Package                   | Screening Level | TID Level    |
|-----------------|---------------------------|-----------------|--------------|
| IRHLNME77110    | SMD-0.2e with ceramic lid | COTS            | 100 krad(Si) |
| IRHLNME73110    | SMD-0.2e with ceramic lid | COTS            | 300 krad(Si) |
| JANSR2N7609U8CE | SMD-0.2e with ceramic lid | JANS            | 100 krad(Si) |
| JANSF2N7609U8CE | SMD-0.2e with ceramic lid | JANS            | 300 krad(Si) |

**IRHLNME77110(JANSR2N7609U8CE)**

**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic)**

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**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Absolute Maximum Ratings**
**1 Absolute Maximum Ratings**
**Table 2 Absolute Maximum Ratings (Pre-Irradiation)**

| Symbol                                       | Parameter                                           | Value          | Unit           |
|----------------------------------------------|-----------------------------------------------------|----------------|----------------|
| $I_{D1} @ V_{GS} = 4.5V, T_C = 25^{\circ}C$  | Continuous Drain Current                            | 6.5            | A              |
| $I_{D2} @ V_{GS} = 4.5V, T_C = 100^{\circ}C$ | Continuous Drain Current                            | 4.1            | A              |
| $I_{DM} @ T_C = 25^{\circ}C$                 | Pulsed Drain Current <sup>1</sup>                   | 26             | A              |
| $P_D @ T_C = 25^{\circ}C$                    | Maximum Power Dissipation                           | 23.2           | W              |
|                                              | Linear Derating Factor                              | 0.18           | W/ $^{\circ}C$ |
| $V_{GS}$                                     | Gate-to-Source Voltage                              | $\pm 10$       | V              |
| $E_{AS}$                                     | Single Pulse Avalanche Energy <sup>2</sup>          | 21             | mJ             |
| $I_{AR}$                                     | Avalanche Current <sup>1</sup>                      | 6.5            | A              |
| $E_{AR}$                                     | Repetitive Avalanche Energy <sup>1</sup>            | 2.32           | mJ             |
| $dv/dt$                                      | Peak Diode Reverse Recovery <sup>3</sup>            | 4.3            | V/ns           |
| $T_J$<br>$T_{STG}$                           | Operating Junction and<br>Storage Temperature Range | -55 to +150    | $^{\circ}C$    |
|                                              | Lead Temperature                                    | 300 (for 5s)   |                |
|                                              | Weight                                              | 0.25 (Typical) |                |

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup>  $V_{DD} = 25V$ , starting  $T_J = 25^{\circ}C$ ,  $L = 0.98mH$ , Peak  $I_L = 6.5A$ ,  $V_{GS} = 10V$ 
<sup>3</sup>  $I_{SD} \leq 6.5A$ ,  $di/dt \leq 490A/\mu s$ ,  $V_{DD} \leq 100V$ ,  $T_J \leq 150^{\circ}C$

## Device Characteristics

## 2 Device Characteristics

## 2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @  $T_j = 25^\circ\text{C}$  (Unless Otherwise Specified)

| Symbol                         | Parameter                                  | Min. | Typ.  | Max. | Unit                 | Test Conditions                                                                |
|--------------------------------|--------------------------------------------|------|-------|------|----------------------|--------------------------------------------------------------------------------|
| $BV_{DSS}$                     | Drain-to-Source Breakdown Voltage          | 100  | —     | —    | V                    | $V_{GS} = 0V, I_D = 250\mu A$                                                  |
| $\Delta BV_{DSS}/\Delta T_J$   | Breakdown Voltage Temp. Coefficient        | —    | 0.105 | —    | V/ $^\circ\text{C}$  | Reference to $25^\circ\text{C}$ , $I_D = 250\mu A$                             |
| $R_{DS(on)}$                   | Static Drain-to-Source On-State Resistance | —    | —     | 0.29 | $\Omega$             | $V_{GS} = 4.5V, I_{D2} = 4.1A^1$                                               |
| $V_{GS(th)}$                   | Gate Threshold Voltage                     | 1.0  | —     | 2.0  | V                    | $V_{DS} = V_{GS}, I_D = 250\mu A$                                              |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient         | —    | -6.0  | —    | mV/ $^\circ\text{C}$ |                                                                                |
| $G_{fs}$                       | Forward Transconductance                   | 3.5  | —     | —    | S                    | $V_{DS} = 15V, I_{D2} = 4.1A^1$                                                |
| $I_{DSS}$                      | Zero Gate Voltage Drain Current            | —    | —     | 1.0  | $\mu A$              | $V_{DS} = 80V, V_{GS} = 0V$                                                    |
|                                |                                            | —    | —     | 10   |                      | $V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$                           |
| $I_{GSS}$                      | Gate-to-Source Leakage Forward             | —    | —     | 100  | nA                   | $V_{GS} = 10V$                                                                 |
|                                | Gate-to-Source Leakage Reverse             | —    | —     | -100 |                      | $V_{GS} = -10V$                                                                |
| $Q_G$                          | Total Gate Charge                          | —    | —     | 11   | nC                   | $I_{D1} = 6.5A$                                                                |
| $Q_{GS}$                       | Gate-to-Source Charge                      | —    | —     | 4.0  |                      | $V_{DS} = 50V$                                                                 |
| $Q_{GD}$                       | Gate-to-Drain ('Miller') Charge            | —    | —     | 6.0  |                      | $V_{GS} = 4.5V$                                                                |
| $t_{d(on)}$                    | Turn-On Delay Time                         | —    | —     | 18   | ns                   | $I_{D1} = 6.5A^{**}$<br>$V_{DD} = 50V$<br>$R_G = 7.5\Omega$<br>$V_{GS} = 5.0V$ |
| $t_r$                          | Rise Time                                  | —    | —     | 75   |                      |                                                                                |
| $t_{d(off)}$                   | Turn-Off Delay Time                        | —    | —     | 50   |                      |                                                                                |
| $t_f$                          | Fall Time                                  | —    | —     | 12   |                      |                                                                                |
| $L_s + L_D$                    | Total Inductance                           | —    | 6.8   | —    | nH                   | Measured from center of Drain pad to center of Source pad                      |
| $C_{iss}$                      | Input Capacitance                          | —    | 572   | —    | pF                   | $V_{GS} = 0V$                                                                  |
| $C_{oss}$                      | Output Capacitance                         | —    | 124   | —    |                      | $V_{DS} = 20V$                                                                 |
| $C_{rss}$                      | Reverse Transfer Capacitance               | —    | 1.6   | —    |                      | $f = 1.0MHz$                                                                   |
| $R_G$                          | Gate Resistance                            | —    | 10.5  | —    | $\Omega$             | $f = 1.0MHz$ , open drain                                                      |

\*\* Switching speed maximum limits are based on manufacturing test equipment and capability.

<sup>1</sup> Pulse width  $\leq 300\mu s$ ; Duty Cycle  $\leq 2\%$

**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Device Characteristics**
**2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)**
**Table 4 Source-Drain Diode Characteristics**

| Symbol          | Parameter                                       | Min.                                                                                           | Typ. | Max. | Unit | Test Conditions                                                                        |
|-----------------|-------------------------------------------------|------------------------------------------------------------------------------------------------|------|------|------|----------------------------------------------------------------------------------------|
| I <sub>S</sub>  | Continuous Source Current (Body Diode)          | —                                                                                              | —    | 6.5  | A    |                                                                                        |
| I <sub>SM</sub> | Pulsed Source Current (Body Diode) <sup>1</sup> | —                                                                                              | —    | 26   | A    |                                                                                        |
| V <sub>SD</sub> | Diode Forward Voltage                           | —                                                                                              | —    | 1.2  | V    | T <sub>J</sub> = 25°C, I <sub>S</sub> = 6.5A, V <sub>GS</sub> = 0V <sup>2</sup>        |
| t <sub>rr</sub> | Reverse Recovery Time                           | —                                                                                              | —    | 215  | ns   | T <sub>J</sub> = 25°C, I <sub>F</sub> = 6.5A, V <sub>DD</sub> ≤ 25V<br>di/dt = 100A/μs |
| Q <sub>rr</sub> | Reverse Recovery Charge                         | —                                                                                              | 703  | —    | nC   |                                                                                        |
| t <sub>on</sub> | Forward Turn-On Time                            | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> ) |      |      |      |                                                                                        |

**2.3 Thermal Characteristics**
**Table 5 Thermal Resistance**

| Symbol          | Parameter        | Min. | Typ. | Max. | Unit                      |
|-----------------|------------------|------|------|------|---------------------------|
| $R_{\theta JC}$ | Junction-to-Case | —    | —    | 5.4  | $^\circ\text{C}/\text{W}$ |

**2.4 Radiation Characteristics**

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**2.4.1 Electrical Characteristics — Post Total Dose Irradiation**
**Table 6 Electrical Characteristics @  $T_J = 25^\circ\text{C}$ , Post Total Dose Irradiation <sup>3, 4</sup>**

| Symbol       | Parameter                                                          | Up to 300 krad (Si) <sup>5</sup> |      | Unit          | Test Conditions                                 |
|--------------|--------------------------------------------------------------------|----------------------------------|------|---------------|-------------------------------------------------|
|              |                                                                    | Min.                             | Max. |               |                                                 |
| $BV_{DSS}$   | Drain-to-Source Breakdown Voltage                                  | 100                              | —    | V             | $V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$   |
| $V_{GS(th)}$ | Gate Threshold Voltage                                             | 1.0                              | 2.0  | V             | $V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$      |
| $I_{GSS}$    | Gate-to-Source Leakage Forward                                     | —                                | 100  | nA            | $V_{GS} = 10\text{V}$                           |
|              | Gate-to-Source Leakage Reverse                                     | —                                | -100 |               | $V_{GS} = -10\text{V}$                          |
| $I_{DSS}$    | Zero Gate Voltage Drain Current                                    | —                                | 1.0  | $\mu\text{A}$ | $V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$    |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance (TO-3) <sup>2</sup>     | —                                | 0.26 | $\Omega$      | $V_{GS} = 4.5\text{V}$ , $I_{D2} = 4.1\text{A}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance (SMD-0.2E) <sup>2</sup> | —                                | 0.29 | $\Omega$      | $V_{GS} = 4.5\text{V}$ , $I_{D2} = 4.1\text{A}$ |
| $V_{SD}$     | Diode Forward Voltage                                              | —                                | 1.2  | V             | $V_{GS} = 0\text{V}$ , $I_F = 6.5\text{A}$      |

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup> Pulse width  $\leq 300\mu\text{s}$ ; Duty Cycle  $\leq 2\%$ 
<sup>3</sup> Total Dose Irradiation with  $V_{GS}$  Bias.  $V_{GS} = 10\text{V}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>4</sup> Total Dose Irradiation with  $V_{DS}$  Bias.  $V_{DS} = 80\text{V}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

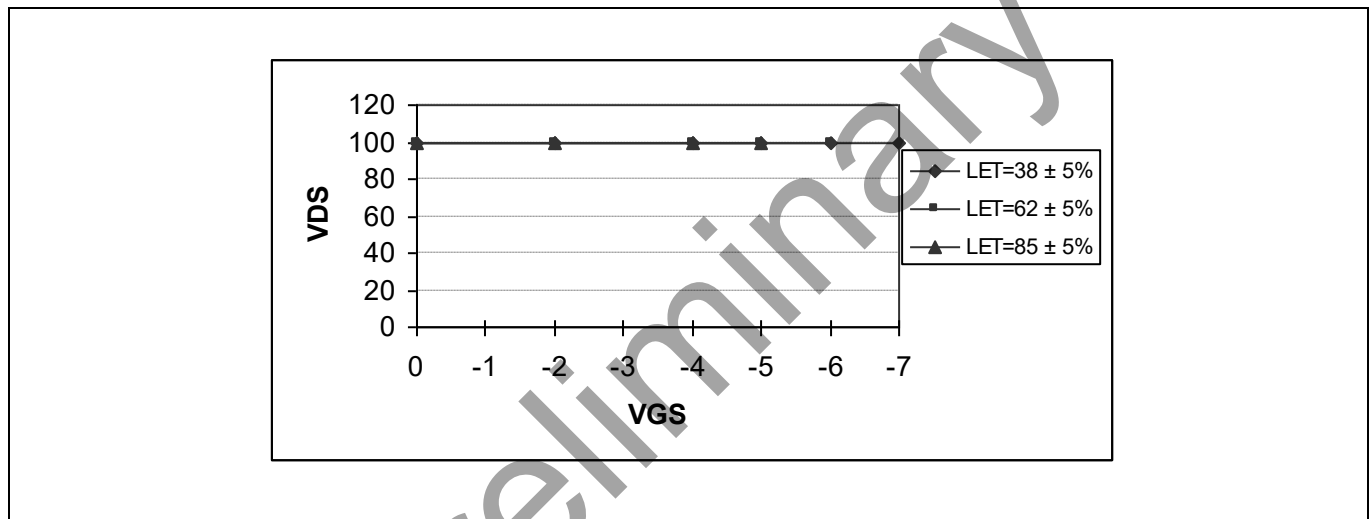
<sup>5</sup> Part numbers IRHLNME77110 (JANSR2N7609U8CE) and IRHLNME73110 (JANSF2N7609U8CE)

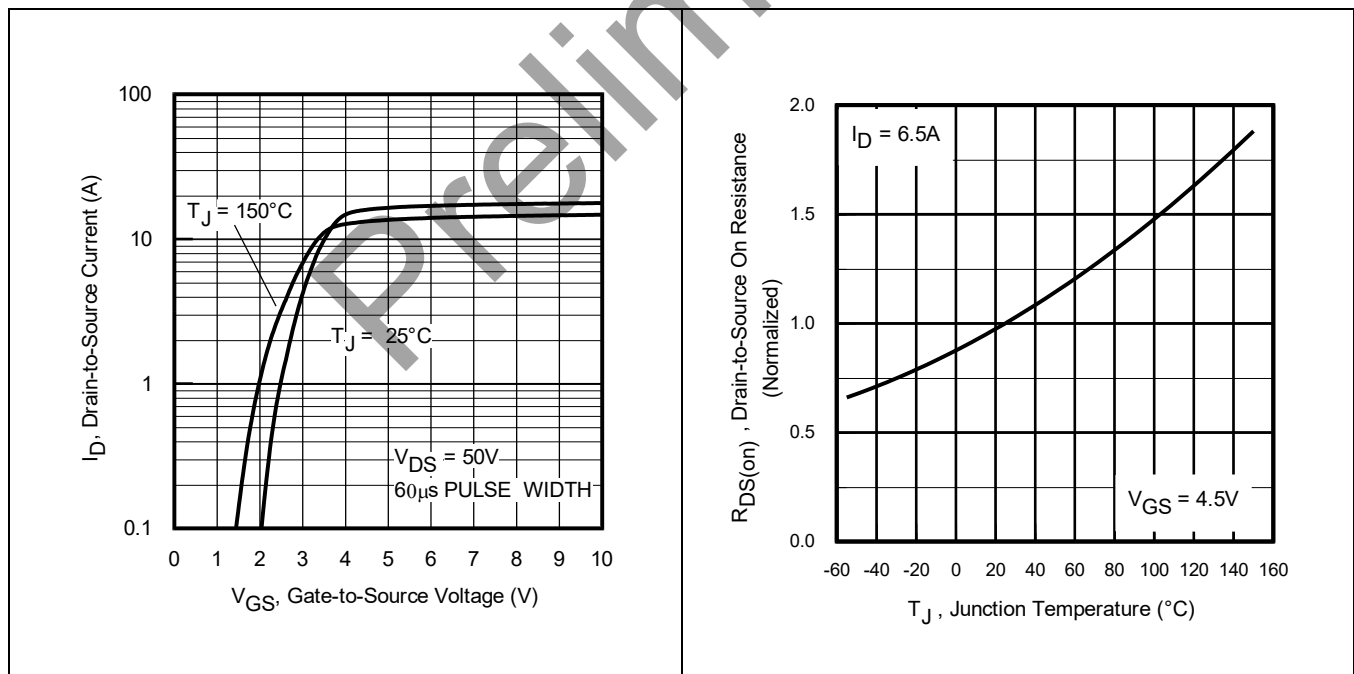
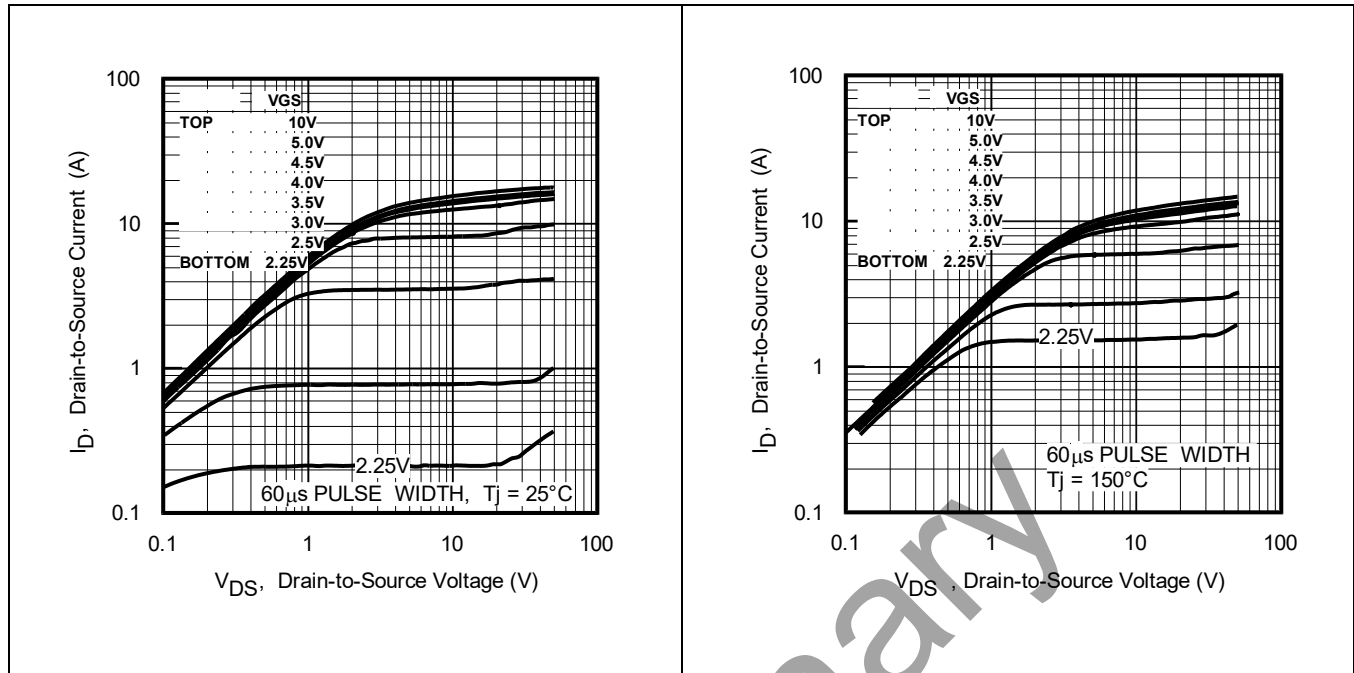
**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Device Characteristics**
**2.4.2 Single Event Effects — Safe Operating Area**

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

**Table 7 Worst Case Single Event Effects Safe Operating Area**

| LET<br>(MeV·cm <sup>2</sup> /mg) | Energy<br>(MeV) | Range<br>(μm) | V <sub>DS</sub> (V)  |                       |                       |                       |                       |                       |
|----------------------------------|-----------------|---------------|----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
|                                  |                 |               | V <sub>GS</sub> = 0V | V <sub>GS</sub> = -2V | V <sub>GS</sub> = -4V | V <sub>GS</sub> = -5V | V <sub>GS</sub> = -6V | V <sub>GS</sub> = -7V |
| 38 ± 5%                          | 300 ± 7.5%      | 38 ± 7.5%     | 100                  | 100                   | 100                   | 100                   | 100                   | 100                   |
| 62 ± 5%                          | 355 ± 7.5%      | 33 ± 7.5%     | 100                  | 100                   | 100                   | 100                   | 100                   | —                     |
| 85 ± 5%                          | 380 ± 10%       | 29 ± 7.5%     | 100                  | 100                   | 100                   | 100                   | —                     | —                     |


**Figure 1 Worst Case Single Event Effect, Safe Operating Area**

**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Electrical Characteristics Curves (Pre-irradiation)**
**3 Electrical Characteristics Curves (Pre-irradiation)**


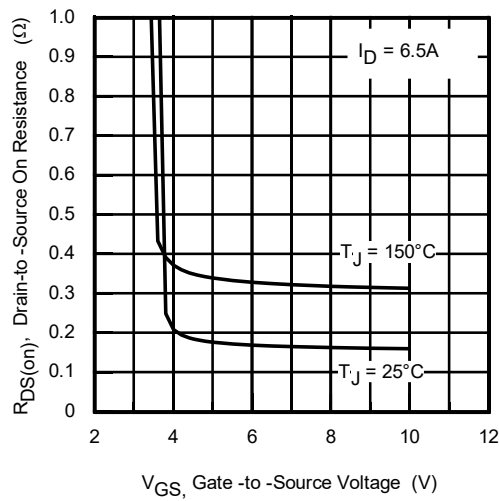
**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Electrical Characteristics Curves (Pre-irradiation)**


**Figure 6** Typical On-Resistance Vs. Gate Voltage

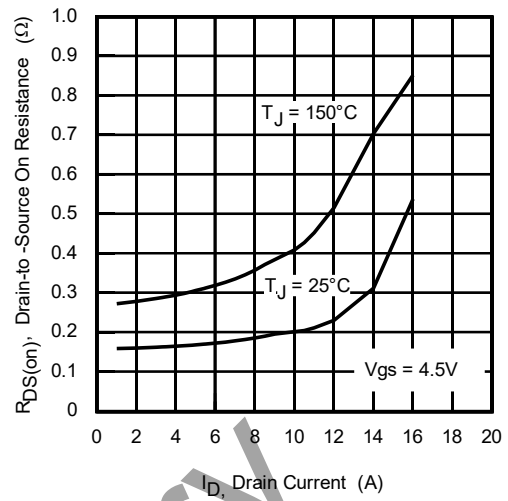


**Figure 7** Typical On-Resistance Vs. Drain Current

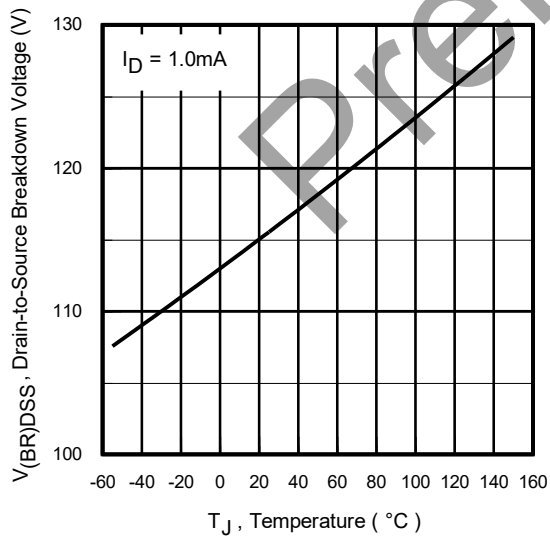


**Figure 8** Typical Drain-to-Source Breakdown Voltage Vs. Temperature

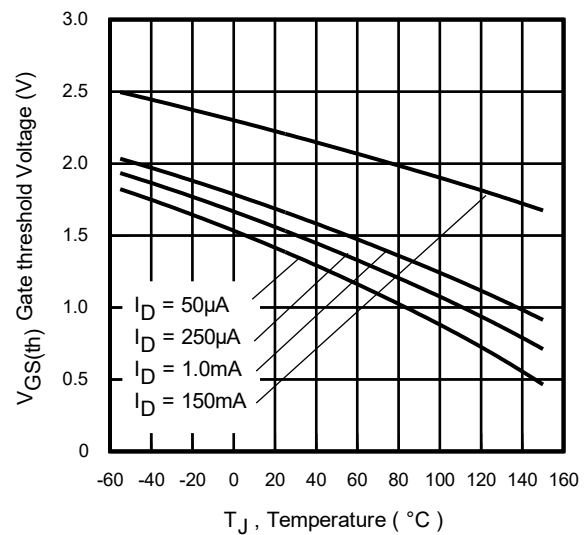


**Figure 9** Typical Threshold Voltage Vs. Temperature

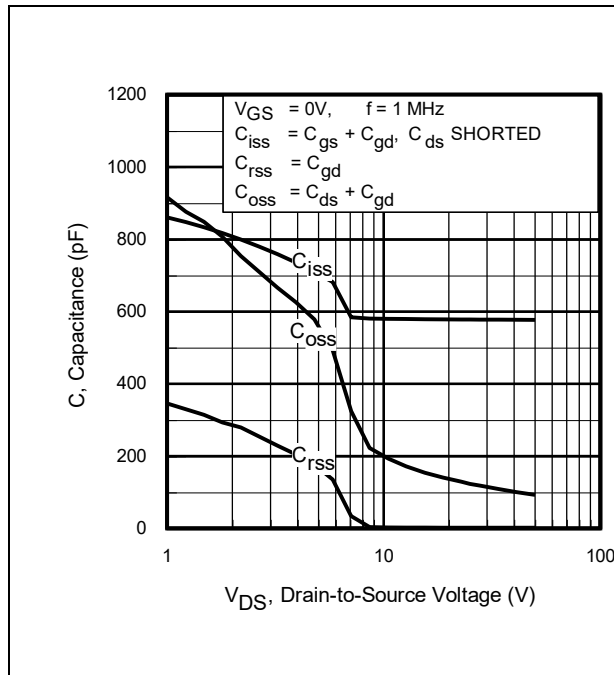
**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Electrical Characteristics Curves (Pre-irradiation)**


**Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage**

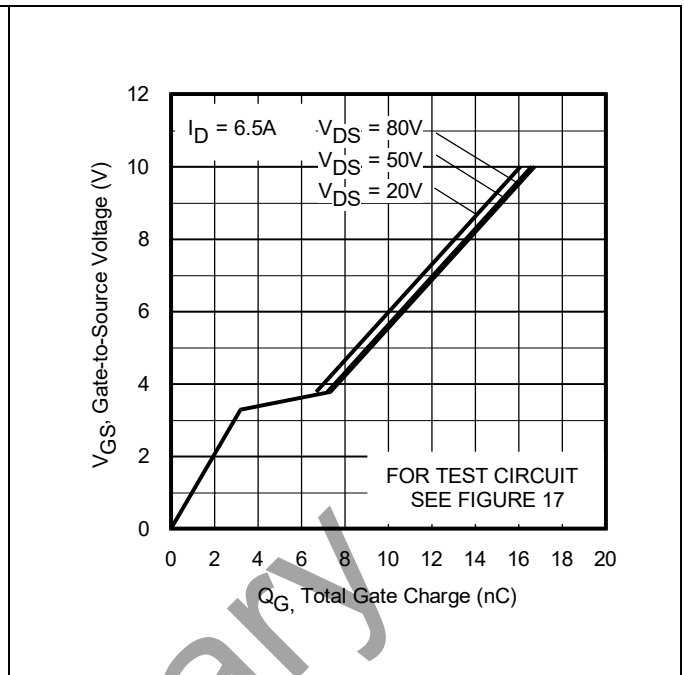


**Figure 11 Typical Gate Charge Vs. Gate-to-Source Voltage**

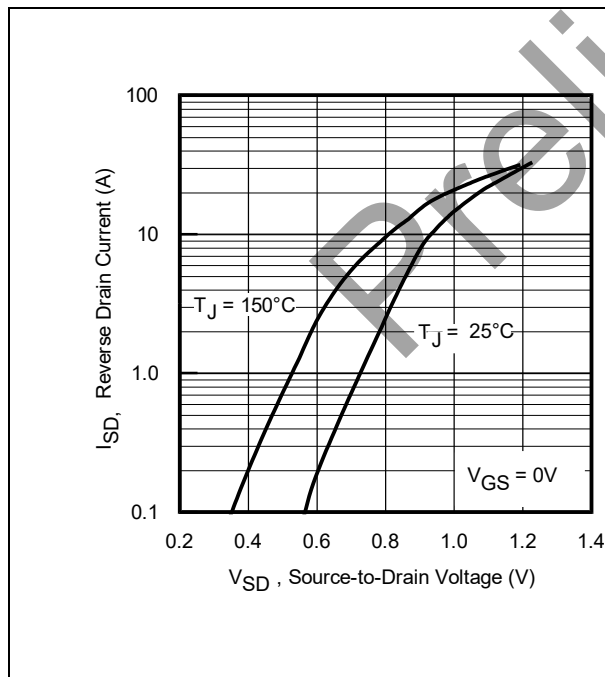


**Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage**

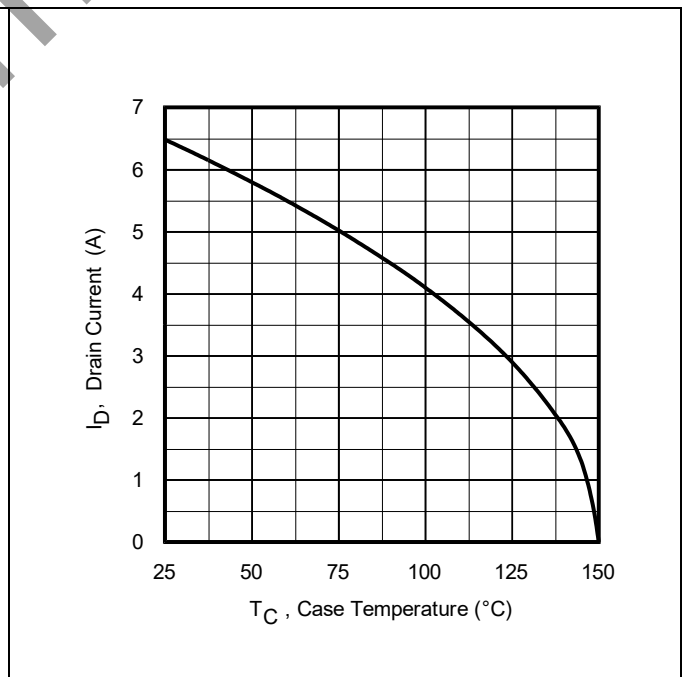
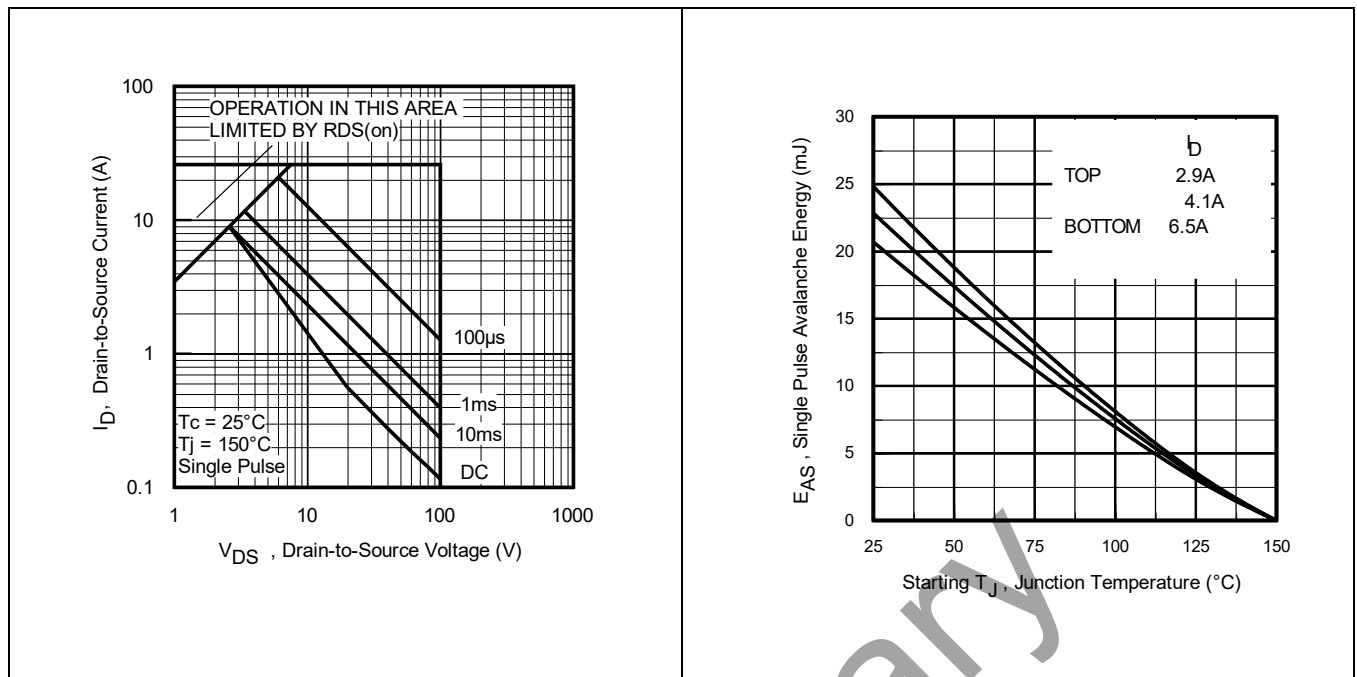
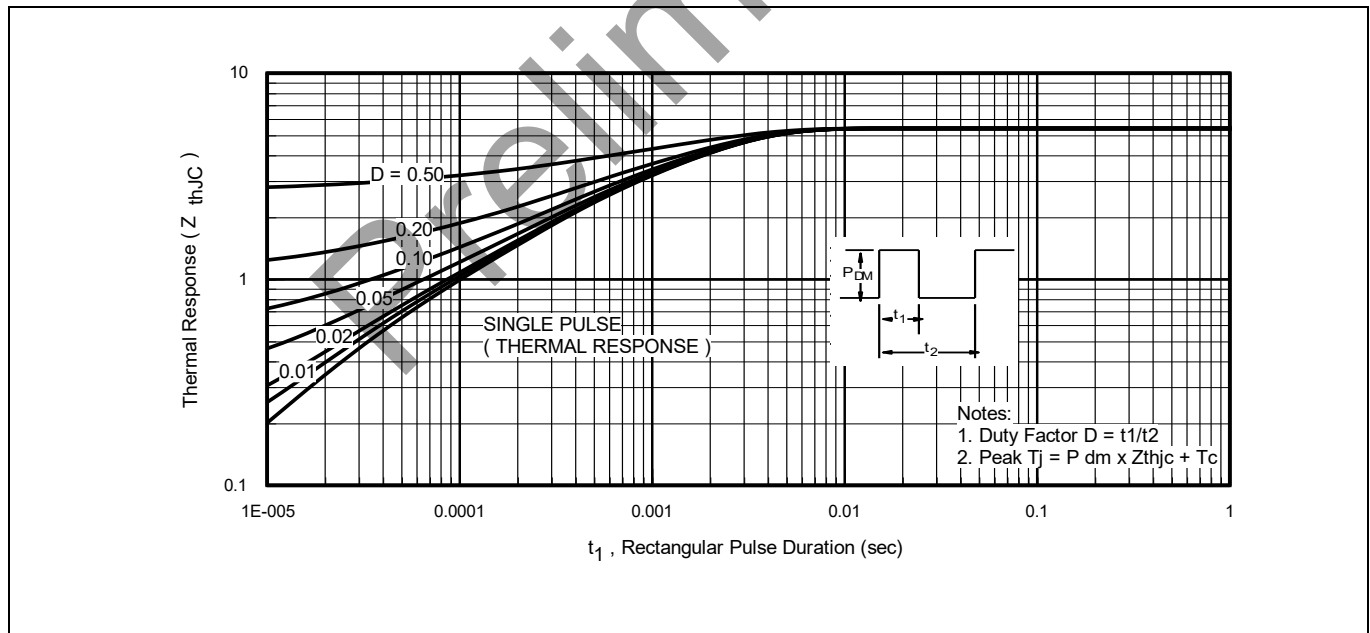


**Figure 13 Maximum Drain Current Vs. Case Temperature**

**IRHLNME77110(JANSR2N7609U8CE)**
**Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)**
**Electrical Characteristics Curves (Pre-irradiation)**

**Figure 14 Maximum Safe Operating Area**
**Figure 15 Maximum Avalanche Energy Vs. Junction Temperature**

**Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case**

# IRHLNME77110(JANSR2N7609U8CE)

Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)

Test Circuits (Pre-irradiation)

## 4 Test Circuits (Pre-irradiation)

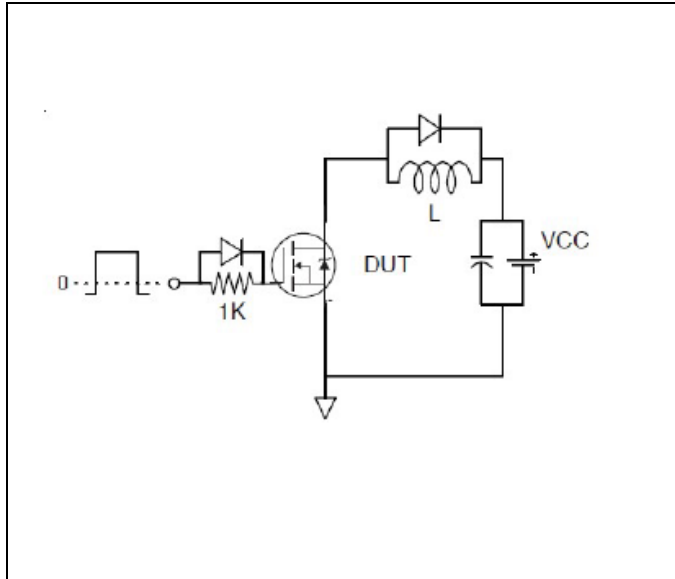


Figure 17 Gate Charge Test Circuit

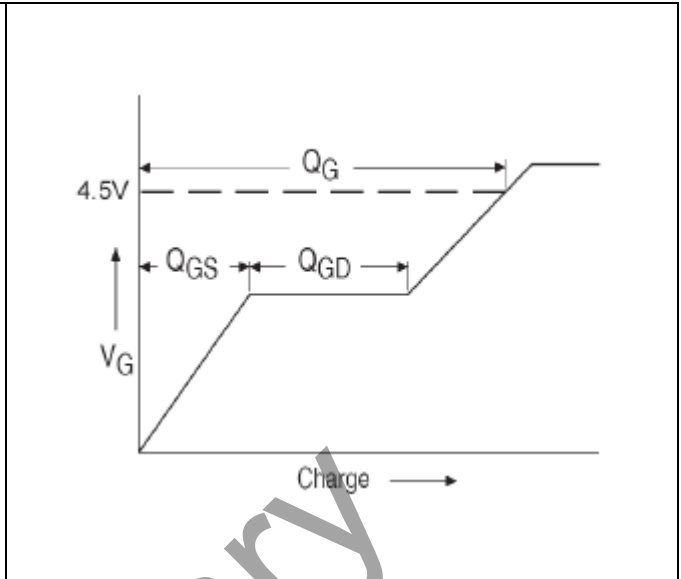


Figure 18 Gate Charge Waveform

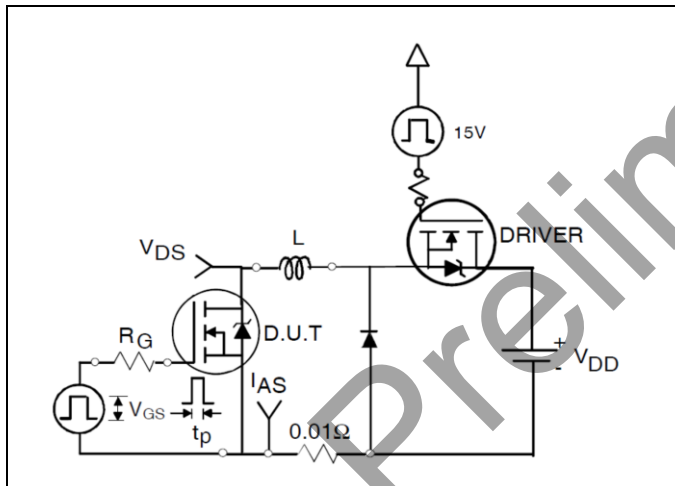


Figure 19 Unclamped Inductive Test Circuit

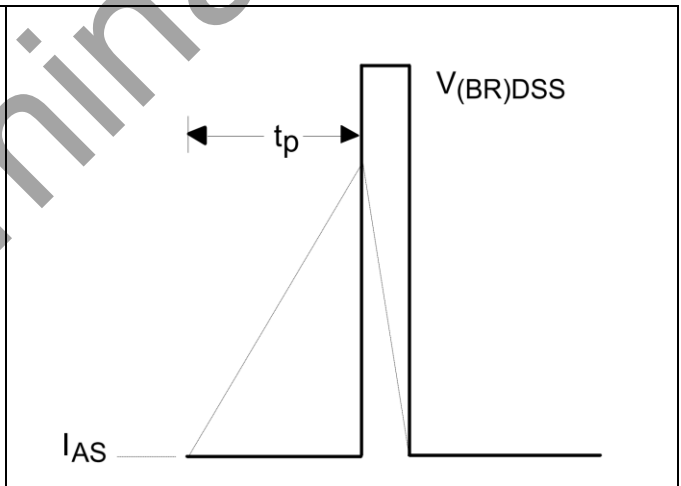


Figure 20 Unclamped Inductive Waveform

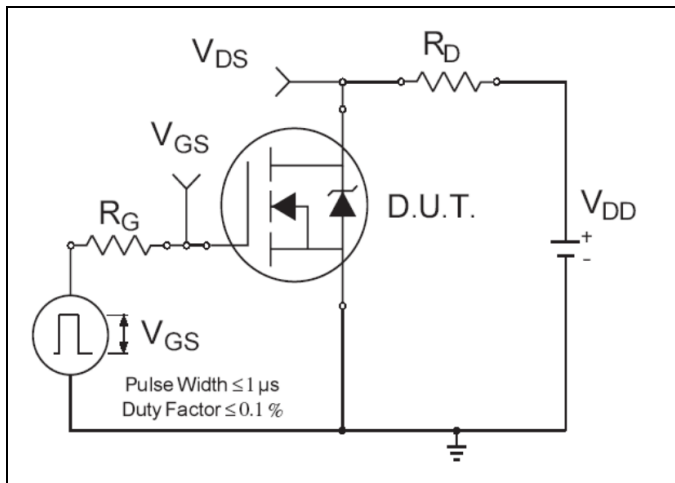


Figure 21 Switching Time Test Circuit

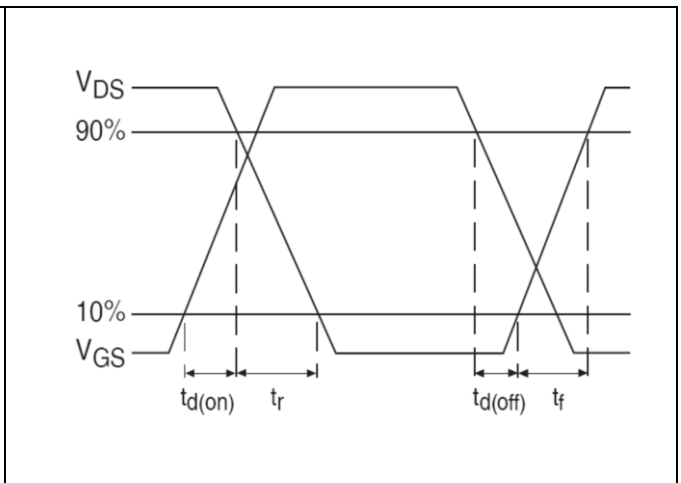


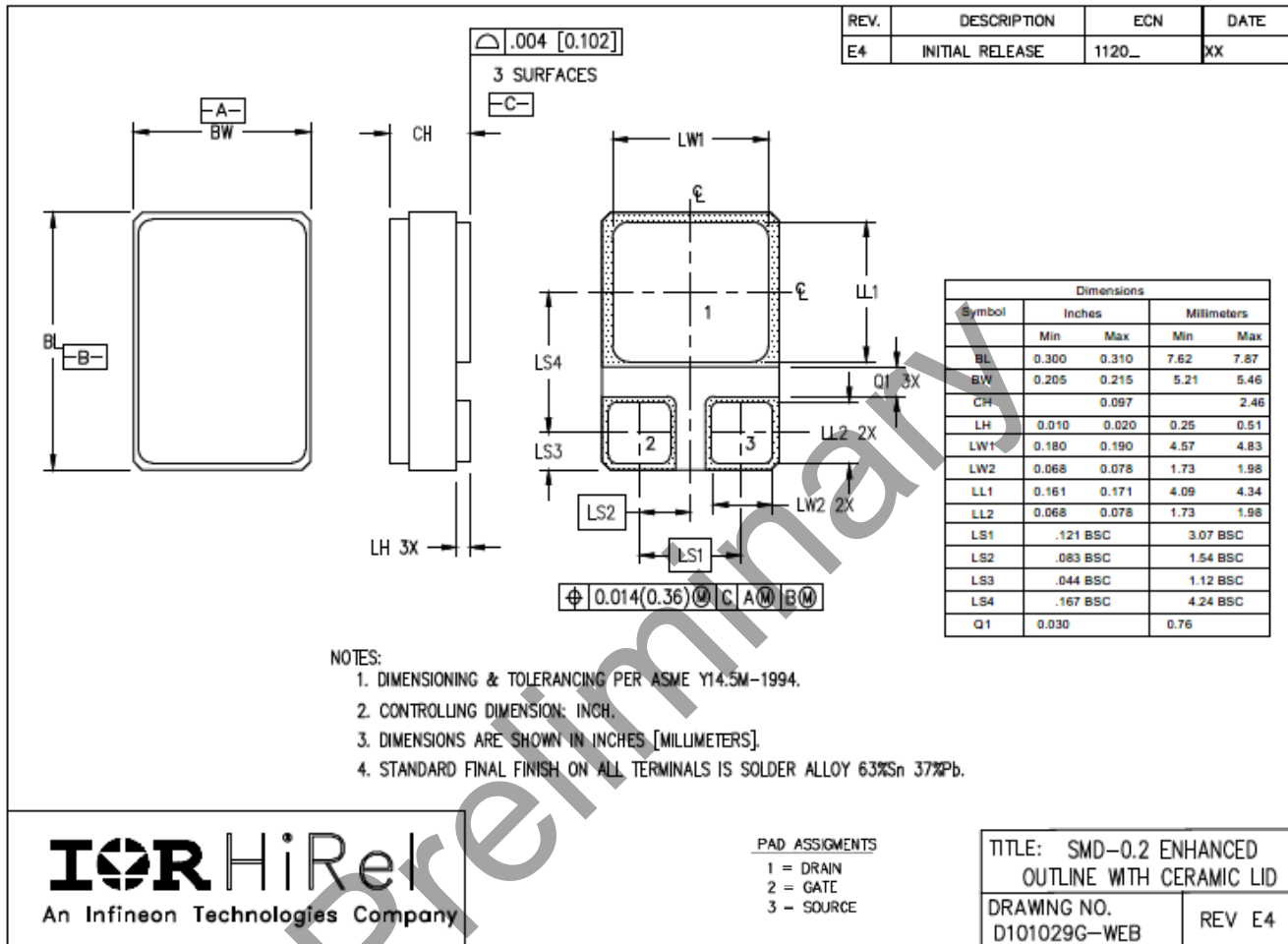
Figure 22 Switching Time Waveforms

## IRHLNME77110(JANSR2N7609U8CE)

Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)

## Package Outline

## 5 Package Outline

Note: For the most updated package outline, please see the website: [TBD](#) [Ceramic Lid](#)

**IRHLNME77110(JANSR2N7609U8CE)****Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2e Ceramic Lid)****Revision history****Revision history**

| Document version | Date of release | Description of changes                            |
|------------------|-----------------|---------------------------------------------------|
|                  | 07/23/2024      | Preliminary datasheet with PPD number (PPD-98021) |

Preliminary

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