IRHLNM87Y20, IRHLNMC87Y20

PD-97811F

Radiation Hardened Logic Level Power MOSFET
Surface Mount (SMD-0.2)
20V, 17A, N-channel, R8 Technology

Features

- 5V CMOS and TTL compatible
- Low $R_{DS(on)}$
- Single event effect (SEE) hardened
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Light weight
- Surface mount
- ESD rating: Class 1B per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** 20V
- **I_D:** 17A
- **$R_{DS(on),max}$:** 15mΩ
- **$Q_{G,\,max}$:** 26nC

SMD-0.2

Potential Applications

- Synchronous rectification
- Redundant power distribution
- Motor drives

Product Validation

Adhered to JANS screening flow according to MIL-PRF-19500 for space applications

Description

IR HiRel R8 Logic Level power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHLNM87Y20	SMD-0.2	COTS	100 krad(Si)
IRHLNM83Y20	SMD-0.2	COTS	300 krad(Si)
IRHLNM87Y20SCS	SMD-0.2	S-level	100 krad(Si)
IRHLNM83Y20SCS	SMD-0.2	S-level	300 krad(Si)
IRHLNMC87Y20	SMD-0.2 with ceramic lid	COTS	100 krad(Si)
IRHLNMC83Y20	SMD-0.2 with ceramic lid	COTS	300 krad(Si)
IRHLNMC87Y20SCS	SMD-0.2 with ceramic lid	S-level	100 krad(Si)
IRHLNMC83Y20SCS	SMD-0.2 with ceramic lid	S-level	300 krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	17*	A
I_{D2} @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	17*	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	68	A
P_D @ T_C = 25°C	Maximum Power Dissipation	36	W
	Linear Derating Factor	0.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
E_{AS}	Single Pulse Avalanche Energy [2]	37	mJ
I_{AR}	Avalanche Current [1]	17	A
E_{AR}	Repetitive Avalanche Energy [1]	3.6	mJ
dv/dt	Peak Diode Reverse Recovery [3]	3.75	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	0.25 (Typical)	g

*Current is limited by package

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] V_{DD} = 20V, starting T_J = 25°C, L = 0.26mH, Peak I_L = 17A, V_{GS} = 12V
[3] $I_{SD} \leq$ 17A, di/dt $\leq$ 419A/µs, $V_{DD} \leq$ 20V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.028	—	V/°C	Reference to 25°C, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	12	15	mΩ	V_{GS} = 4.5V, I_{D2} = 17A [1]
		—	11	14		V_{GS} = 7.0V, I_{D2} = 17A [1]
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.3	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.2	—	mV/°C	
Gfs	Forward Transconductance	20	—	—	S	V_{DS} = 15V, I_{D2} = 17A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V_{DS} = 16V, V_{GS} = 0V
		—	—	10		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 12V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -12V
Q_G	Total Gate Charge	—	21	26	nC	I_{D1} = 17A V_{DS} = 10V V_{GS} = 5.5V
Q_{GS}	Gate-to-Source Charge	—	6.2	8.0		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	4.1	8.0		
$t_{d(on)}$	Turn-On Delay Time	—	18	24	ns	I_{D1} = 17A ** V_{DD} = 10V R_G = 2.35Ω V_{GS} = 5.5V
t_r	Rise Time	—	73	150		
$t_{d(off)}$	Turn-Off Delay Time	—	24	32		
t_f	Fall Time	—	10	18		
$L_s + L_D$	Total Inductance	—	1.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	2336	—	pF	V_{GS} = 0V V_{DS} = 20V ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	596	—		
C_{rss}	Reverse Transfer Capacitance	—	147	—		
R_G	Gate Resistance	—	0.76	—	Ω	ƒ = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	68	A	
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 17A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	41	ns	T_J = 25°C, I_F = 17A, $V_{DD} \leq$ 20V di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	—	—	33	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	3.5	°C/W

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si)		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	V	V_{GS} = 0V, I_D = 250µA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.3	V	V_{DS} = V_{GS}, I_D = 250µA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 12V
	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -12V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	µA	V_{DS} = 16V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	15	mΩ	V_{GS} = 4.5V, I_{D2} = 17A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.2) [2]	—	15	mΩ	V_{GS} = 4.5V, I_{D2} = 17A
V_{SD}	Diode Forward Voltage	—	1.0	V	V_{GS} = 0V, I_F = 17A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 16V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Worst Case Single Event Effects Safe Operating Area

LET ($MeV \cdot cm^2/mg$)	Energy (MeV)	Range (µm)	V_{DS} (V)					
			V_{GS} = 0V	V_{GS} = -1V	V_{GS} = -2V	V_{GS} = -3V	V_{GS} = -4V	V_{GS} = -5V
40 ± 5%	312 ± 5%	40.1 ± 5%	18	18	18	18	17	15
67.9± 5%	675 ± 5%	52.5 ± 5%	17	17	17	17	14	12
93.2 ± 5%	1105 ± 5%	65.1 ± 5%	17	16	16	14	10	8

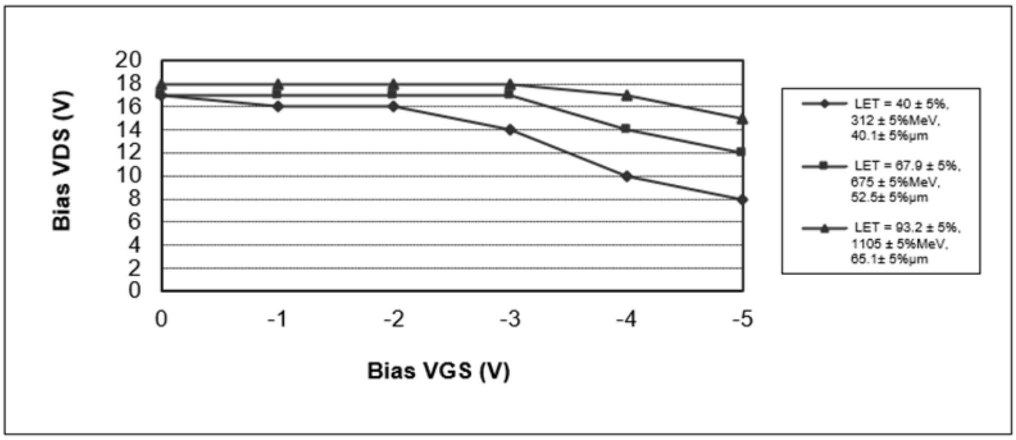


Figure 1 Worst Case Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

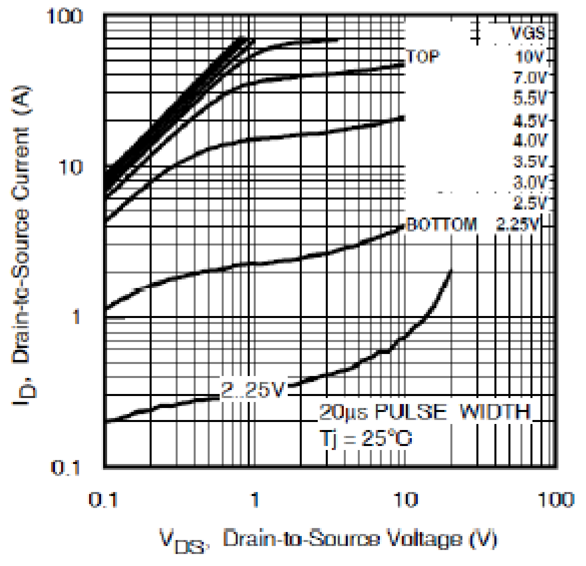


Figure 2 **Typical Output Characteristics**

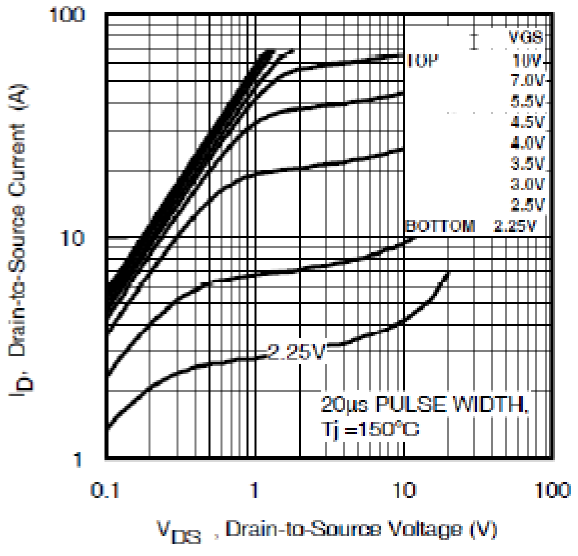


Figure 3 **Typical Output Characteristics**

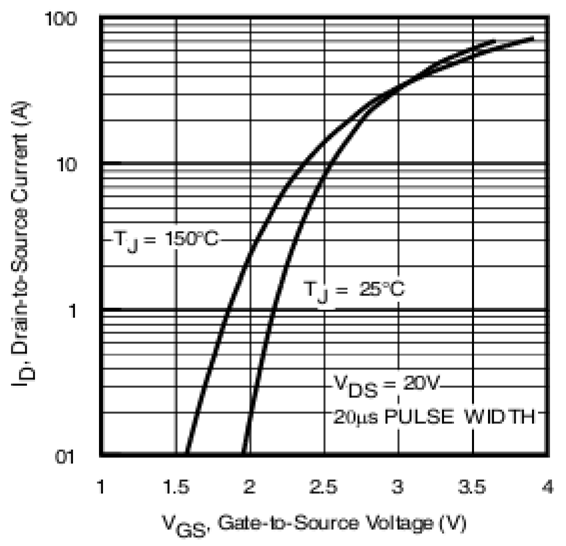


Figure 4 **Typical Transfer Characteristics**

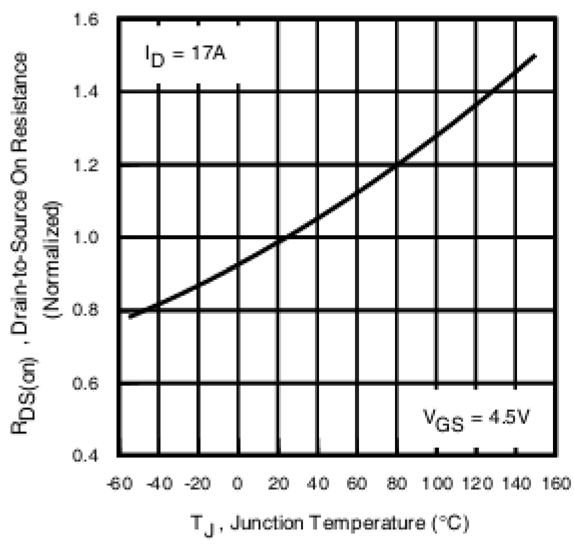


Figure 5 **Normalized On-Resistance Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

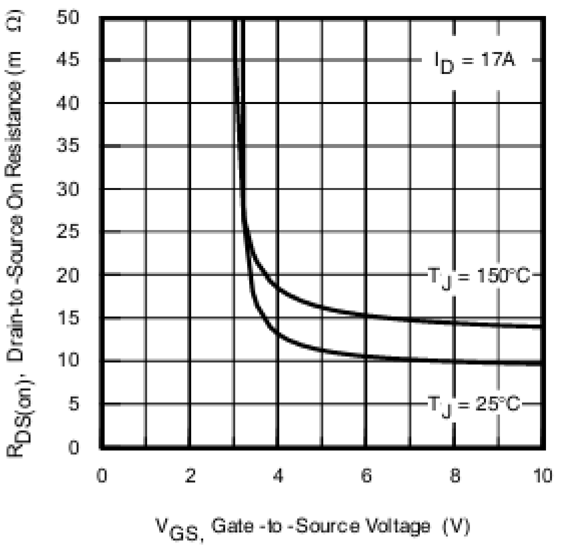


Figure 6 **Typical On-Resistance Vs. Gate Voltage**

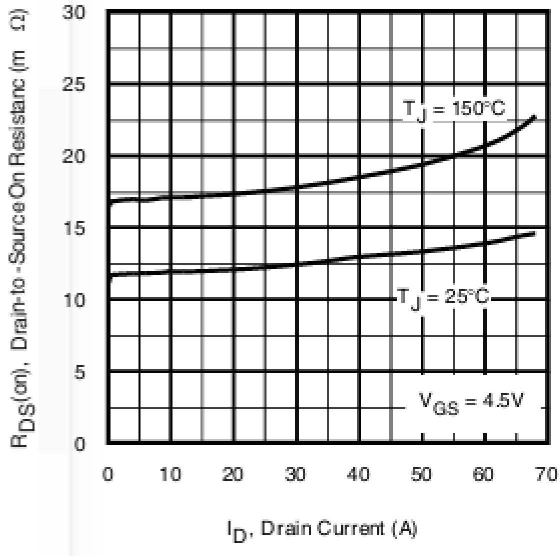


Figure 7 **Typical On-Resistance Vs. Drain Current**

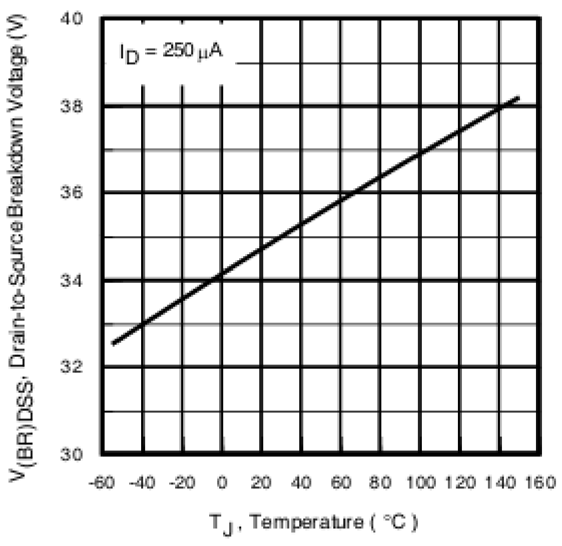


Figure 8 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

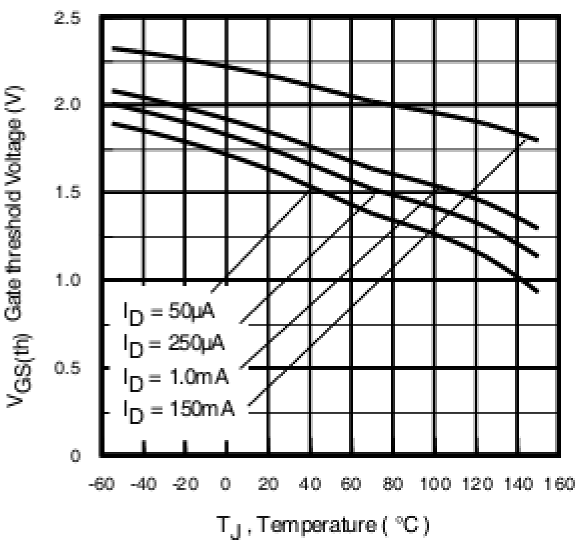


Figure 9 **Typical Threshold Voltage Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

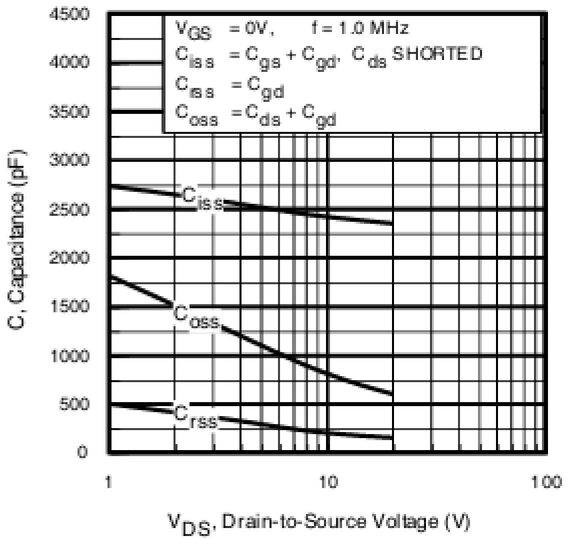


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

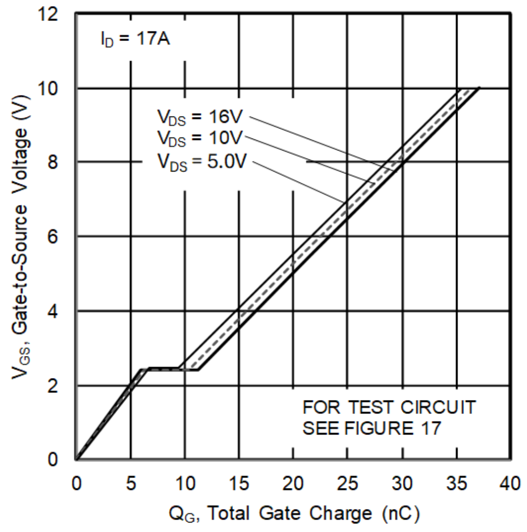


Figure 11 Typical Gate Charge Vs. Gate-to-Source Voltage

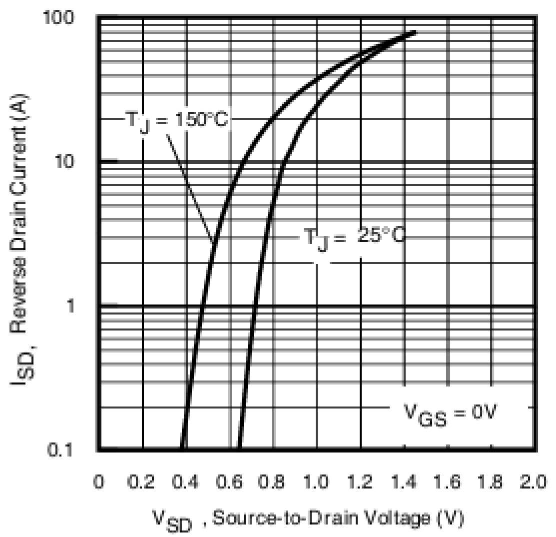


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

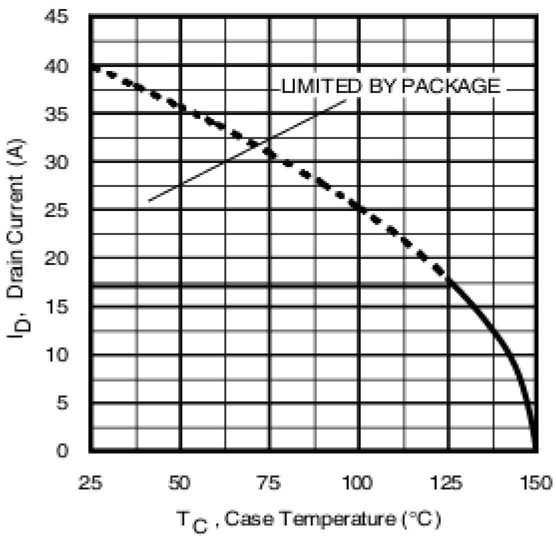


Figure 13 Maximum Drain Current Vs. Case Temperature

Electrical Characteristics Curves (Pre-irradiation)

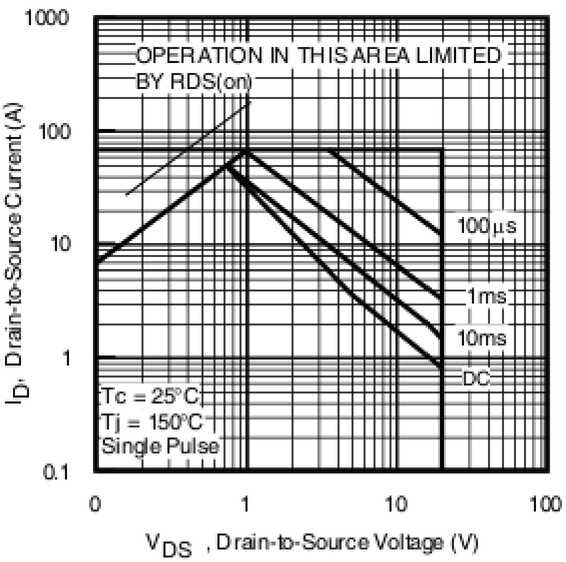


Figure 14 Maximum Safe Operating Area

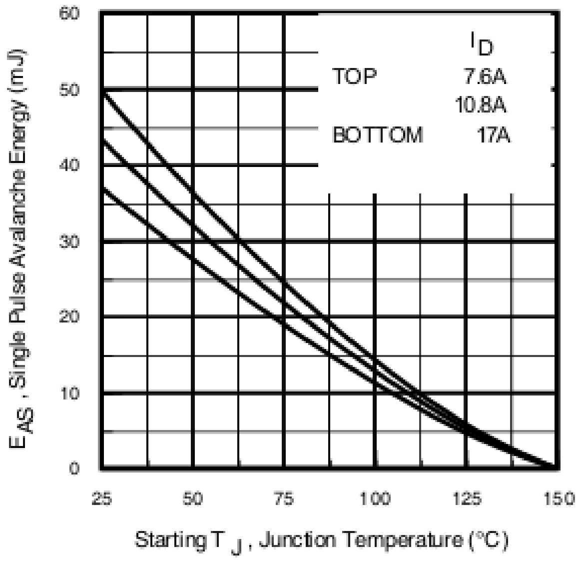


Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

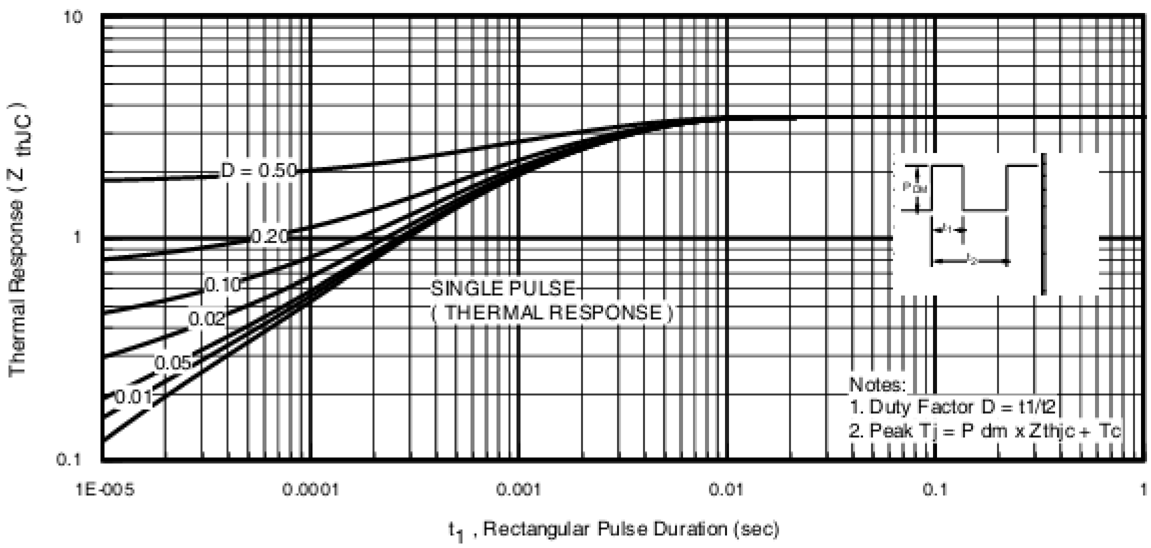


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

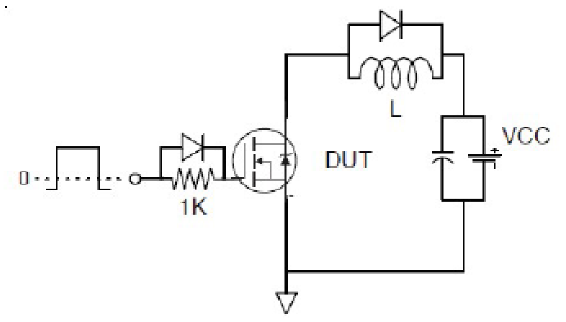


Figure 17 **Gate Charge Test Circuit**

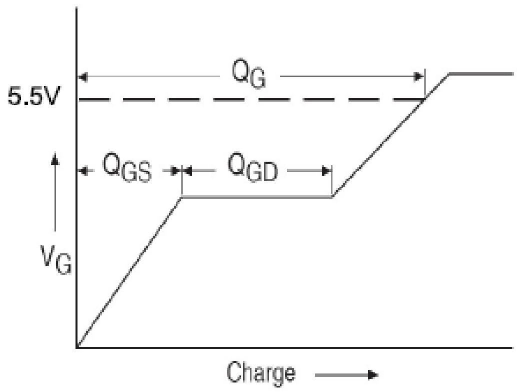


Figure 18 **Gate Charge Waveform**

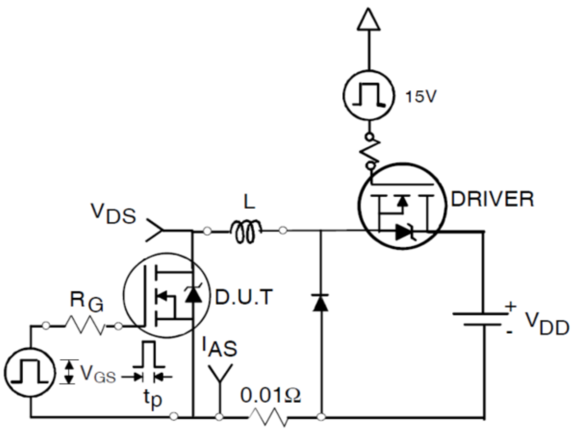


Figure 19 **Unclamped Inductive Test Circuit**

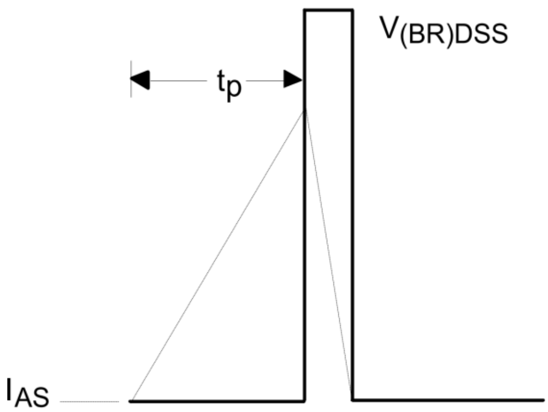


Figure 20 **Unclamped Inductive Waveform**

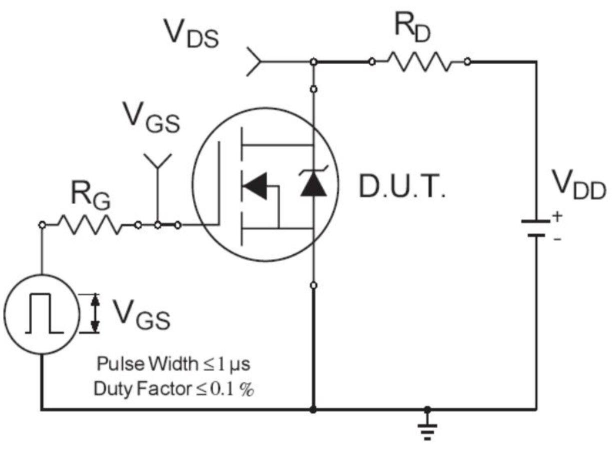


Figure 21 **Switching Time Test Circuit**

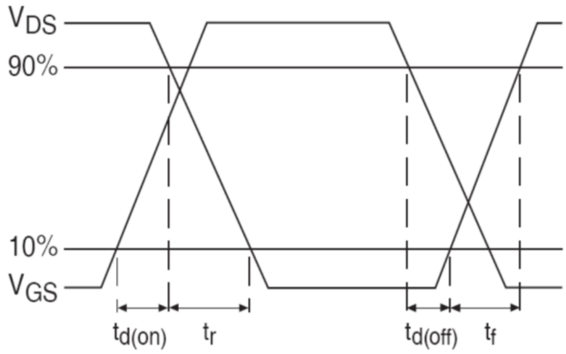
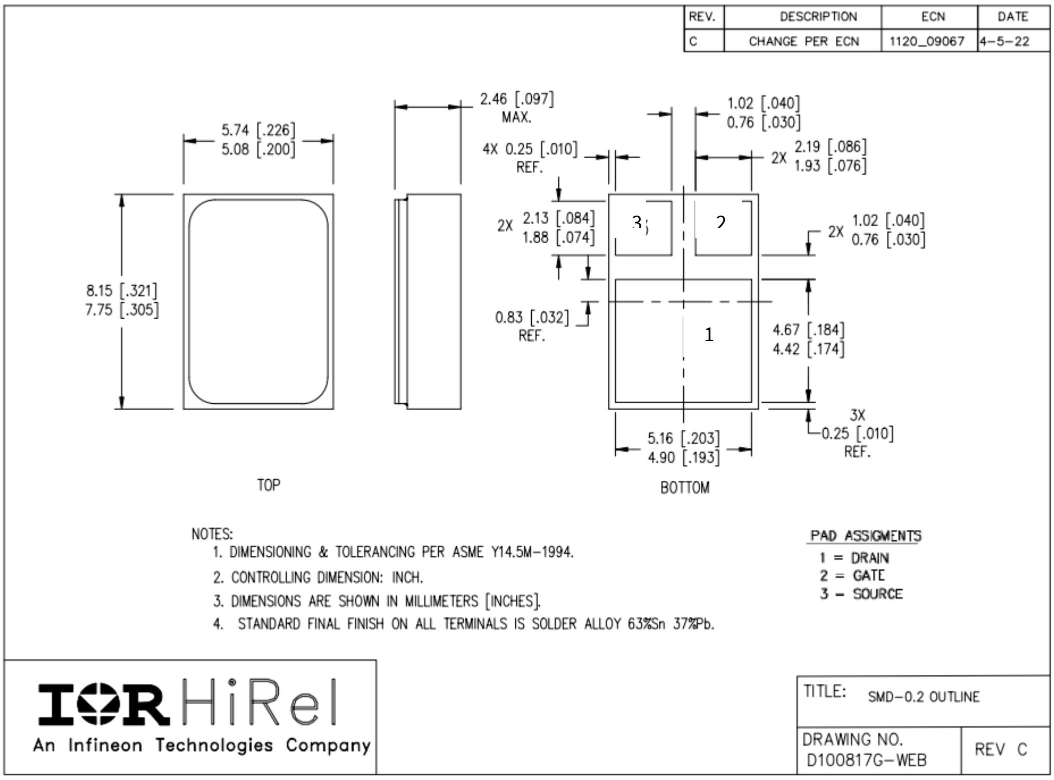


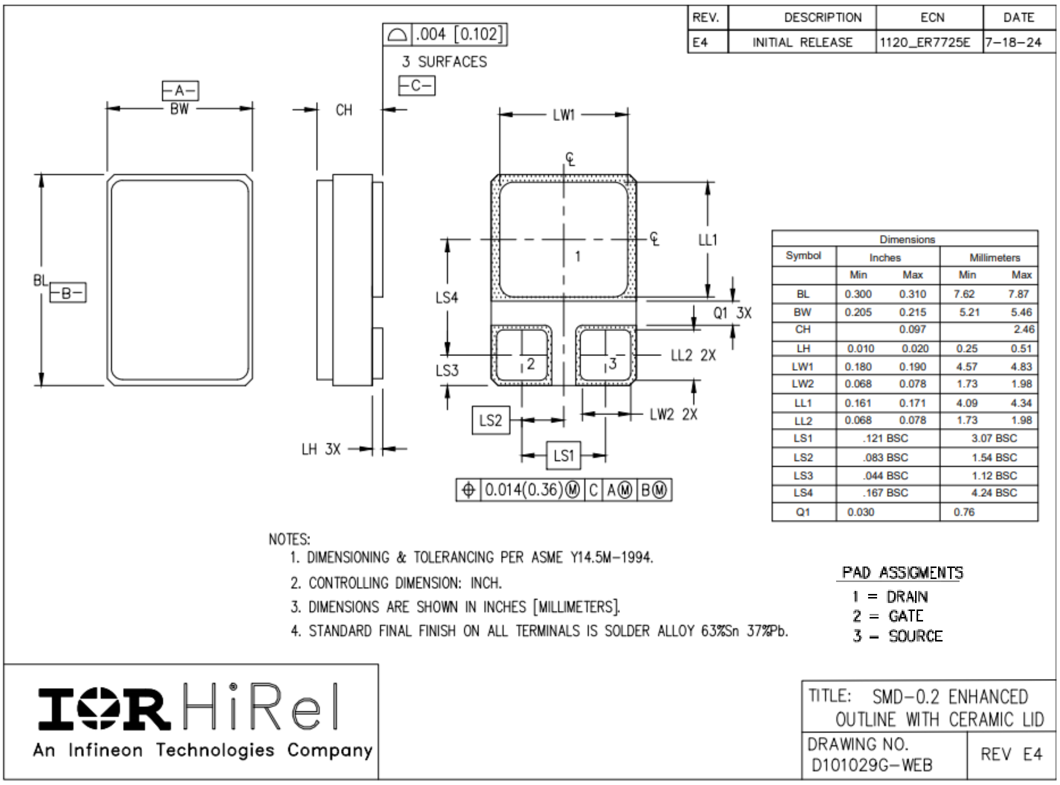
Figure 22 **Switching Time Waveforms**

5 Package Outline

Note: For the most updated package outline, please see the website: SMD-0.2 (Metal Lid)



Note: For the most updated package outline, please see the website: SMD-0.2 (Ceramic Lid)



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
BL	0.300	0.310	7.62	7.87
BW	0.205	0.215	5.21	5.46
CH		0.097		2.46
LH	0.010	0.020	0.25	0.51
LW1	0.180	0.190	4.57	4.83
LW2	0.068	0.078	1.73	1.98
LL1	0.161	0.171	4.09	4.34
LL2	0.068	0.078	1.73	1.98
LS1	.121 BSC		3.07 BSC	
LS2	.083 BSC		1.54 BSC	
LS3	.044 BSC		1.12 BSC	
LS4	.167 BSC		4.24 BSC	
Q1	0.030		0.76	

Revision history

Document version	Date of release	Description of changes
	07/08/2013	Datasheet (PD-97811)
Rev A	07/31/2018	Updated based on ECN-1120_05171
Rev B	12/20/2019	Updated based on ECN-1120_07685
Rev C	02/23/2021	Updated based on ECN-1120_08445
Rev D	04/25/2022	Updated based on ECN-1120_09025
Rev E	07/01/2024	Updated based on ECN-1120_09994
Rev F	10/16/2025	Updated based on ECN- Z8F80847339

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