

IRHLNM7S7214, IRHLNMC7S7214

PD-97852C

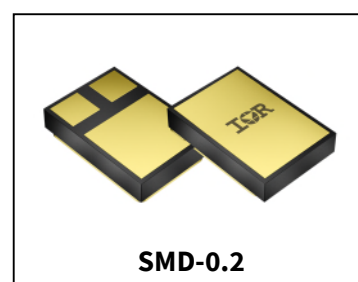
Radiation Hardened Logic Level Power MOSFET Surface Mount (SMD-0.2) 250V, 3.2A, N-channel, R7 Technology

Features

- 5V CMOS and TTL compatible
- Fast switching
- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Surface mount
- Light weight
- ESD rating: Class 1B per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}** : 250V
- **I_D** : 3.2A
- **$R_{DS(on), max}$** : 1.1 Ω
- **Q_G** : 13nC



Potential Applications

- Synchronous rectification
- Redundant power distribution
- Motor drives

Product Validation

Qualified to IR HiRel's S-level screening flow which is equivalent to MIL-PRF-19500

Description

IR HiRel R7 S-line Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Ordering Information

Table 1 **Ordering options**

Part number	Package	Screening Level	TID Level
IRHLNM7S7214	SMD-0.2	COTS	100 krad(Si)
IRHLNM7S3214	SMD-0.2	COTS	300 krad(Si)
IRHLNMS7214SCS	SMD-0.2	S-level	100 krad(Si)
IRHLNM7S3214SCS	SMD-0.2	S-level	300 krad(Si)
IRHLNMC7S7214	SMD-0.2 with ceramic lid	COTS	100 krad(Si)
IRHLNMC7S3214	SMD-0.2 with ceramic lid	COTS	300 krad(Si)
IRHLNMC7S7214SCS	SMD-0.2 with ceramic lid	S-level	100 krad(Si)
IRHLNMC7S3214SCS	SMD-0.2 with ceramic lid	S-level	300 krad(Si)

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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 4.5V, T_C = 25^{\circ}C$	Continuous Drain Current	3.2	A
$I_{D2} @ V_{GS} = 4.5V, T_C = 100^{\circ}C$	Continuous Drain Current	2.0	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	12.8	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	23.2	W
	Linear Derating Factor	0.18	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ²	17.6	mJ
I_{AR}	Avalanche Current ¹	3.2	A
E_{AR}	Repetitive Avalanche Energy ¹	2.32	mJ
dv/dt	Peak Diode Reverse Recovery ³	11	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Lead Temperature	300 (for 5s)	
	Weight	0.25 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 50V$, starting $T_J = 25^{\circ}C$, $L = 3.45mH$, Peak $I_L = 3.2A$, $V_{GS} = 10V$ ³ $I_{SD} \leq 3.2A$, $di/dt \leq 1535A/\mu s$, $V_{DD} \leq 250V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.1	Ω	$V_{GS} = 4.5V, I_{D2} = 2.0A^1$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.8	—	mV/ $^\circ\text{C}$	
G_{fs}	Forward Transconductance	3.2	—	—	S	$V_{DS} = 10V, I_{D2} = 2.0A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	15		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -10V$
Q_G	Total Gate Charge	—	—	13	nC	$I_{D1} = 3.2A$
Q_{GS}	Gate-to-Source Charge	—	—	5.8		$V_{DS} = 125V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	4.3		$V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	—	17	ns	$I_{D1} = 3.2A^{**}$ $V_{DD} = 125V$ $R_G = 7.5\Omega$ $V_{GS} = 5.0V$
t_r	Rise Time	—	—	35		
$t_{d(off)}$	Turn-Off Delay Time	—	—	45		
t_f	Fall Time	—	—	22		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	629	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	68	—		$V_{DS} = 20V$
C_{rss}	Reverse Transfer Capacitance	—	2.6	—		$f = 1.0MHz$
R_G	Gate Resistance	—	8.0	—	Ω	$f = 1.0MHz$, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.2	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	12.8	A	
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 3.2A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	250	ns	T _J = 25°C, I _F = 3.2A, V _{DD} ≤ 25V di/dt = 100A/μs
Q _{rr}	Reverse Recovery Charge	—	—	1.24	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	5.4	$^\circ\text{C}/\text{W}$

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 300 krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 10\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -10\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	$V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	1.2	Ω	$V_{GS} = 4.5\text{V}$, $I_{D2} = 2.0\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.2) ²	—	1.1	Ω	$V_{GS} = 4.5\text{V}$, $I_{D2} = 2.0\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 3.2\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 10\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 200\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHLNM7S7214, IRHLNM7S3214, IRHLNMC7S7214 and IRHLNMC7S3214

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Worst Case Single Event Effects Safe Operating Area

ION	LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)			
				V _{GS} = 0V	V _{GS} = -1V	V _{GS} = -5V	V _{GS} = -7V
Kr	35 ± 5%	580 ± 5%	70 ± 5%	250	250	250	250
Xe	60 ± 7.5%	1050 ± 5%	79 ± 5%	250	250	—	—

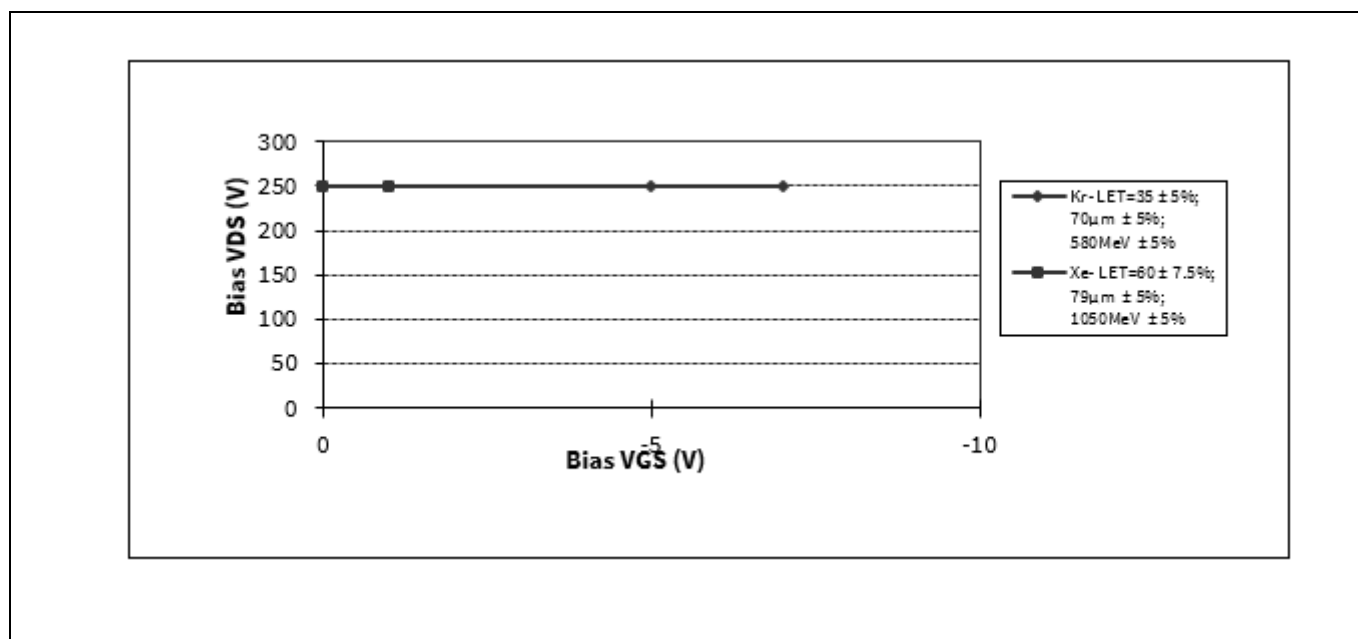


Figure 1 Worst Case Single Event Effect, Safe Operating Area

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

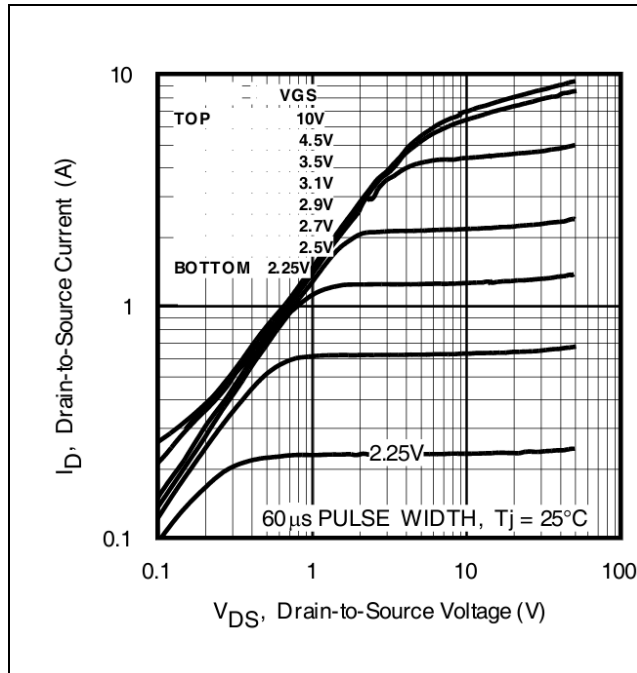


Figure 2 Typical Output Characteristics

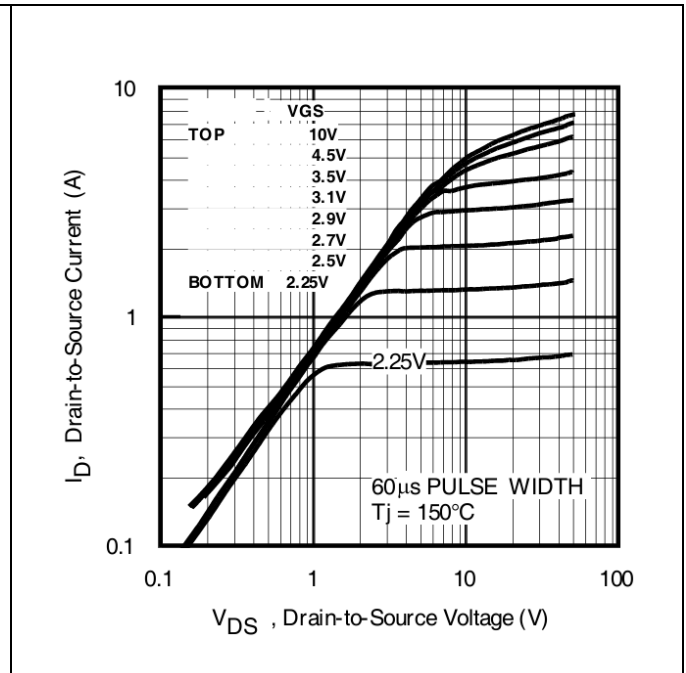


Figure 3 Typical Output Characteristics

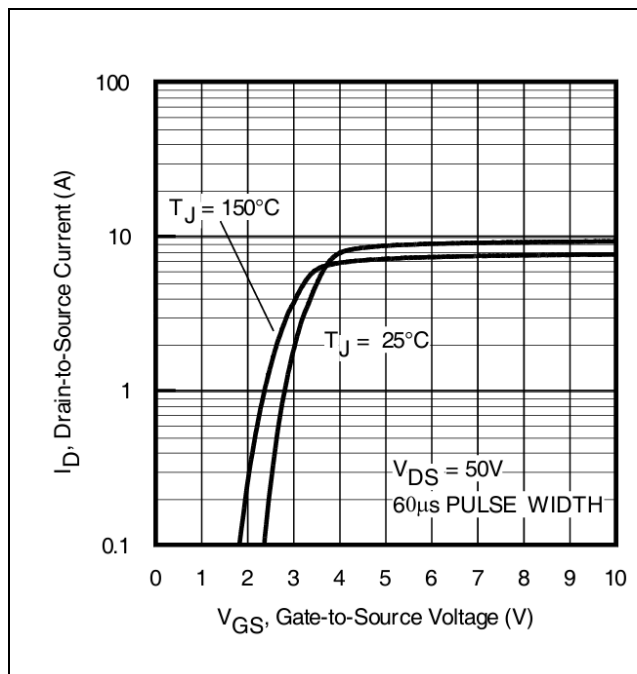


Figure 4 Typical Transfer Characteristics

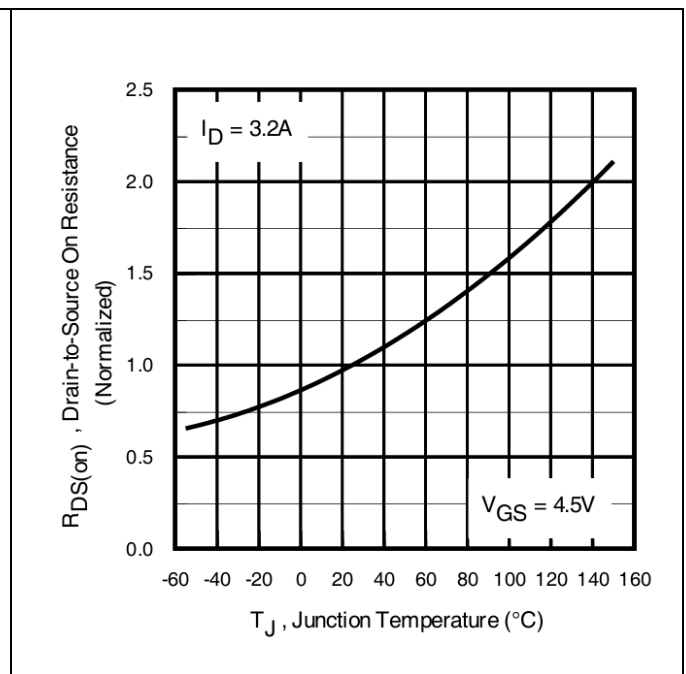


Figure 5 Normalized On-Resistance Vs. Temperature

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

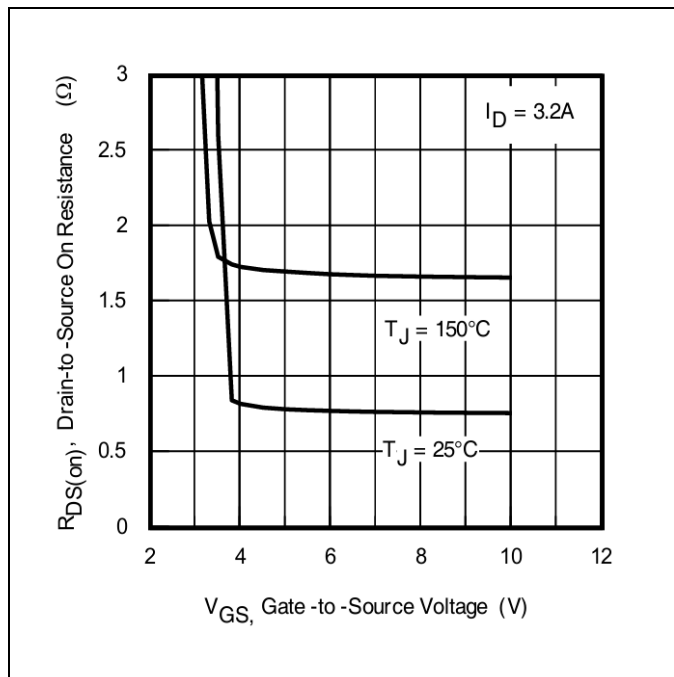


Figure 6 Typical On-Resistance Vs. Gate Voltage

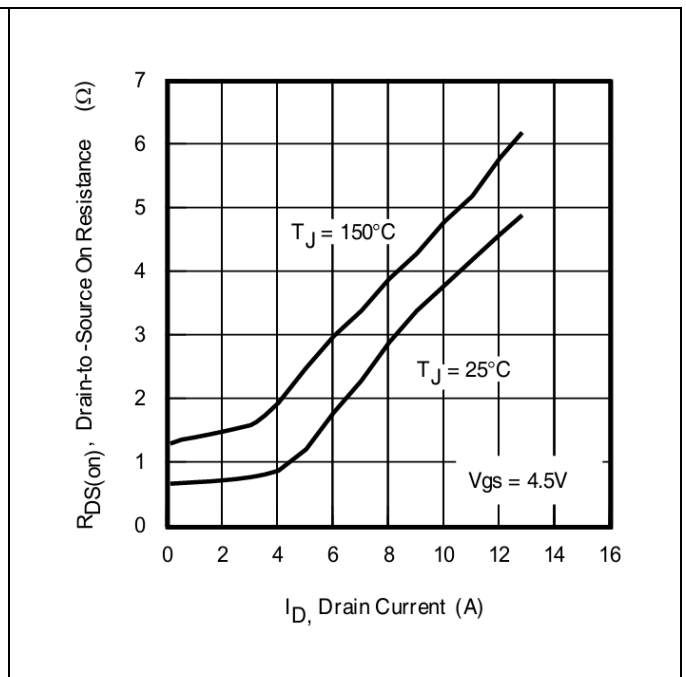


Figure 7 Typical On-Resistance Vs. Drain Current

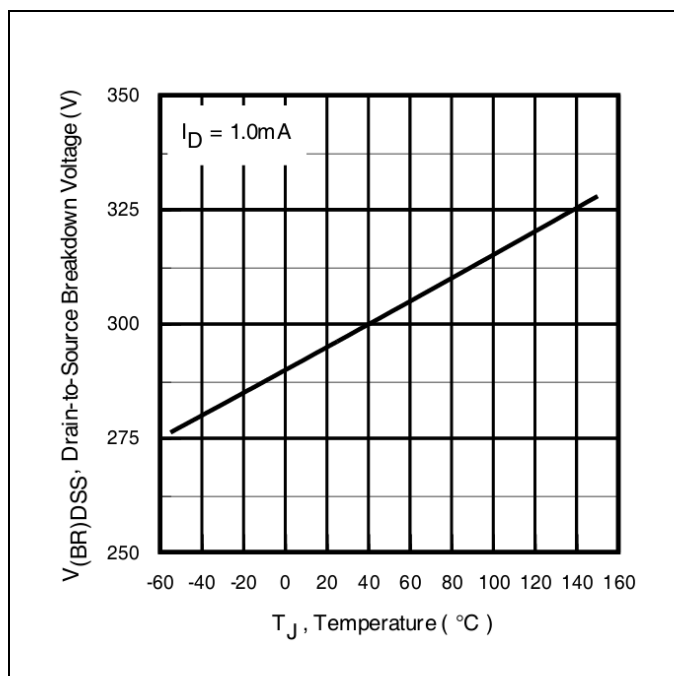


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

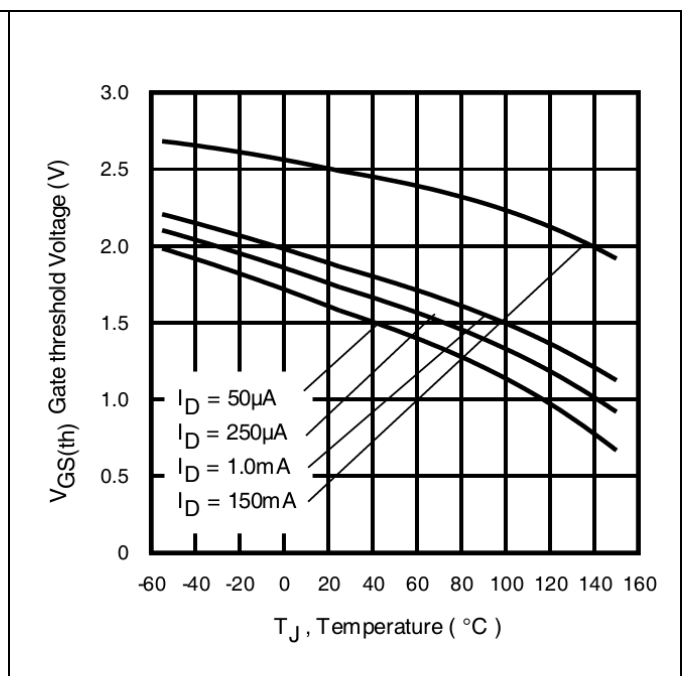


Figure 9 Typical Threshold Voltage Vs. Temperature

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

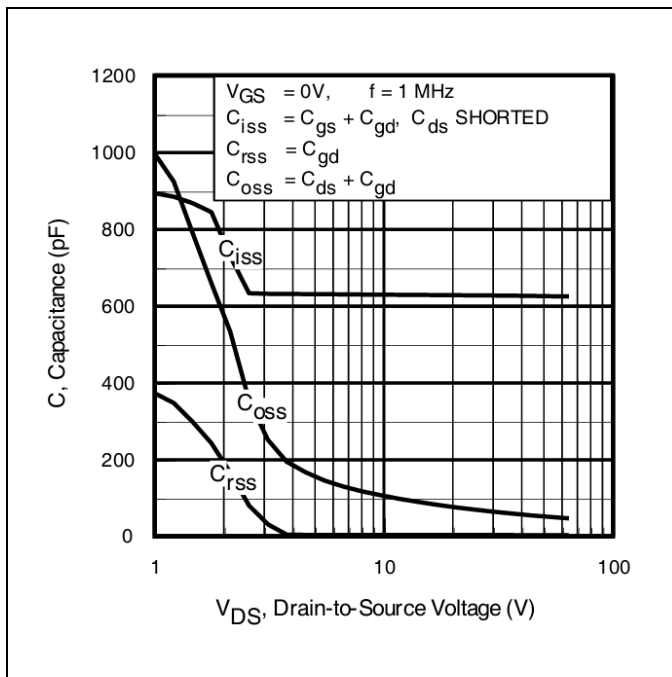


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

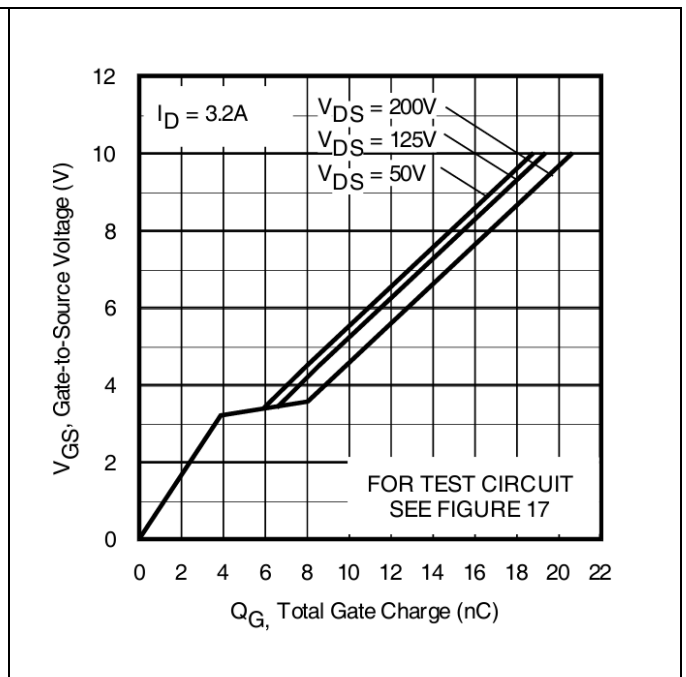


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

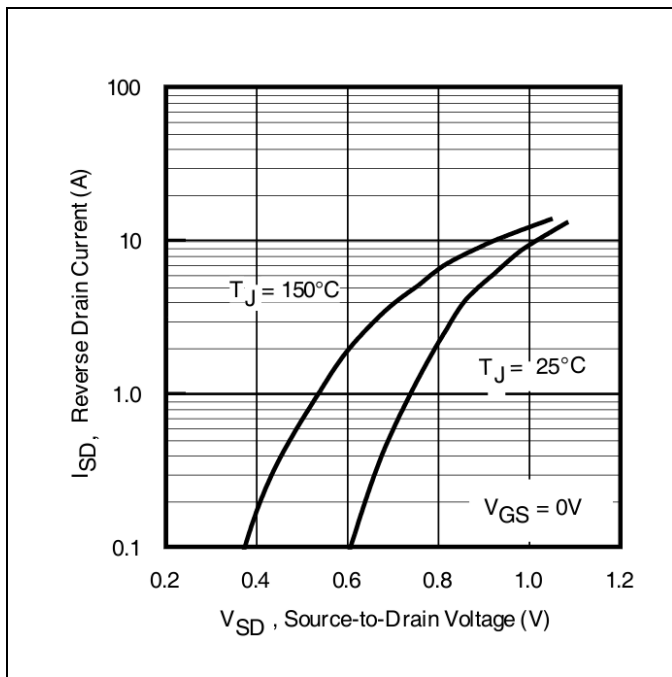


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

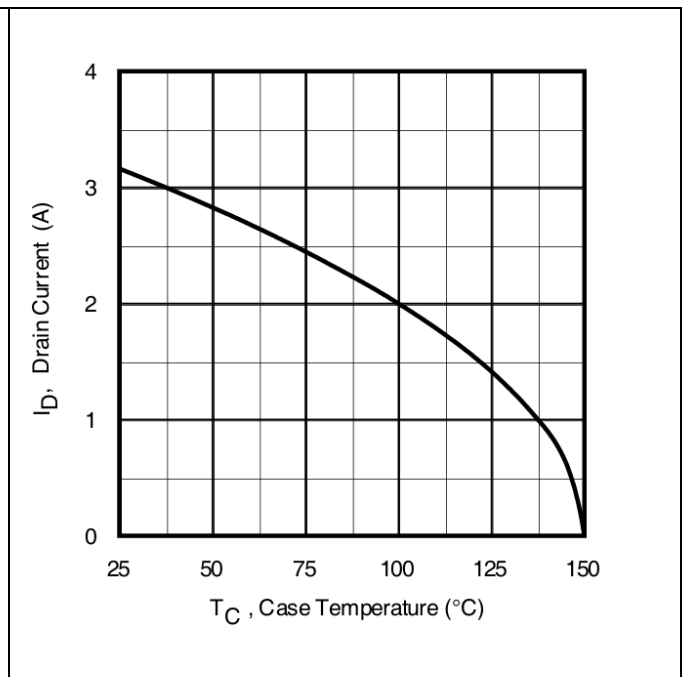


Figure 13 Maximum Drain Current Vs. Case Temperature

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

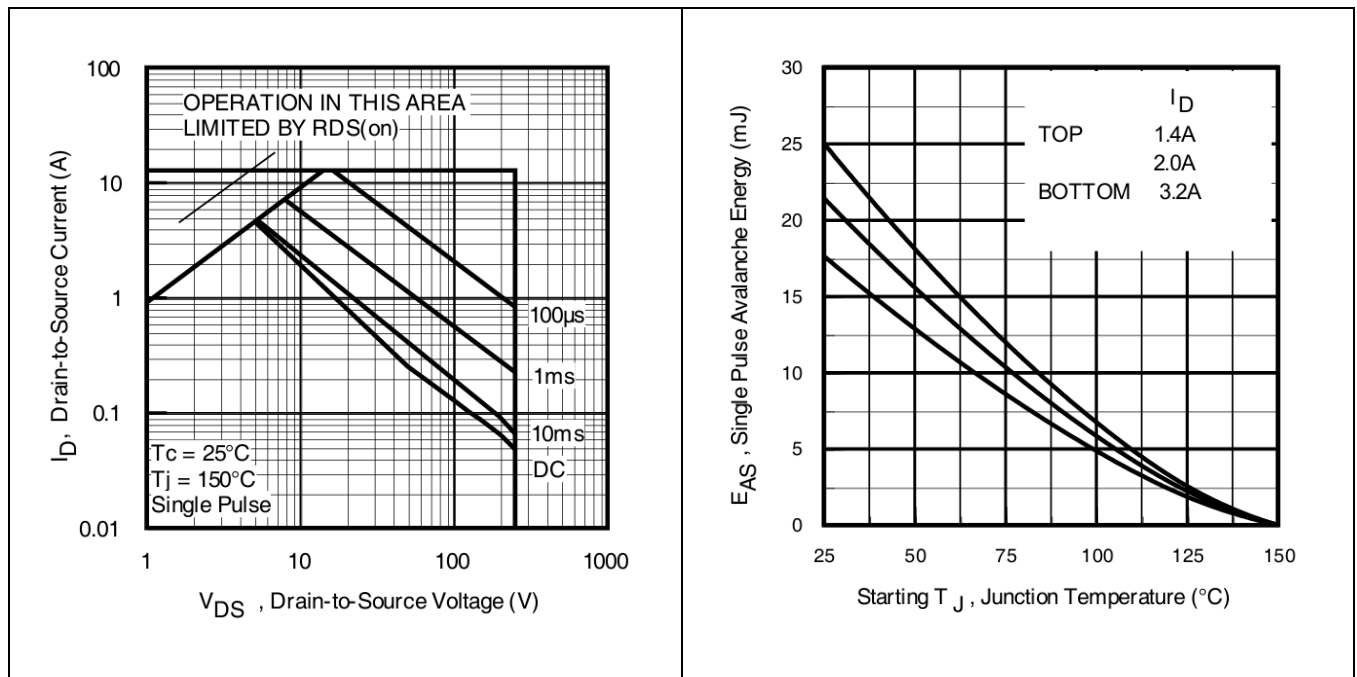


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

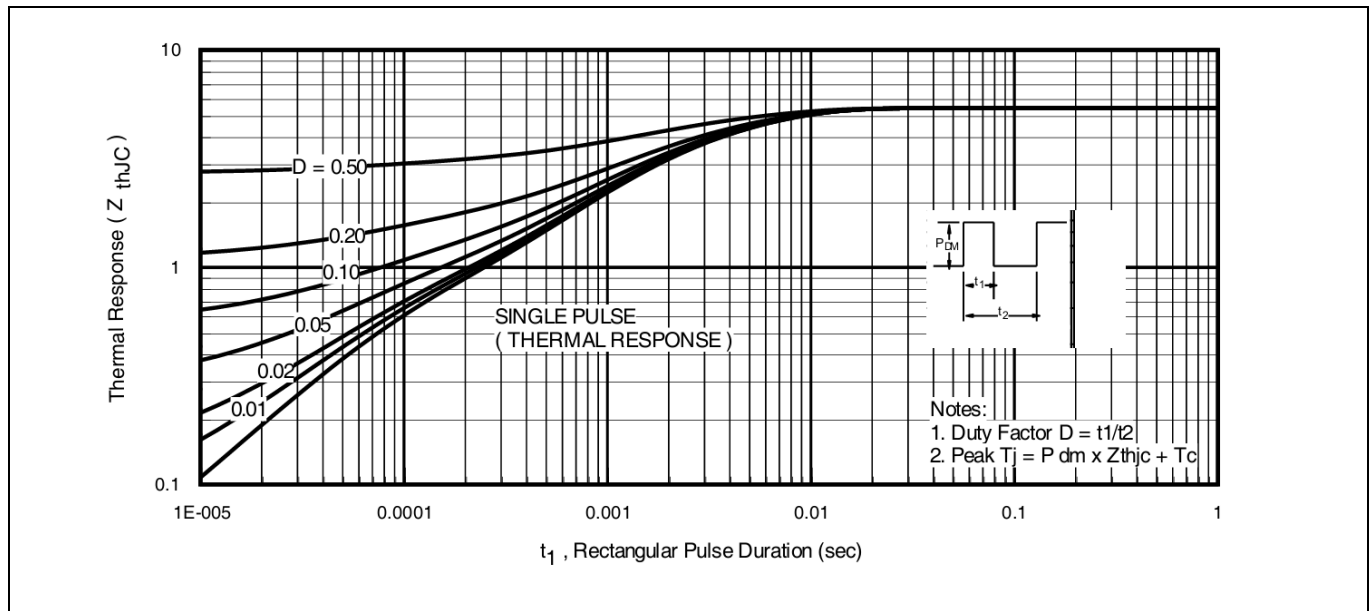


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

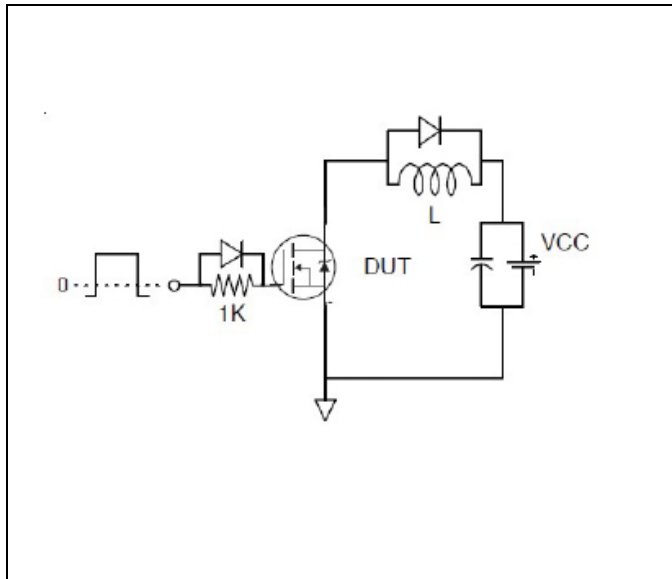


Figure 17 Gate Charge Test Circuit

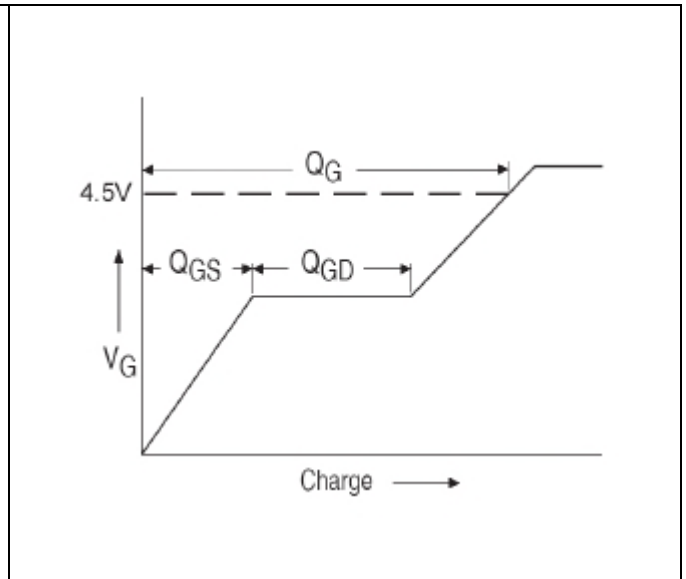


Figure 18 Gate Charge Waveform

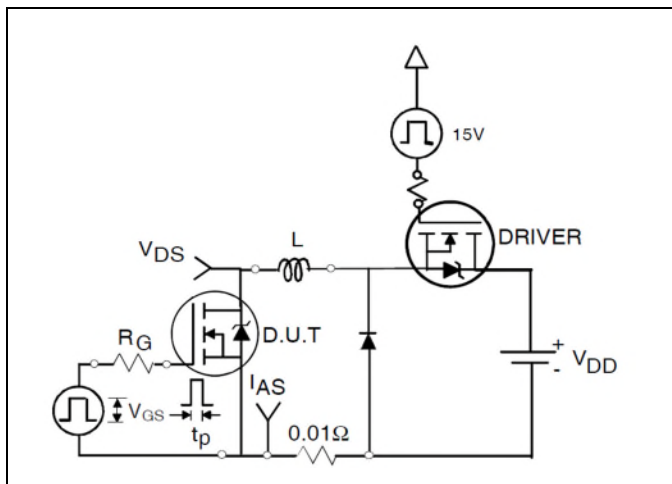


Figure 19 Unclamped Inductive Test Circuit

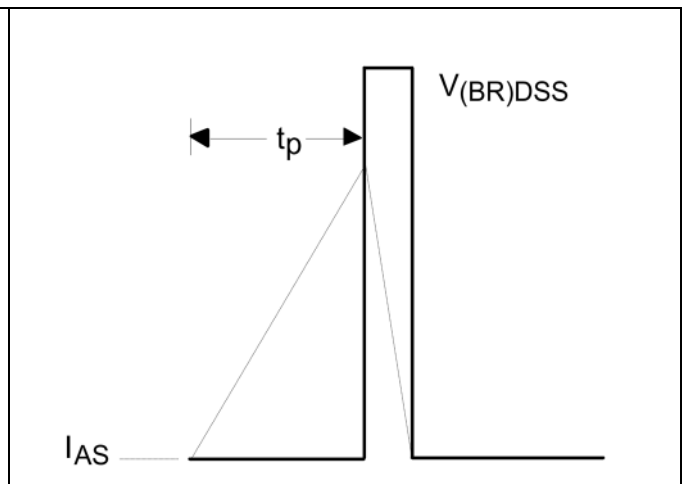


Figure 20 Unclamped Inductive Waveform

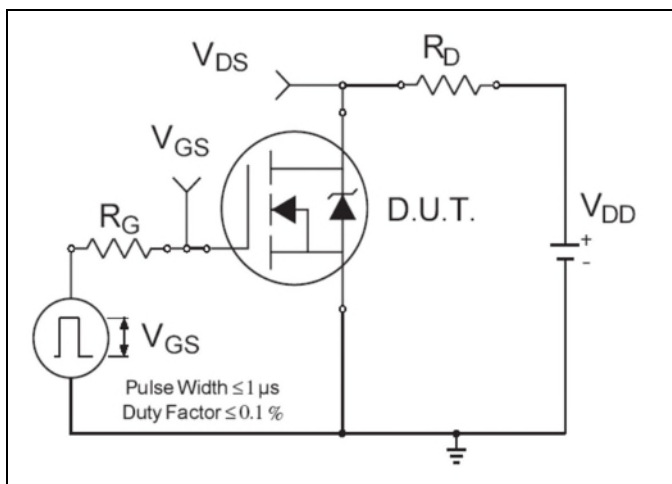


Figure 21 Switching Time Test Circuit

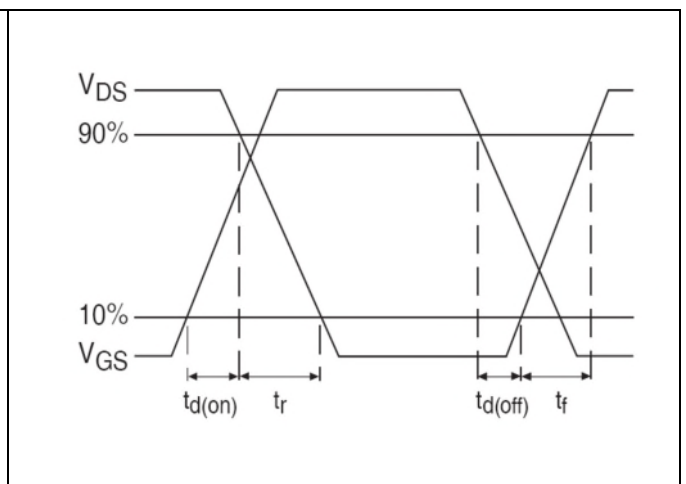


Figure 22 Switching Time Waveforms

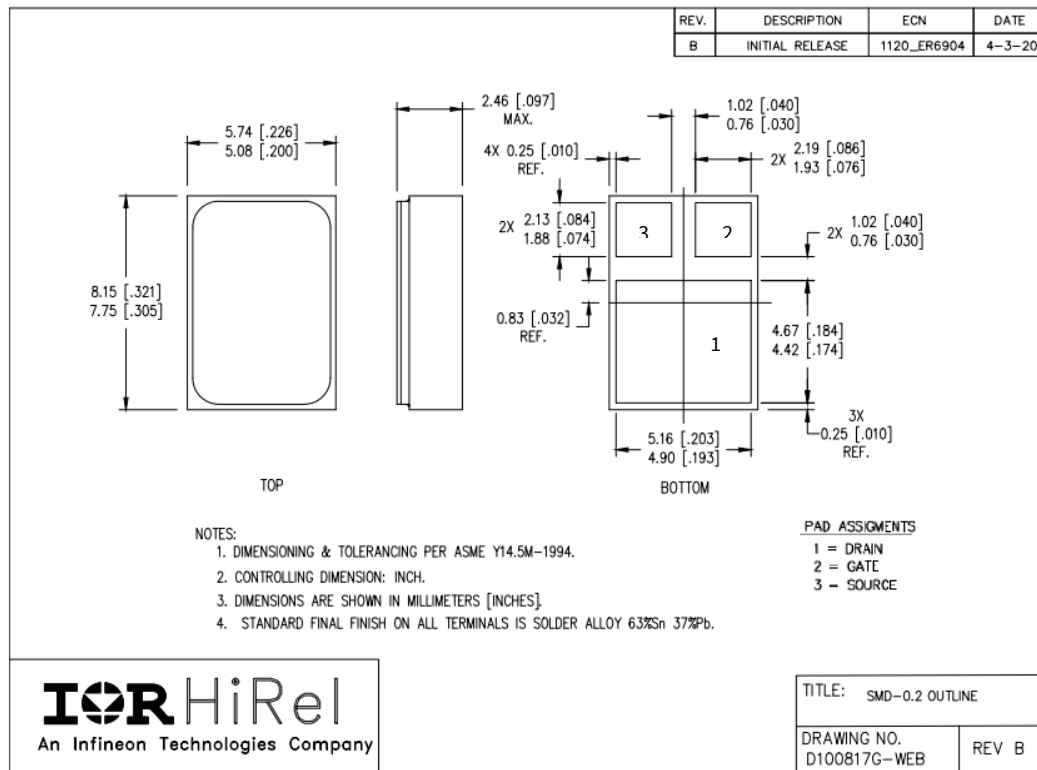
IRHLNM7S7214, IRHLNMC7S7214

Radiation Hardened Logic Level Power MOSFET Surface-Mount (SMD-0.2)

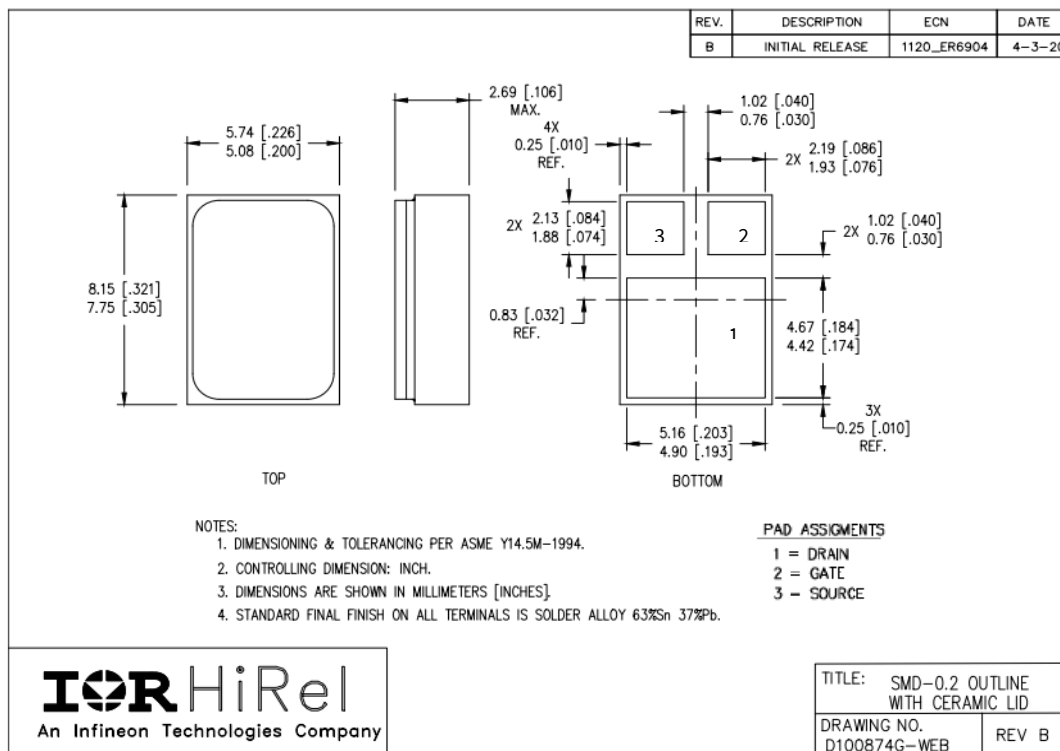
Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SMD-0.2 \(Metal Lid\)](#)



Note: For the most updated package outline, please see the website: [SMD-0.2 \(Ceramic Lid\)](#)



Revision history**Revision history**

Document version	Date of release	Description of changes
	01/11/2017	Datasheet (PD-97852)
Rev A	01/25/2019	Updated based on ECN-1120_06909
Rev B	10/23/2020	Updated based on ECN-1120_08221
Rev C	01/06/2023	Updated based on ECN-1120_09176

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