

# IRHLNKC797034 (JANSR2N7624U3CE)

PD-98015B

## Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e Ceramic Lid) 60V, -22A, P-channel, R7 Technology

### Features

- 5V CMOS and TTL Compatible
- Fast switching
- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: class 1C per MIL-STD-750, Method 1020

### Potential Applications

- DC-DC converter
- Motor drives
- Synchronous rectification

### Product Validation

Qualified according to MIL-PRF-19500 for space applications

### Description

IR HiRel R7 Logic Level Power MOSFETs provide a simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

### Ordering Information

**Table 1** Ordering options

Part number	Package	Screening Level	TID Level
IRHLNKC797034	SMD-0.5e (Ceramic Lid)	COTS	100 krad(Si)
JANSR2N7624U3CE	SMD-0.5e (Ceramic Lid)	JANS	100 krad(Si)
IRHLNKC793034	SMD-0.5e (Ceramic Lid)	COTS	300 krad(Si)
JANSF2N7624U3CE	SMD-0.5e (Ceramic Lid)	JANS	300 krad(Si)

### Product Summary

- **BV<sub>DSS</sub>**: -60V
- **I<sub>D</sub>**: -22A
- **R<sub>DS(on), max</sub>**: 72mΩ
- **Q<sub>G, max</sub>**: 36nC
- **REF**: MIL-PRF-19500/757



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**IRHLNKC797034 (JANSR2N7624U3CE)**
**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**
**Absolute Maximum Ratings**

# 1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings (Pre-Irradiation)**

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = -4.5V, T_C = 25^\circ C$	Continuous Drain Current	-22*	A
$I_{D2} @ V_{GS} = -4.5V, T_C = 100^\circ C$	Continuous Drain Current	-14.9	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current <sup>1</sup>	-88	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	57	W
	Linear Derating Factor	0.45	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 10	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>	79	mJ
$I_{AR}$	Avalanche Current <sup>1</sup>	-22	A
$E_{AR}$	Repetitive Avalanche Energy <sup>1</sup>	5.7	mJ
dv/dt	Peak Diode Reverse Recovery <sup>3</sup>	-12.3	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	

\* Current is limited by package

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup>  $V_{DD} = -25V$ , starting  $T_J = 25^\circ C$ ,  $L = 0.32mH$ , Peak  $I_L = -22A$ ,  $V_{GS} = -10V$ 
<sup>3</sup>  $I_{SD} \leq -22A$ ,  $di/dt \leq -350A/\mu s$ ,  $V_{DD} \leq -60V$ ,  $T_J \leq 150^\circ C$

**IRHLNKC797034 (JANSR2N7624U3CE)**
**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**
**Device Characteristics**
**2 Device Characteristics**
**2.1 Electrical Characteristics (Pre-Irradiation)**
**Table 3 Static and Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-60	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.055	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = -1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	72	m $\Omega$	$V_{GS} = -4.5V, I_{D2} = -14.9A^1$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	$V_{DS} \geq V_{GS}, I_D = -250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.5	—	mV/ $^\circ\text{C}$	
Gfs	Forward Transconductance	16	—	—	S	$V_{DS} = -10V, I_{D2} = -14.9A^1$
$I_{DSS}$	Zero Gate Voltage Drain Current	—	—	-1.0	$\mu A$	$V_{DS} = -48V, V_{GS} = 0V$
		—	—	-15		$V_{DS} = -48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -10V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 10V$
$Q_G$	Total Gate Charge	—	—	36	nC	$I_{D1} = -22A$
$Q_{GS}$	Gate-to-Source Charge	—	—	10		$V_{DS} = -30V$
$Q_{GD}$	Gate-to-Drain ('Miller') Charge	—	—	18		$V_{GS} = -4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	—	32	ns	$I_{D1} = -22A^{**}$
$t_r$	Rise Time	—	—	250		$V_{DD} = -30V$
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		$R_G = 7.5\Omega$
$t_f$	Fall Time	—	—	102		$V_{GS} = -5.0V$
$L_s + L_D$	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
$C_{iss}$	Input Capacitance	—	2261	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	583	—		$V_{DS} = -25V$
$C_{rss}$	Reverse Transfer Capacitance	—	91	—		$f = 1.0\text{MHz}$
$R_G$	Gate Resistance	—	—	20	$\Omega$	$f = 1.0\text{MHz}$ , open drain

\*\* Switching speed maximum limits are based on manufacturing test equipment and capability.

<sup>1</sup> Pulse width  $\leq 300\mu s$ ; Duty Cycle  $\leq 2\%$

**IRHLNKC797034 (JANSR2N7624U3CE)**
**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**
**Device Characteristics**
**2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)**
**Table 4 Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-22	A	
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>1</sup>	—	—	-88	A	
$V_{SD}$	Diode Forward Voltage	—	—	-5.0	V	$T_J = 25^\circ\text{C}$ , $I_S = -22\text{A}$ , $V_{GS} = 0\text{V}$ <sup>2</sup>
$t_{rr}$	Reverse Recovery Time	—	—	110	ns	$T_J = 25^\circ\text{C}$ , $I_F = -22\text{A}$ , $V_{DD} \leq -50\text{V}$
$Q_{rr}$	Reverse Recovery Charge	—	88	—	nC	$di/dt = -100\text{A}/\mu\text{s}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

**2.3 Thermal Characteristics**
**Table 5 Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	2.2	$^\circ\text{C}/\text{W}$

**2.4 Radiation Characteristics**

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**2.4.1 Electrical Characteristics - Post Total Dose Irradiation**
**Table 6 Electrical Characteristics @  $T_J = 25^\circ\text{C}$ , Post Total Dose Irradiation<sup>3, 4</sup>**

Symbol	Parameter	Up to 300krads (Si) <sup>5</sup>		Unit	Test Conditions
		Min.	Max.		
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-60	—	V	$V_{GS} = 0\text{V}$ , $I_D = -250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	$V_{DS} \geq V_{GS}$ , $I_D = -250\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	-100	nA	$V_{GS} = -10\text{V}$
	Gate-to-Source Leakage Reverse	—	100		$V_{GS} = 10\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current	—	-1.0	$\mu\text{A}$	$V_{DS} = -48\text{V}$ , $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) <sup>2</sup>	—	76	m $\Omega$	$V_{GS} = -4.5\text{V}$ , $I_D = -14.9\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.5e) <sup>2</sup>	—	72	m $\Omega$	$V_{GS} = -4.5\text{V}$ , $I_D = -14.9\text{A}$
$V_{SD}$	Diode Forward Voltage	—	-5.0	V	$V_{GS} = 0\text{V}$ , $I_S = -22\text{A}$

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup> Pulse width  $\leq 300\mu\text{s}$ ; Duty Cycle  $\leq 2\%$ 
<sup>3</sup> Total Dose Irradiation with  $V_{GS}$  Bias.  $V_{GS} = -10\text{V}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>4</sup> Total Dose Irradiation with  $V_{DS}$  Bias.  $V_{DS} = -48\text{V}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>5</sup> Part numbers IRHLNKC797034 (JANSR2N7624U3CE), and IRHLNKC793034 (JANSF2N7624U3CE)

Device Characteristics

2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm <sup>2</sup> /mg)	Energy (MeV)	Range (μm)	V <sub>DS</sub> (V)					
			V <sub>GS</sub> = 0V	V <sub>GS</sub> = 2V	V <sub>GS</sub> = 4V	V <sub>GS</sub> = 5V	V <sub>GS</sub> = 6V	V <sub>GS</sub> = 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-40
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	—
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	—	—

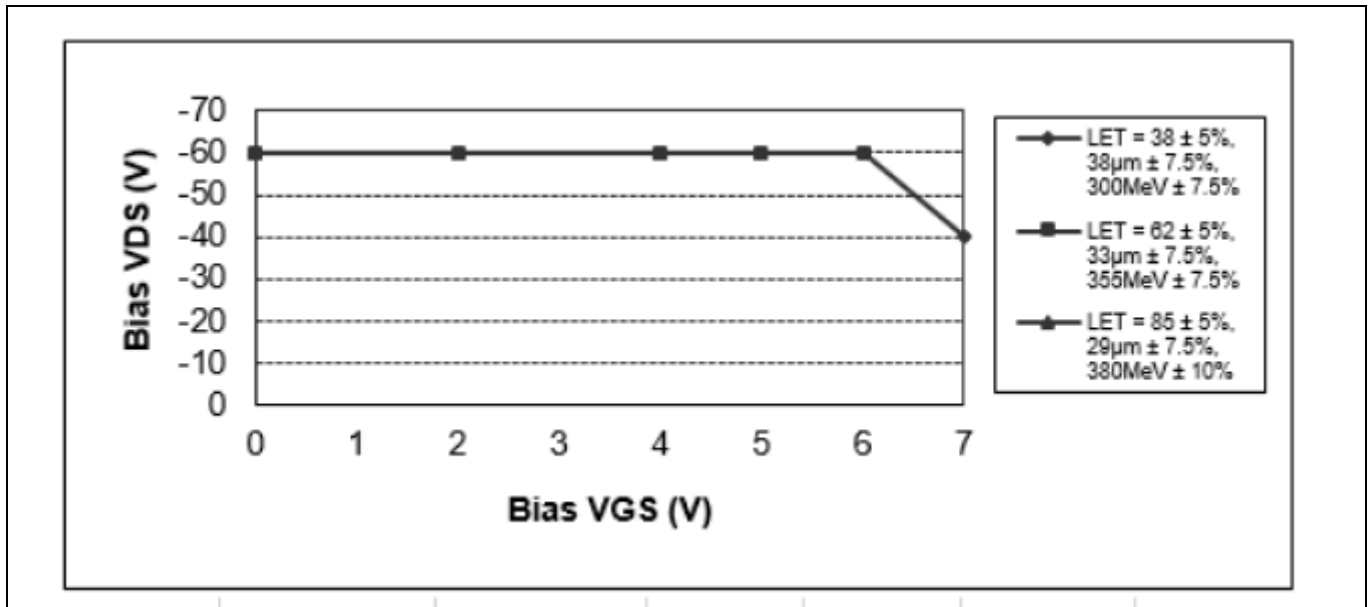


Figure 1 Typical Single Event Effect, Safe Operating Area

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Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)

Electrical Characteristics Curves (Pre-irradiation)

### 3 Electrical Characteristics Curves (Pre-irradiation)

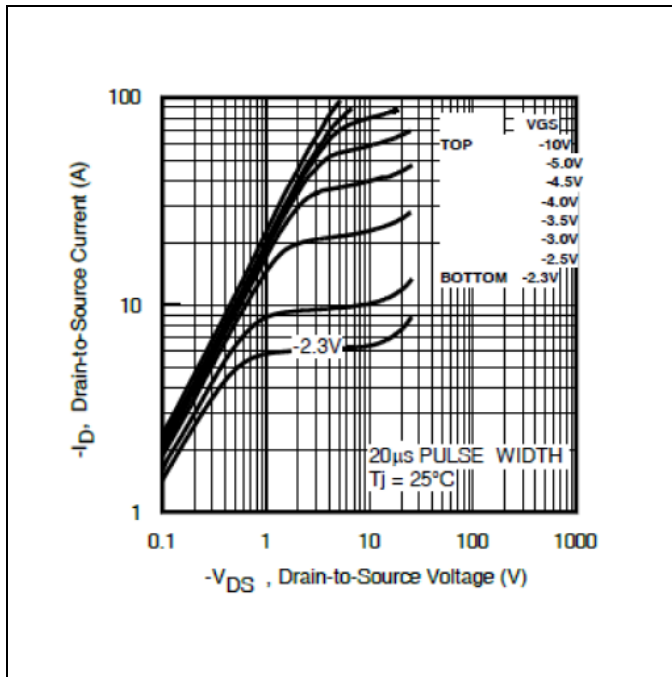


Figure 2 Typical Output Characteristics

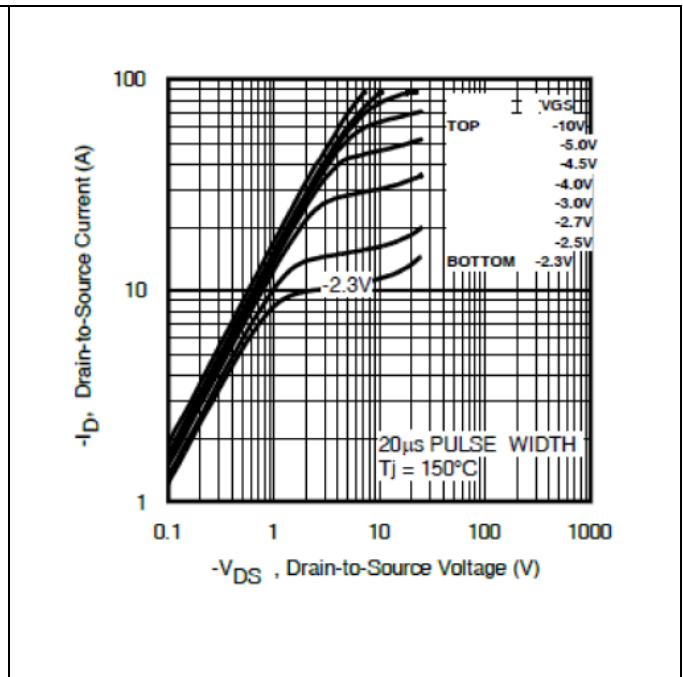


Figure 3 Typical Output Characteristics

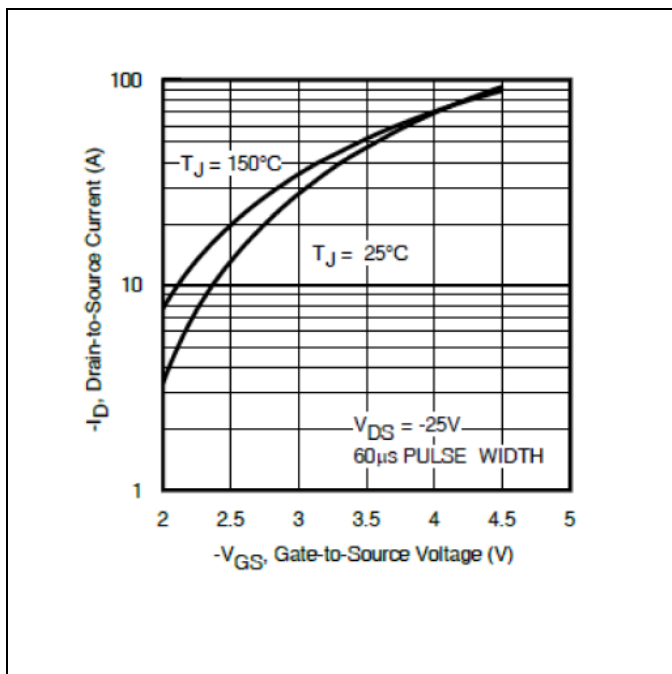


Figure 4 Typical Transfer Characteristics

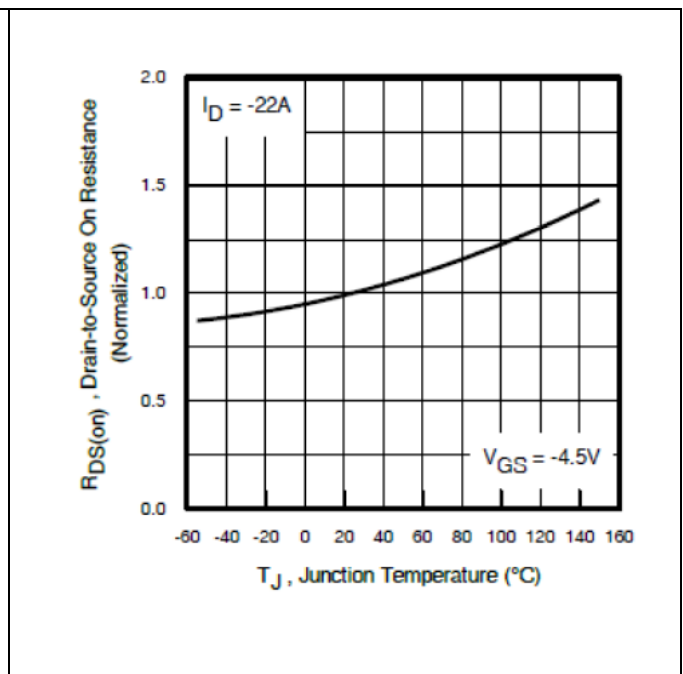
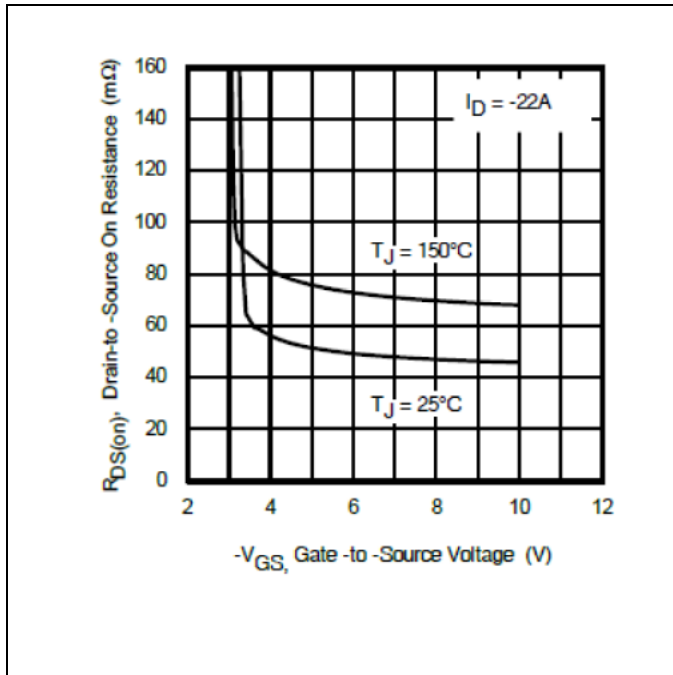


Figure 5 Normalized On-Resistance Vs. Temperature

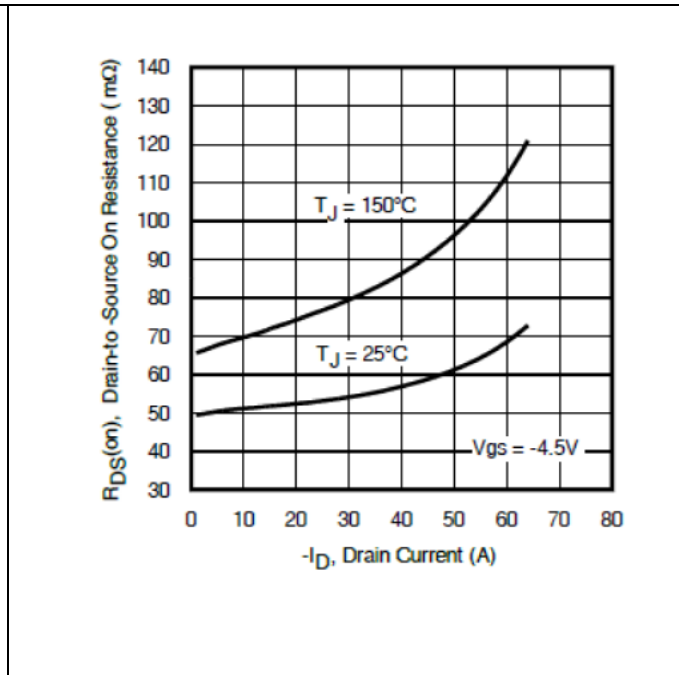
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**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**

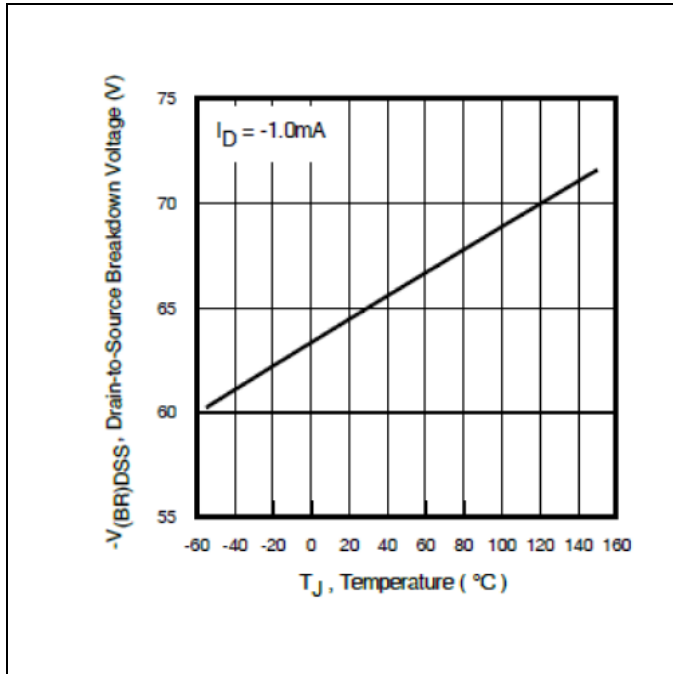
**Electrical Characteristics Curves (Pre-irradiation)**



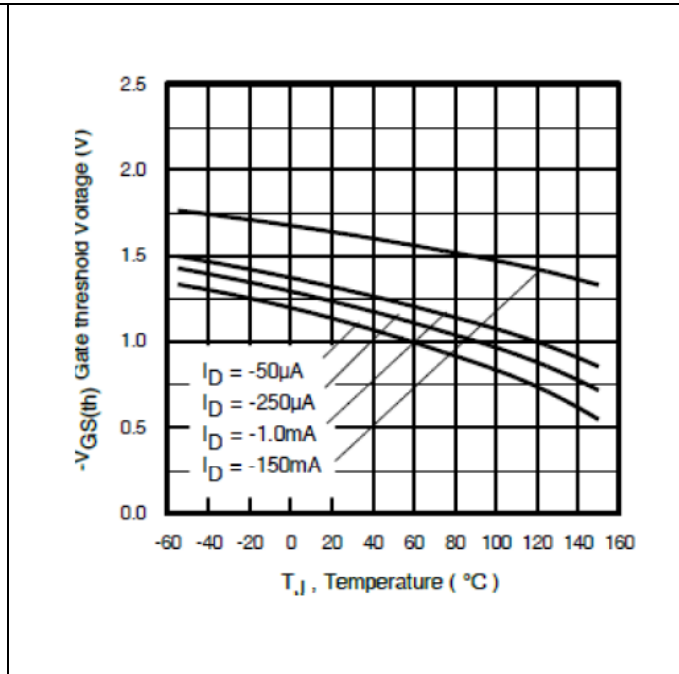
**Figure 6 Typical On-Resistance Vs. Gate Voltage**



**Figure 7 Typical On-Resistance Vs. Drain Current**



**Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

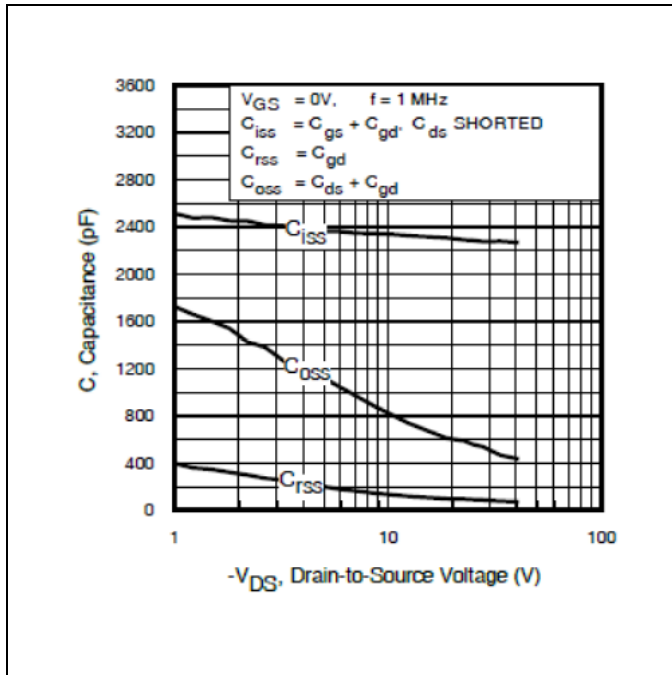


**Figure 9 Typical Threshold Voltage Vs. Temperature**

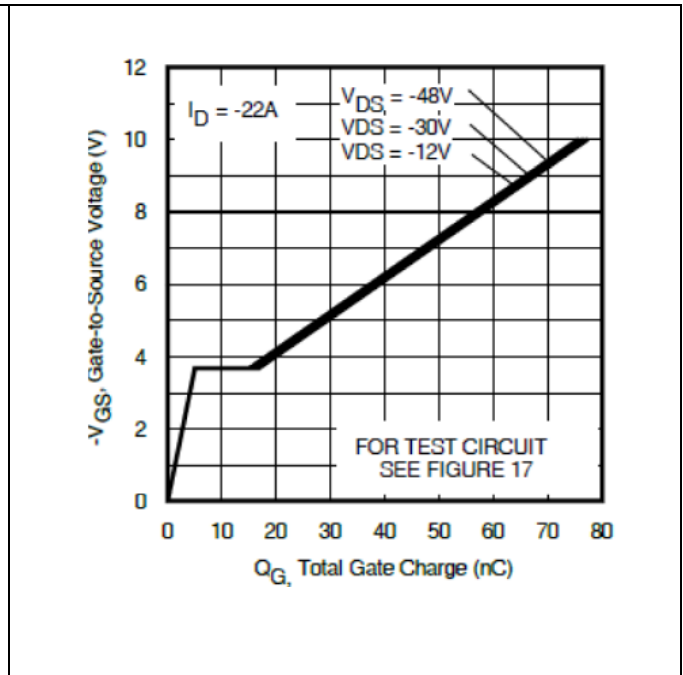
**IRHLNKC797034 (JANSR2N7624U3CE)**

**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**

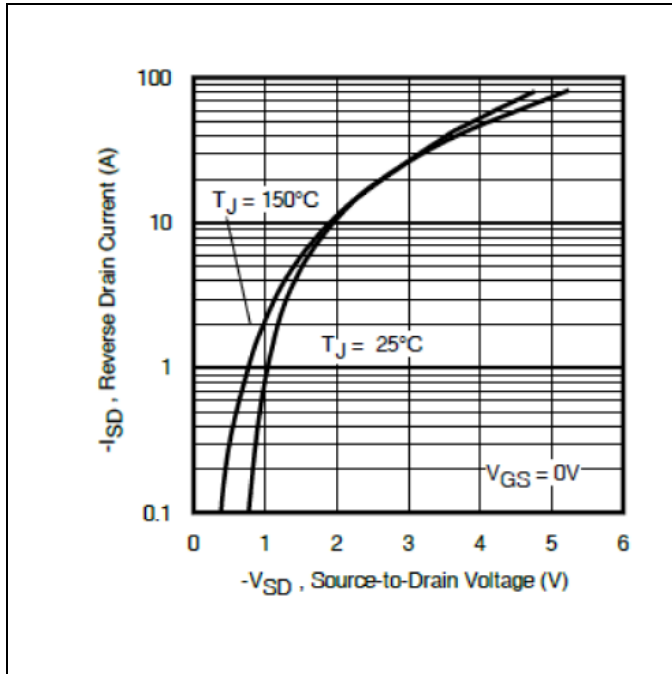
**Electrical Characteristics Curves (Pre-irradiation)**



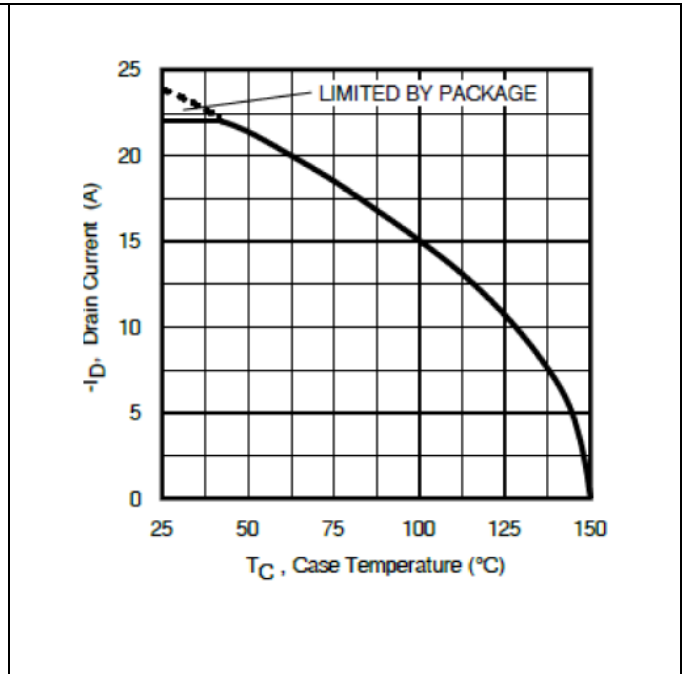
**Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage**



**Figure 11 Typical Gate Charge Vs. Gate-to-Source Voltage**



**Figure 12 Typical Source-Drain Vs. Diode Forward Voltage**

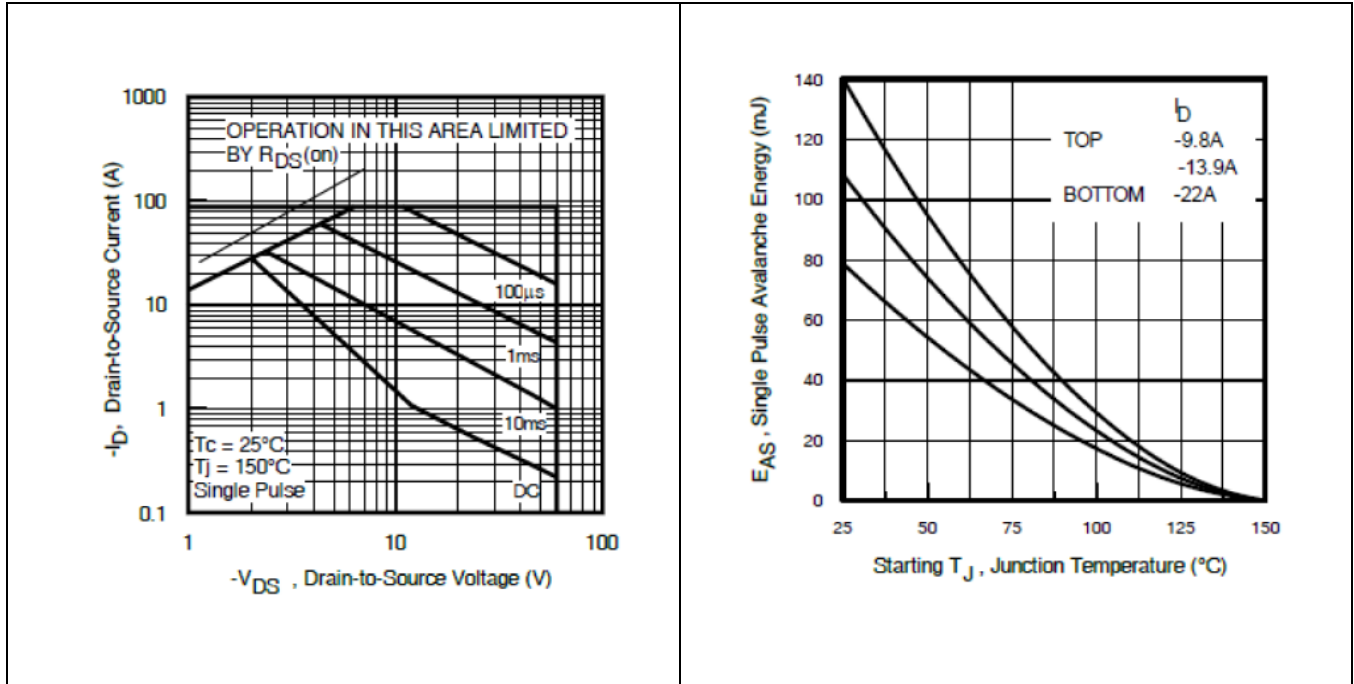


**Figure 13 Maximum Drain Current Vs. Case Temperature**

**IRHLNKC797034 (JANSR2N7624U3CE)**

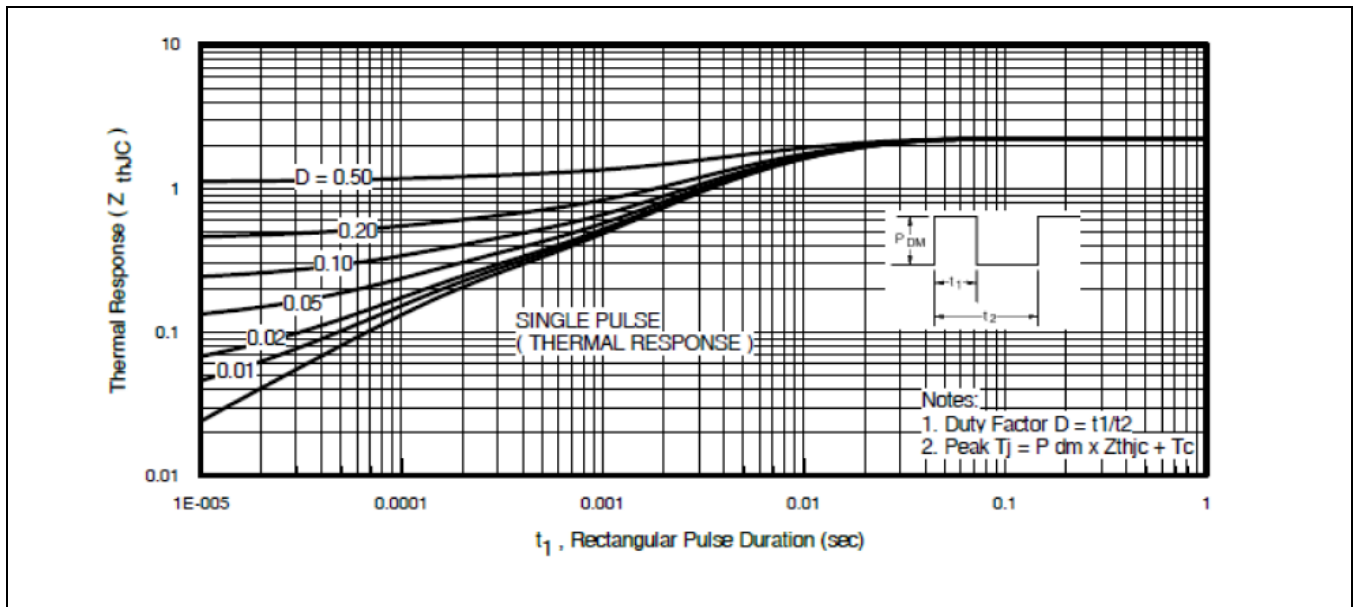
**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**

**Electrical Characteristics Curves (Pre-irradiation)**



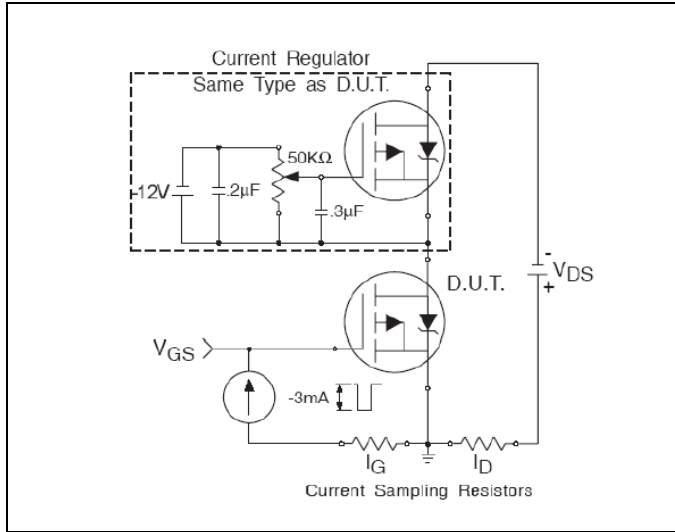
**Figure 14 Maximum Safe Operating Area**

**Figure 15 Maximum Avalanche Energy Vs. Junction Temperature**

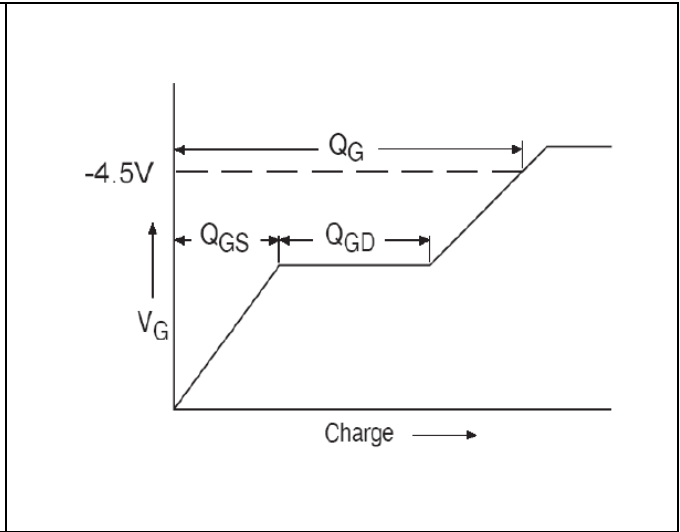


**Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case**

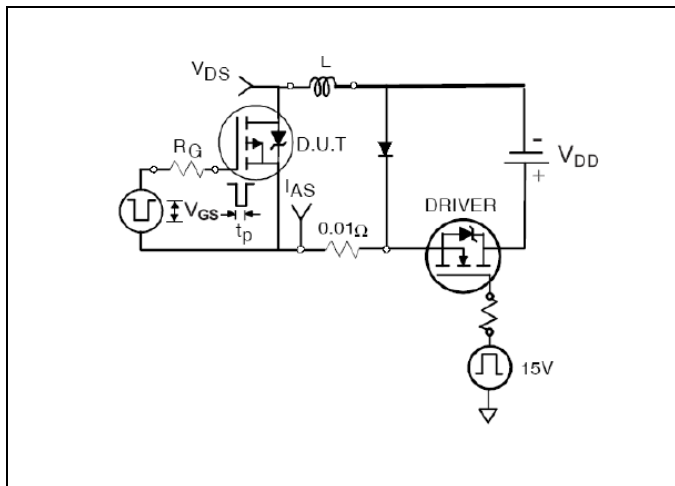
**4 Test Circuits (Pre-irradiation)**



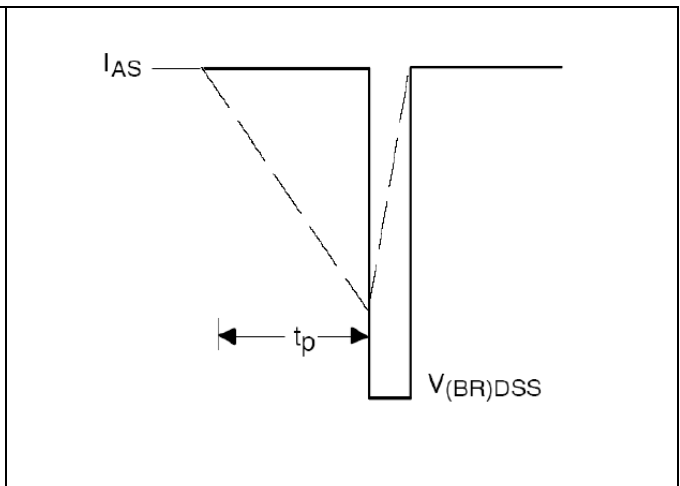
**Figure 17 Gate Charge Test Circuit**



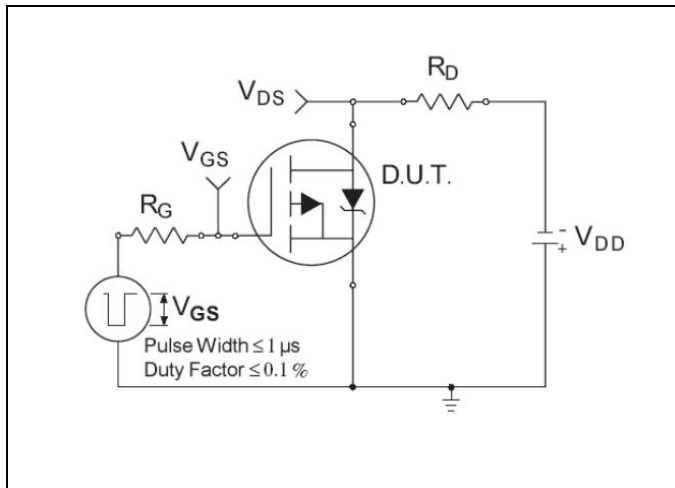
**Figure 18 Gate Charge Waveform**



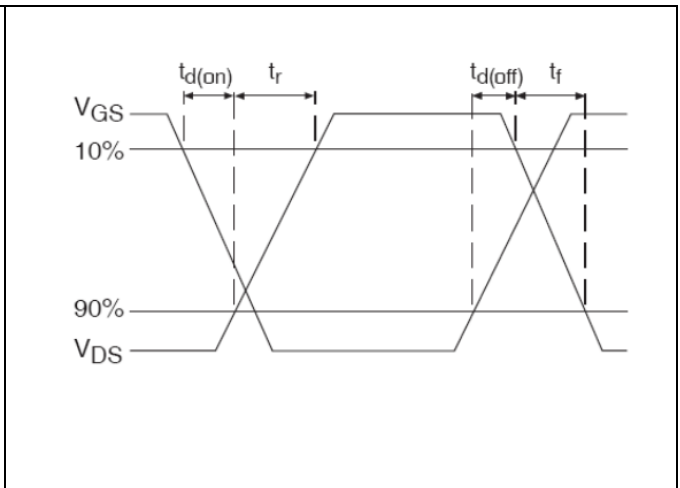
**Figure 19 Unclamped Inductive Test Circuit**



**Figure 20 Unclamped Inductive Waveform**



**Figure 21 Switching Time Test Circuit**



**Figure 22 Switching Time Waveforms**

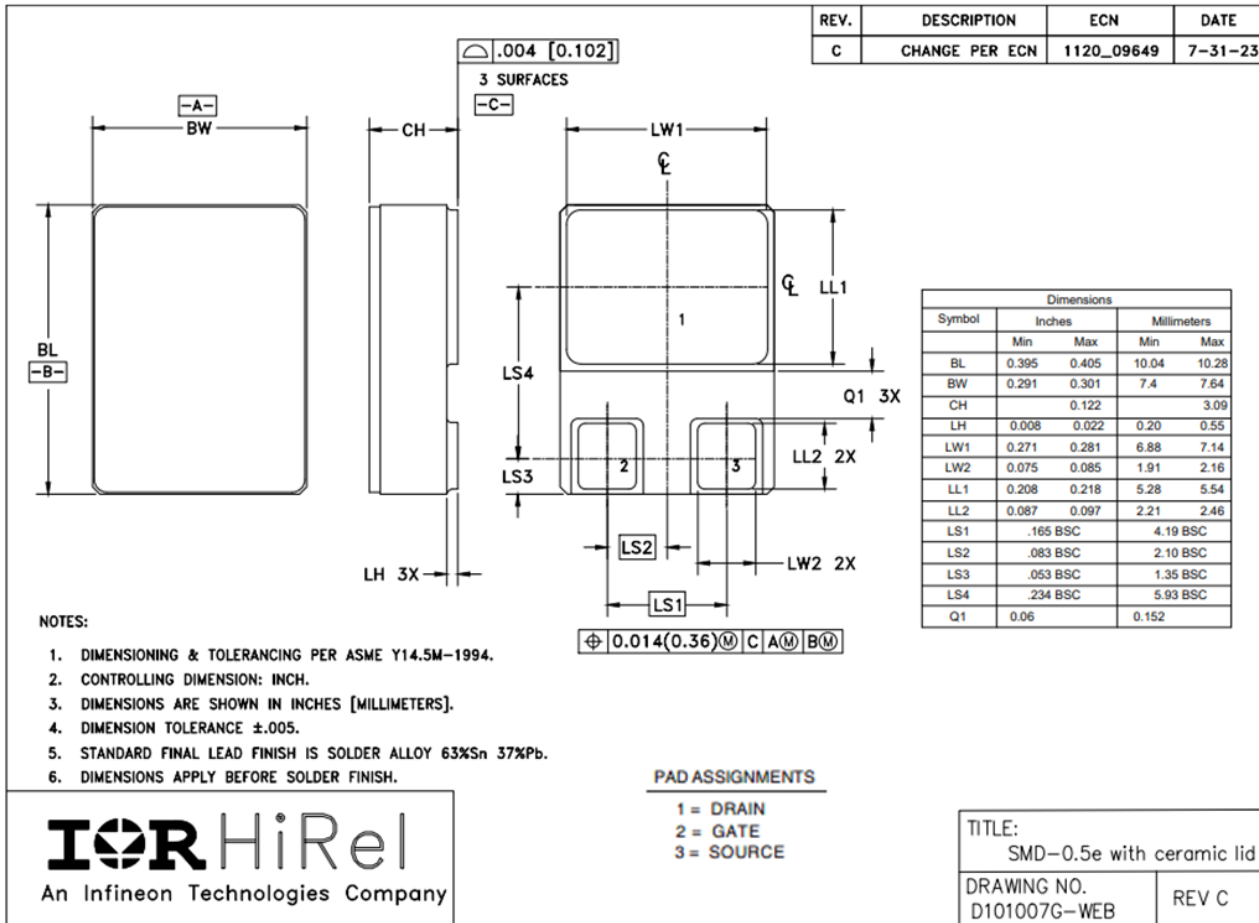
**IRHLNKC797034 (JANSR2N7624U3CE)**

**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**

**Package Outline**

**5 Package Outline**

Note: For the most updated package outline, please see the website: [SMD-0.5e with Ceramic Lid](#)



**IRHLNKC797034 (JANSR2N7624U3CE)**

**Radiation Hardened Logic level Power MOSFET Surface Mount (SMD-0.5e)**

**Revision history**

**Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
	05/02/2024	Preliminary datasheet with PPD number (PPD-98015)
Rev A	05/22/2024	Final datasheet with PD number
Rev B	03/03/2026	Updated based on ECN- Z8F80892464

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