

IRHLF770Z4

PD-94695J

Radiation Hardened Logic Level Power MOSFET Thru-Hole TO-205AF (TO-39) 60V, 1.6A, N-channel, R7 Technology

Features

- 5V CMOS and TTL compatible
- Fast switching
- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Light weight
- Hermetically sealed
- ESD rating: Class 0B per MIL-STD-750, Method 1020

Product Summary

- BV_{DSS} : 60V
- I_D : 1.6A
- $R_{DS(on),max}$: 0.65Ω
- $Q_{G,max}$: 2.6nC

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHLF770Z4	TO-39	COTS	100 krad(Si)
IRHLF770Z4SCS	TO-39	S-Level	100 krad(Si)
IRHLF730Z4	TO-39	COTS	300 krad(Si)
IRHLF730Z4SCS	TO-39	S-Level	300 krad(Si)

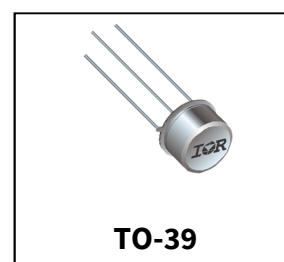


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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 4.5V, T_C = 25^{\circ}C$	Continuous Drain Current	1.6*	A
$I_{D2} @ V_{GS} = 4.5V, T_C = 100^{\circ}C$	Continuous Drain Current	1.0*	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	6.4	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	5.0	W
	Linear Derating Factor	0.04	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ²	6.9	mJ
I_{AR}	Avalanche Current ¹	1.6	A
E_{AR}	Repetitive Avalanche Energy ¹	0.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	3.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	0.98 (Typical)	

* Derated to match the complementary P-Channel Logic Level Power Mosfet - IRHLF7970Z4

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, $L = 5.4mH$, Peak $I_L = 1.6A$, $V_{GS} = 10V$ ³ $I_{SD} \leq 1.6A$, $di/dt \leq 92A/\mu s$, $V_{DD} \leq 60V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.08	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.65	Ω	$V_{GS} = 4.5V$, $I_{D2} = 1.0A$ ¹
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-3.5	—		
G_{fs}	Forward Transconductance	1.1	—	—	S	$V_{DS} = 10V$, $I_{D2} = 1.0A$ ¹
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	$V_{DS} = 48V$, $V_{GS} = 0V$
		—	—	10		$V_{DS} = 48V$, $V_{GS} = 0V$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -10V$
Q_G	Total Gate Charge	—	—	2.6	nC	$I_{D1} = 1.6A$ $V_{DS} = 30V$ $V_{GS} = 4.5V$
Q_{GS}	Gate-to-Source Charge	—	—	0.8		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.5		
$t_{d(on)}$	Turn-On Delay Time	—	—	6.5	ns	$I_{D1} = 1.6A$ ** $V_{DD} = 30V$ $R_G = 24\Omega$ $V_{GS} = 4.5V$
t_r	Rise Time	—	—	14		
$t_{d(off)}$	Turn-Off Delay Time	—	—	30		
t_f	Fall Time	—	—	13		
$L_s + L_D$	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C_{iss}	Input Capacitance	—	152	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	39	—		
C_{rss}	Reverse Transfer Capacitance	—	1.6	—		
R_G	Gate Resistance	—	9.5	—	Ω	$f = 1.0\text{MHz}$, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.6	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	6.4	A	
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 1.6A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	78	ns	T _J = 25°C, I _F = 1.6A, V _{DD} ≤ 25V di/dt = 100A/μs ²
Q _{rr}	Reverse Recovery Charge	—	—	150	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	25	$^\circ\text{C}/\text{W}$

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 300 krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 10\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -10\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	$V_{DS} = 48\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	0.65	Ω	$V_{GS} = 4.5\text{V}$, $I_{D2} = 1.0\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-39) ²	—	0.65	Ω	$V_{GS} = 4.5\text{V}$, $I_{D2} = 1.0\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 1.6\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 10\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 48\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHLF770Z4 and IRHLF730Z4

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Radiation Hardened Logic Level Power MOSFET Thru-Hole (TO-39)
Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)					
			V _{GS} = 0V	V _{GS} = -2V	V _{GS} = -3V	V _{GS} = -4V	V _{GS} = -5V	V _{GS} = -6V
38.1	358	43.9	60	60	60	60	60	60
60.9	659	54	60	60	60	60	60	—
90.7	1375	75.4	60	60	—	—	—	—

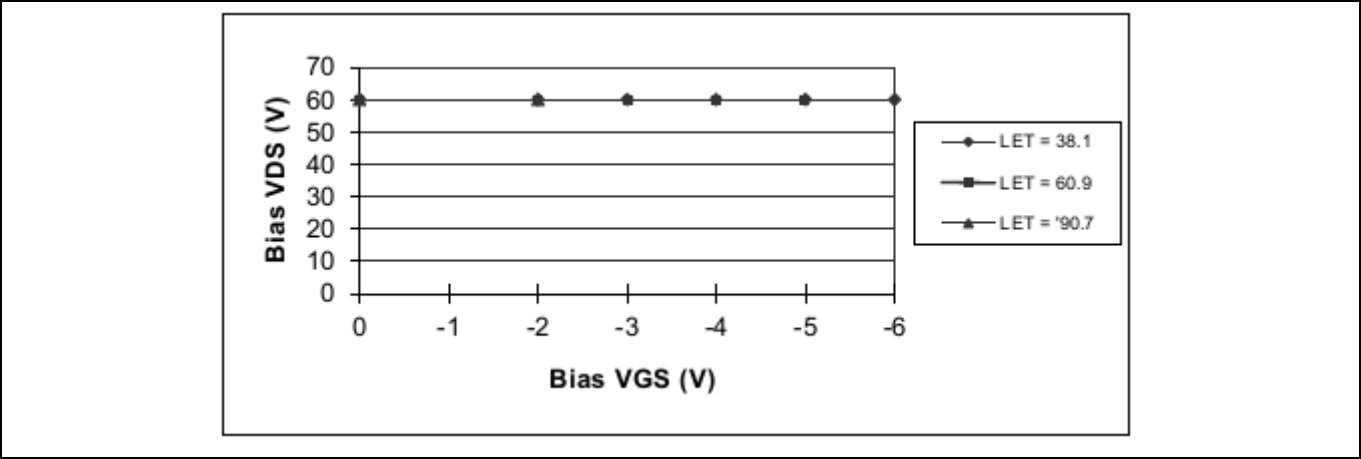


Figure 1 Typical Single Event Effect, Safe Operating Area

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Radiation Hardened Logic Level Power MOSFET Thru-Hole (TO-39)

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

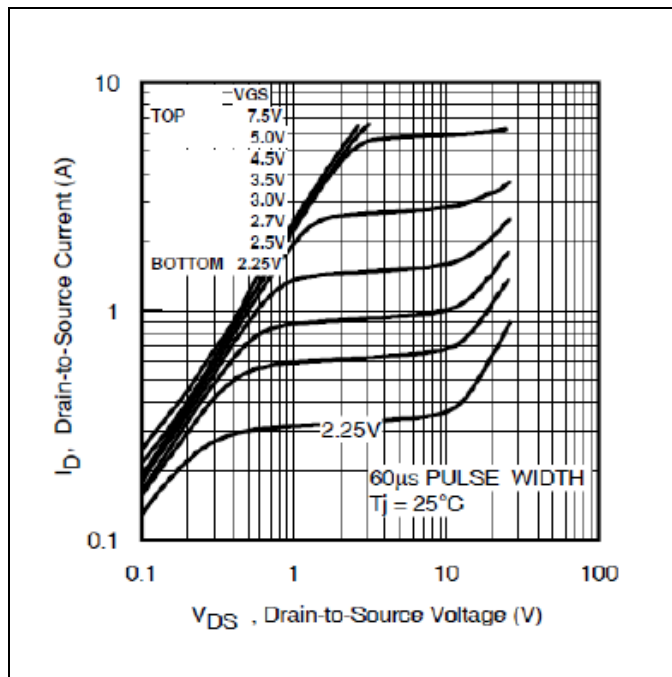


Figure 2 Typical Output Characteristics

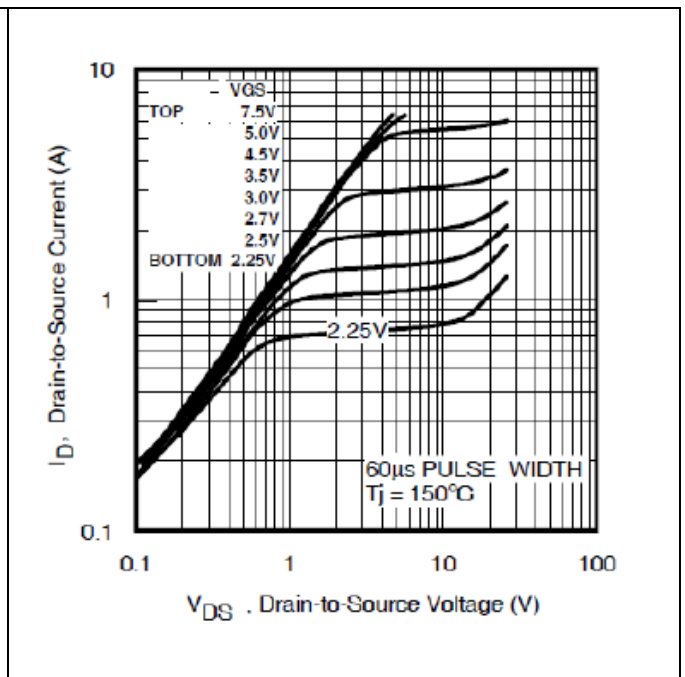


Figure 3 Typical Output Characteristics

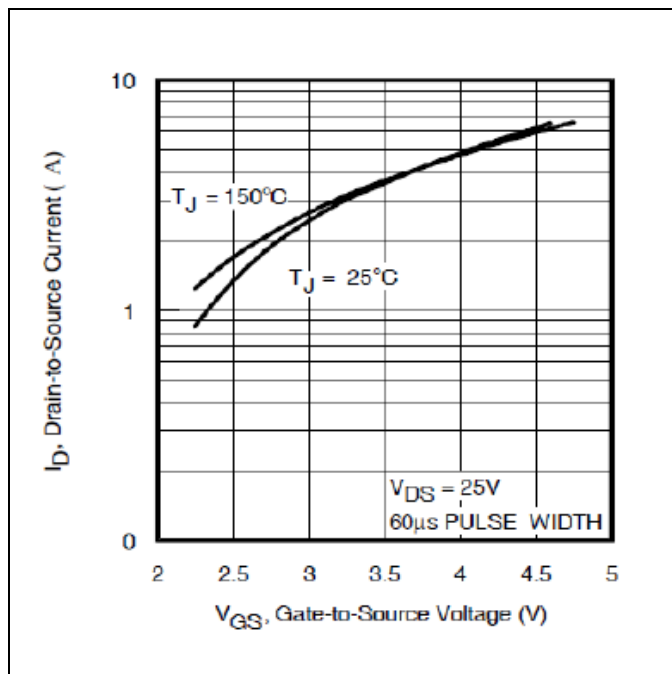


Figure 4 Typical Transfer Characteristics

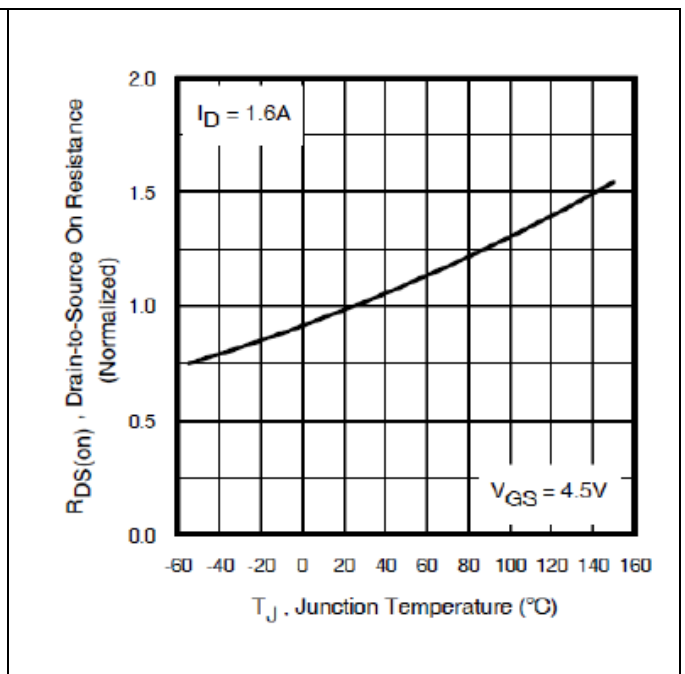


Figure 5 Normalized On-Resistance Vs. Temperature

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Radiation Hardened Logic Level Power MOSFET Thru-Hole (TO-39)

Electrical Characteristics Curves (Pre-irradiation)

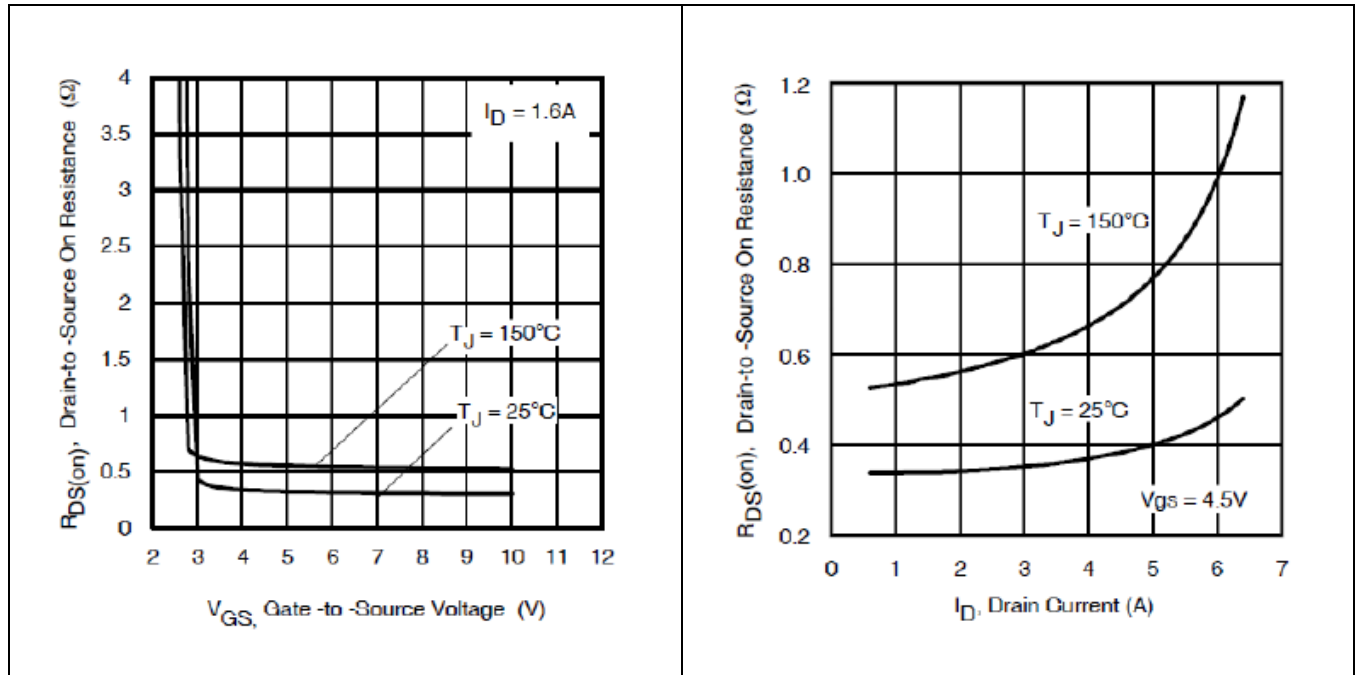


Figure 6 Typical On-Resistance Vs Gate Voltage

Figure 7 Typical On-Resistance Vs Drain Current

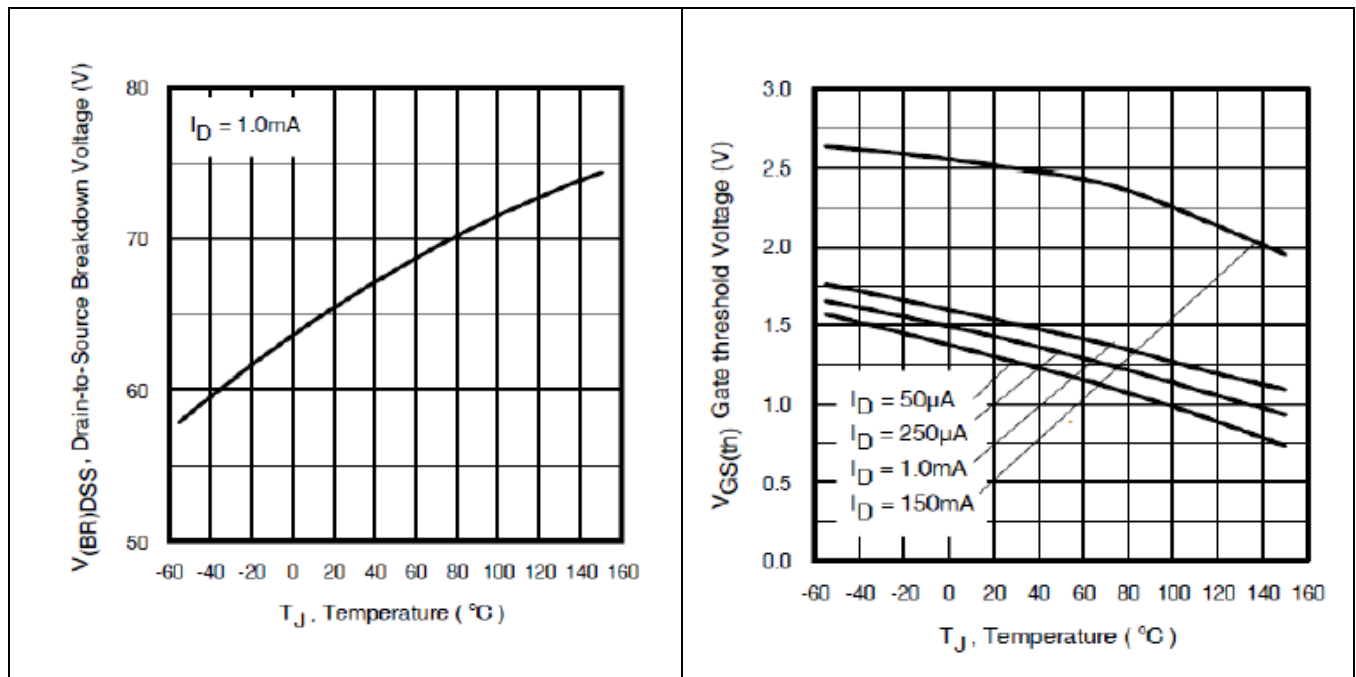


Figure 8 Typical Drain-to Source Breakdown Voltage Vs. Temperature

Figure 9 Typical Threshold Voltage Vs Temperature

Radiation Hardened Logic Level Power MOSFET Thru-Hole (TO-39)

Electrical Characteristics Curves (Pre-irradiation)

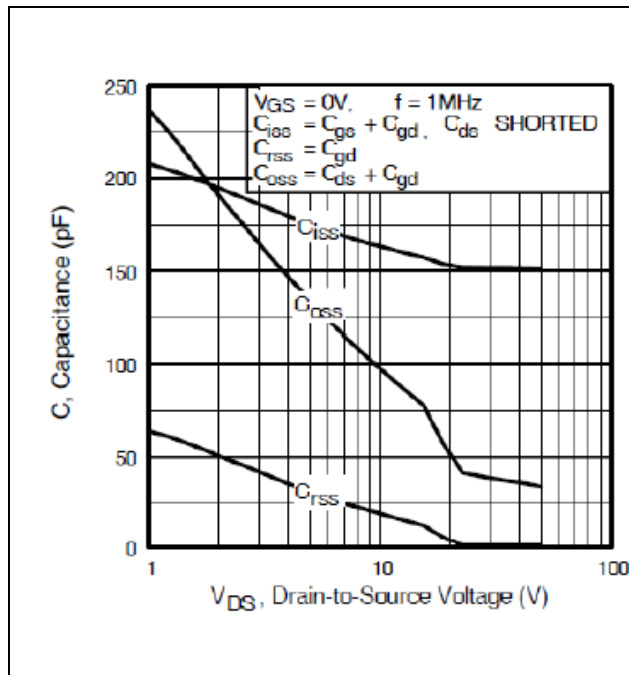


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

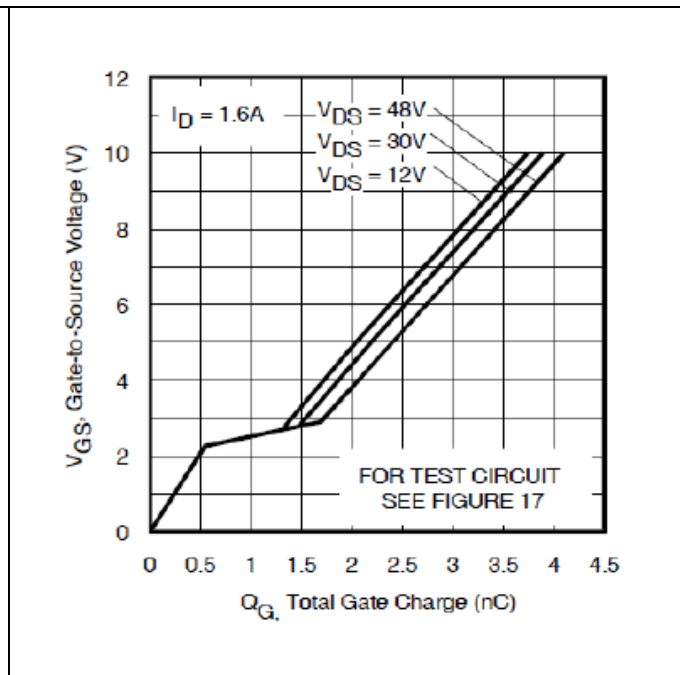


Figure 11 Typical Gate Charge Vs. Gate-to-Source Voltage

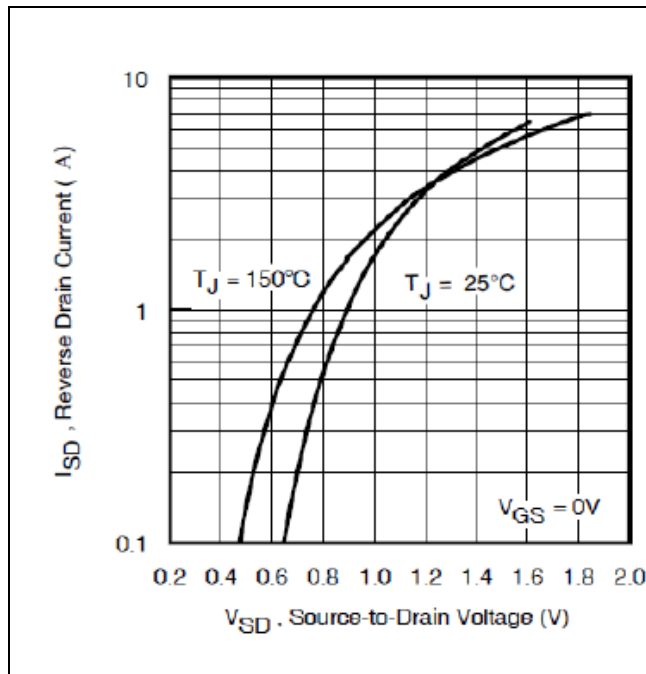


Figure 12 Typical Source-Drain Diode Forward Voltage

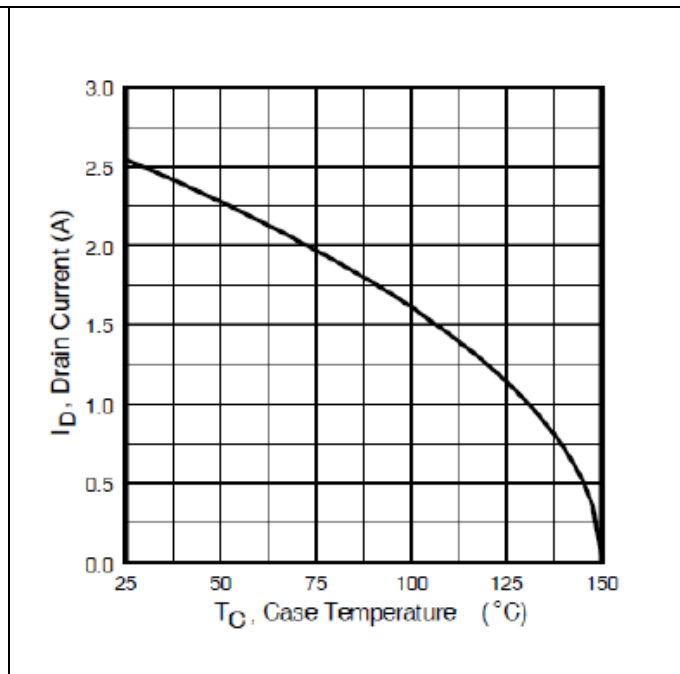
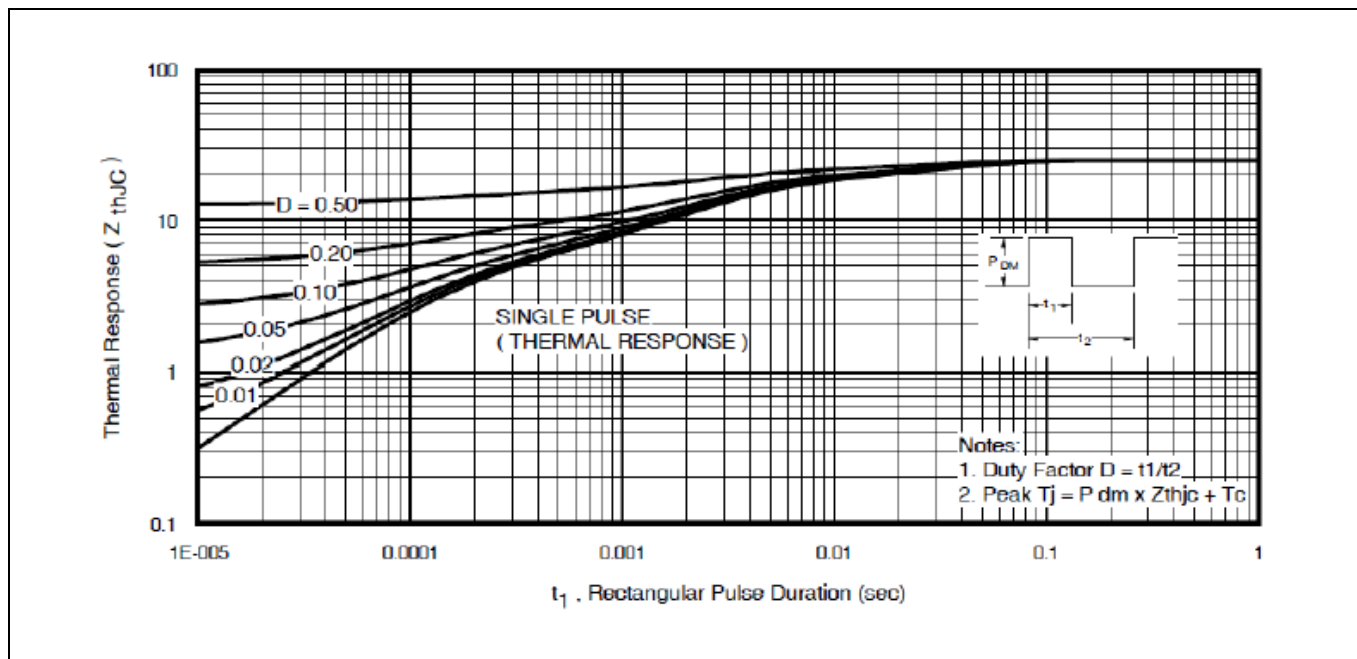
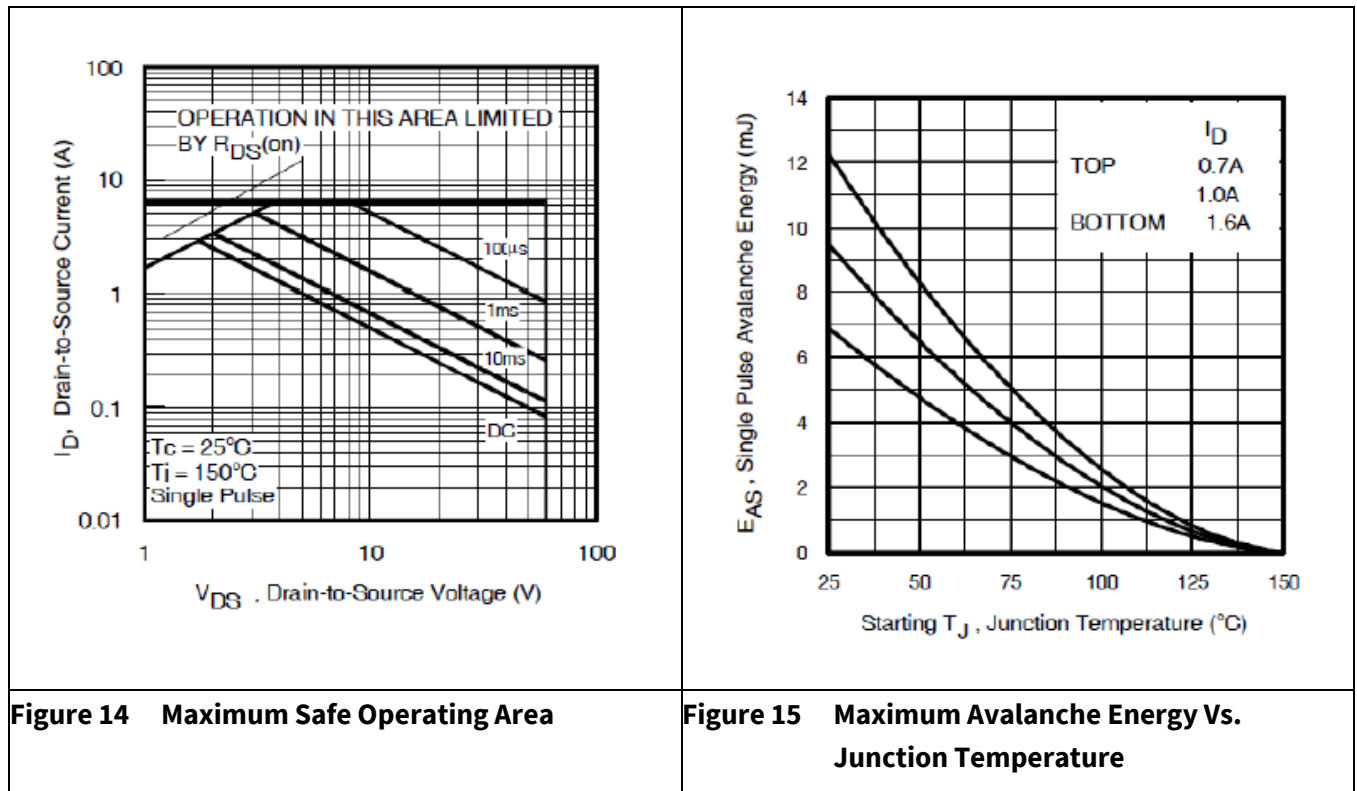


Figure 13 Maximum Drain Current Vs. Case Temperature

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Radiation Hardened Logic Level Power MOSFET Thru-Hole (TO-39)

Electrical Characteristics Curves (Pre-irradiation)



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Radiation Hardened Logic Level Power MOSFET Thru-Hole (TO-39)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

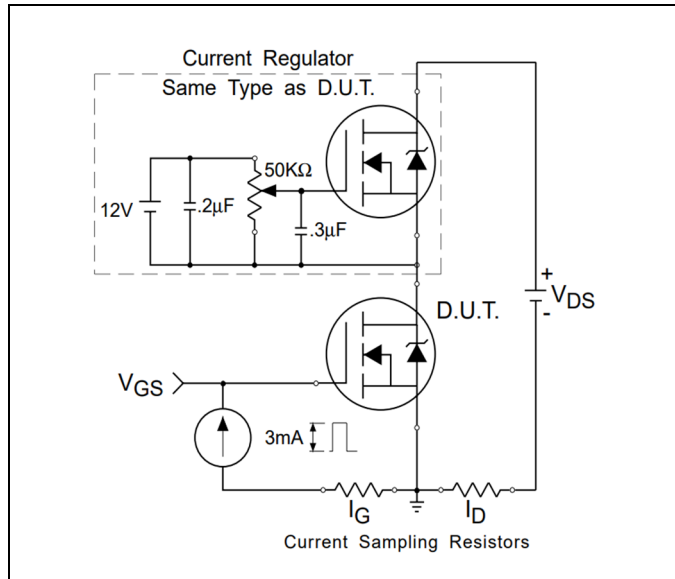


Figure 17 Gate Charge Test Circuit

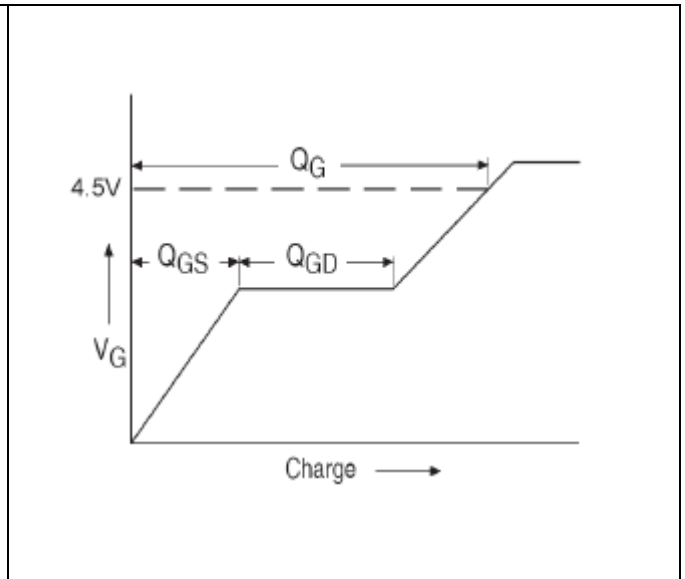


Figure 18 Gate Charge Waveform

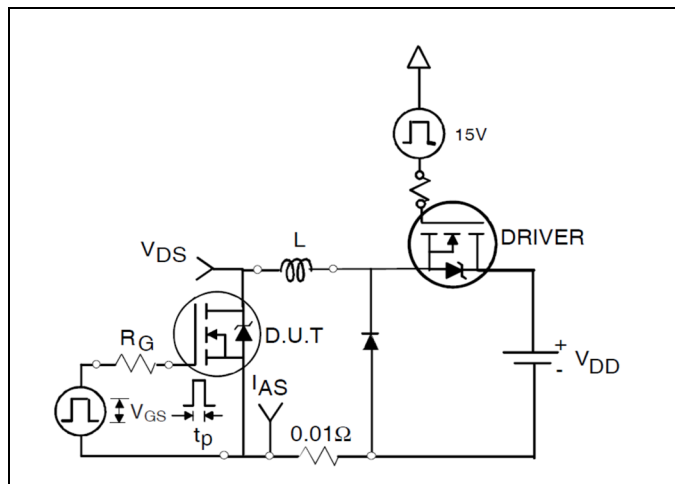


Figure 19 Unclamped Inductive Test Circuit

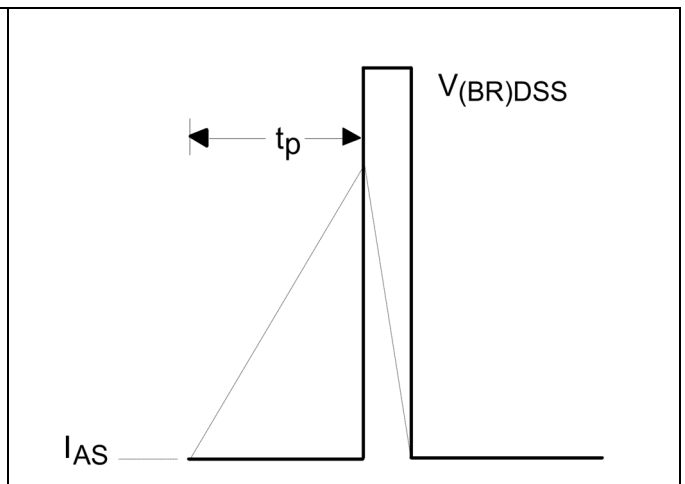


Figure 20 Unclamped Inductive Waveform

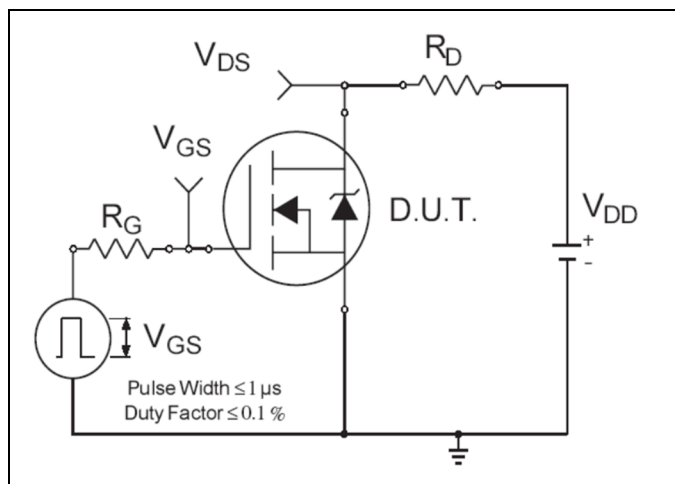


Figure 21 Switching Time Test Circuit

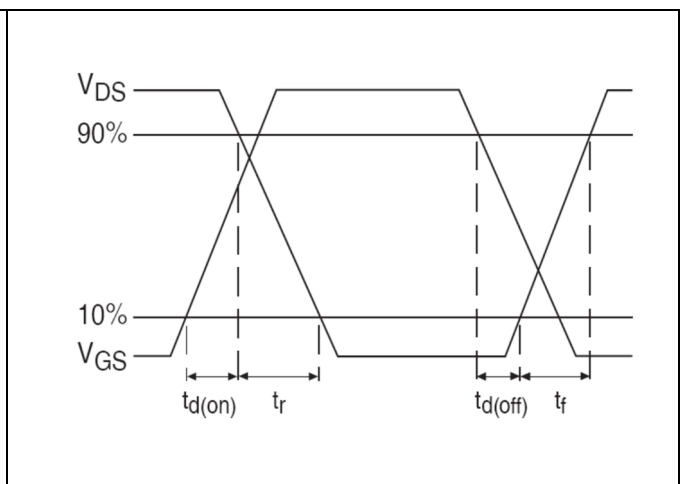
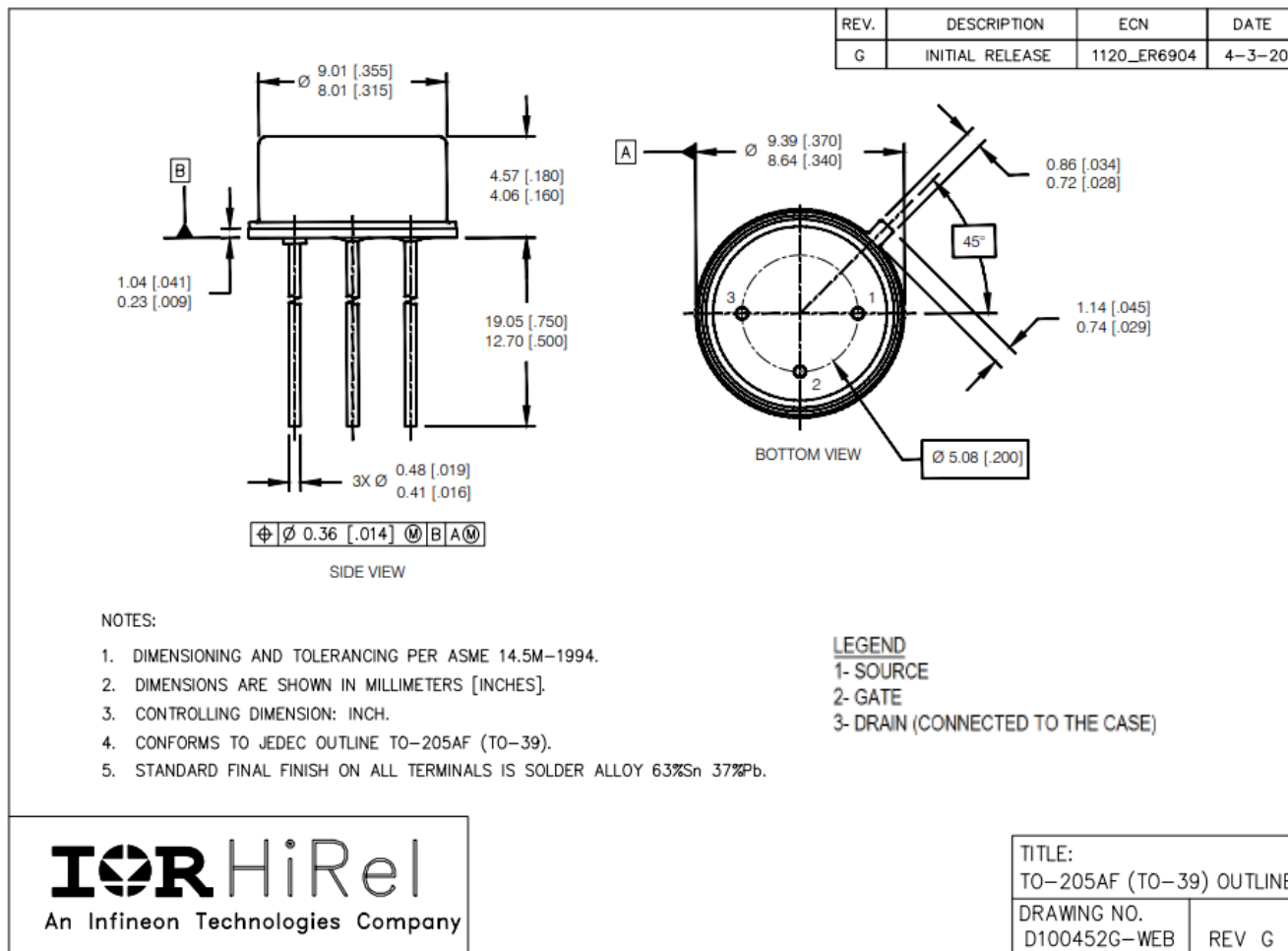


Figure 22 Switching Time Waveforms

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [TO-39](#)



Revision history

Document version	Date of release	Description of changes
	07/08/2003	Datasheet (PD-94695)
Rev A	10/22/2003	Updated from R6 to R7
Rev B	04/08/2004	Updated switching test condition-page2
Rev C	05/11/2005	Updated based on ECN-12213
Rev D	05/14/2007	Updated based on ECN-14810
Rev E	03/20/2008	Updated SEE table
Rev F	06/15/2010	Updated based on ECN-16672
Rev G	10/02/2016	Updated based on ECN-1120_01414
Rev H	05/13/2018	Updated based on ECN-1120_05810
Rev J	08/12/2022	Updated based on ECN-1120_09174

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