

IRHE9110

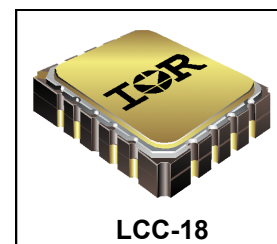
RADIATION HARDENED POWER MOSFET SURFACE MOUNT (LCC-18)

100V, P-CHANNEL

RAD Hard™ HEXFET® TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHE9110	100 kRads(Si)	1.1Ω	-2.3A
IRHE93110	300 kRads(Si)	1.1Ω	-2.3A



Description

IR HiRel RADHard™ HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low R_{DS(on)} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low R_{DS(on)}
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = -12V, T _C = 25°C	Continuous Drain Current	-2.3	A
I _{D2} @ V _{GS} = -12V, T _C = 100°C	Continuous Drain Current	-1.5	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	-9.2	
P _D @ T _C = 25°C	Maximum Power Dissipation	15	W
	Linear Derating Factor	0.1	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	75	mJ
I _{AR}	Avalanche Current ①	-2.3	A
E _{AR}	Repetitive Avalanche Energy ①	1.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-12.5	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temp.	300 (for 5s)	
	Weight	0.42 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.094	—	V/°C	Reference to 25°C, I _D = 1-.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.1	Ω	V _{GS} = -12V, I _{D2} = -1.5A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
g _{fs}	Forward Transconductance	—	—	—	S	V _{DS} = -15V, I _{D2} = -1.5A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = -80V, V _{GS} = 0V
		—	—	-250		V _{DS} = -80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _G	Total Gate Charge	—	—	16	nC	I _{D1} = -2.3A
Q _{GS}	Gate-to-Source Charge	—	—	4.3		V _{DS} = -50V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	3.3		V _{GS} = -12V
t _{d(on)}	Turn-On Delay Time	—	—	21	ns	V _{DD} = -50V
t _r	Rise Time	—	—	17		I _{D1} = -2.3A
t _{d(off)}	Turn-Off Delay Time	—	—	32		R _G = 7.5Ω
t _f	Fall Time	—	—	32		V _{GS} = -12V
L _s + L _D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	290	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	94	—		V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	13	—		f = 1.0MHz
R _g	Internal Gate Resistance	—	20.5	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-2.3	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-9.2		
V _{SD}	Diode Forward Voltage	—	—	-2.6	V	T _J = 25°C, I _S = -2.3A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	138	ns	T _J = 25°C, I _F = -2.3A, V _{DD} ≤ -25V
Q _{rr}	Reverse Recovery Charge	—	—	520	nC	di/dt = -100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	
R _{θJC}	Junction-to-Case	—	—	8.3	°C/W	
R _{θJPCB}	Junction-to-PC Board	—	19	—		Solder to a copper clad PC Board
R _{θJA}	Junction-to-Air	—	—	75		Typical Socket

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = -25V, starting T_J = 25°C, L = 28mH, Peak I_L = -2.3A, V_{GS} = -12V
- ③ I_{SD} ≤ -2.3A, di/dt ≤ -540A/μs, V_{DD} ≤ -100V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. -80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	100 kRads (Si) ¹		Up to 300k - 1000 kRads (Si) ²		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V _{GS} = 0V, I _D = -1.0mA
V _{GS(th)}	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100	nA	V _{GS} = 20V
I _{DSS}	Zero Gate Voltage Drain Current	—	-25	—	-25	μA	V _{DS} = -80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	1.06	—	1.06	Ω	V _{GS} = -12V, I _{D2} = -1.5A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (LCC-18)	—	1.1	—	1.1	Ω	V _{GS} = -12V, I _{D2} = -1.5A
V _{SD}	Diode Forward Voltage ④	—	-2.6	—	-2.6	V	V _{GS} = 0V, I _S = -2.3A

1. Part number IRHE9110
2. Part number IRHE93110

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
				@ VGS = 0V	@ VGS = 5V	@ VGS = 10V	@ VGS = 15V	@ VGS = 20V
Cu	28.0	285	43.0	-100	-100	-100	-70	-60
Br	36.8	305	39	-100	-100	-70	-50	-40
I	59.8	343	32.6	-60	—	—	—	—

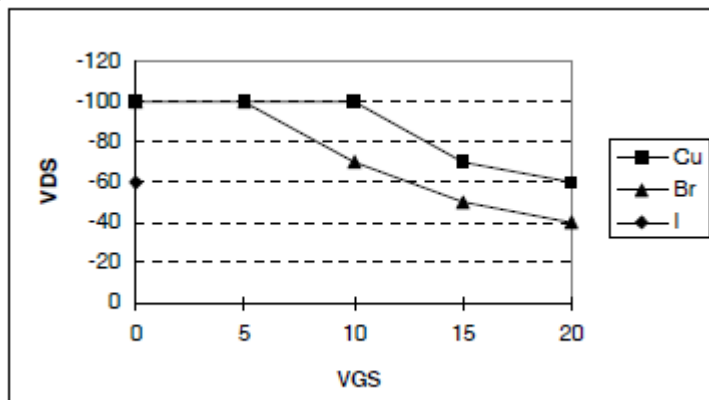


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

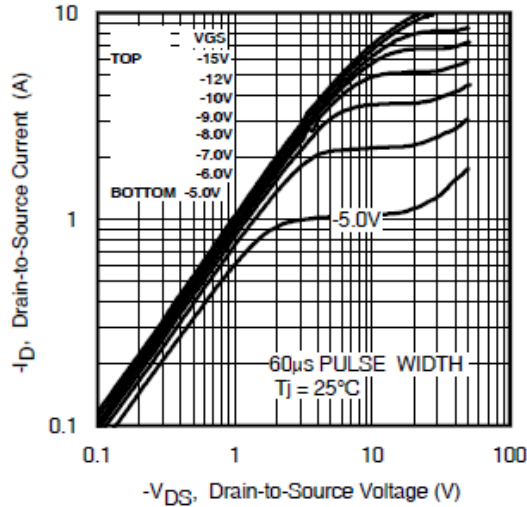


Fig 1. Typical Output Characteristics

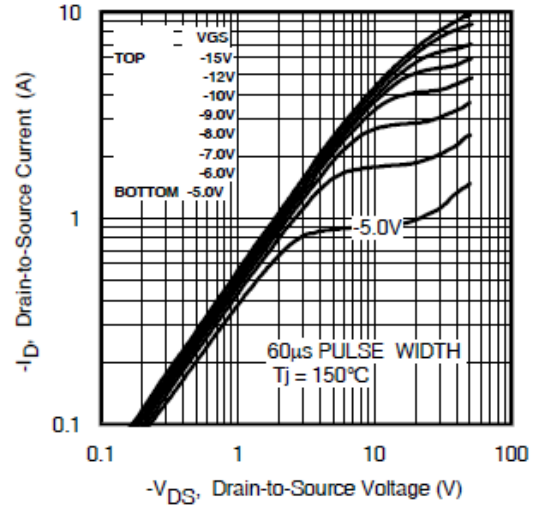


Fig 2. Typical Output Characteristics

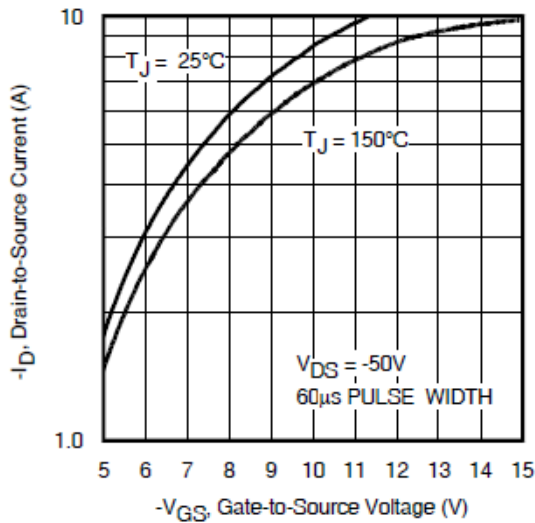


Fig 3. Typical Transfer Characteristics

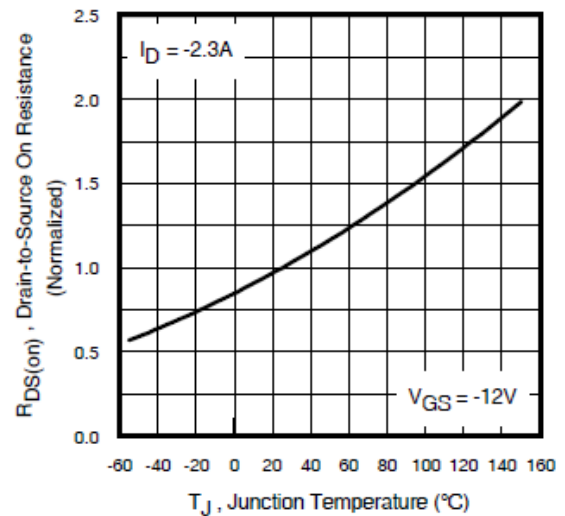


Fig 4. Normalized On-Resistance Vs. Temperature

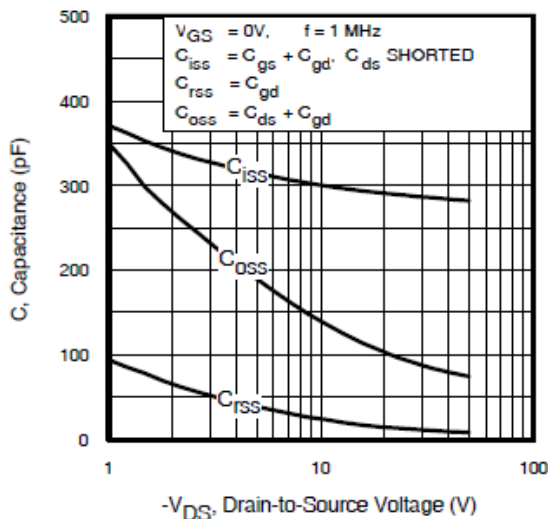


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

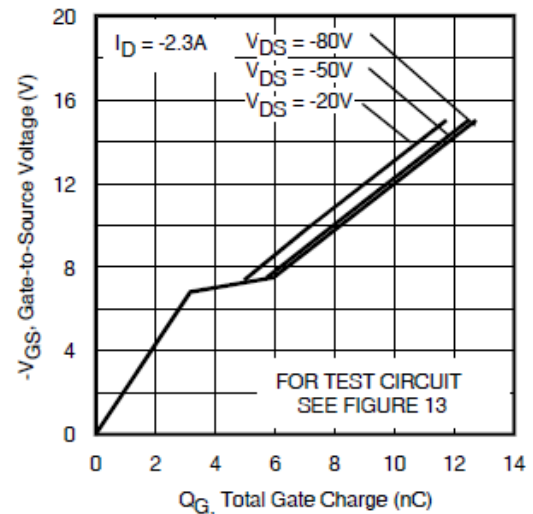


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

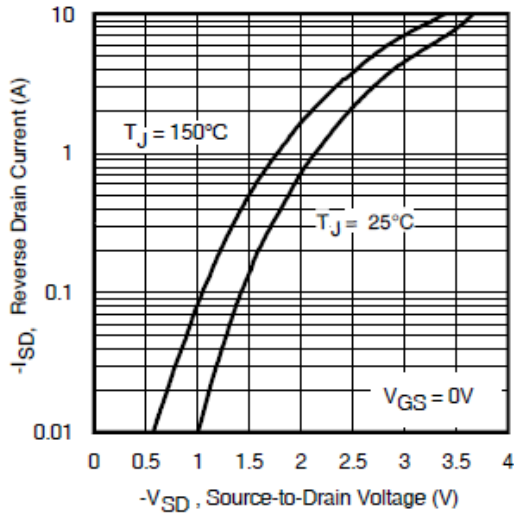


Fig 7. Typical Source-Drain Diode Forward Voltage

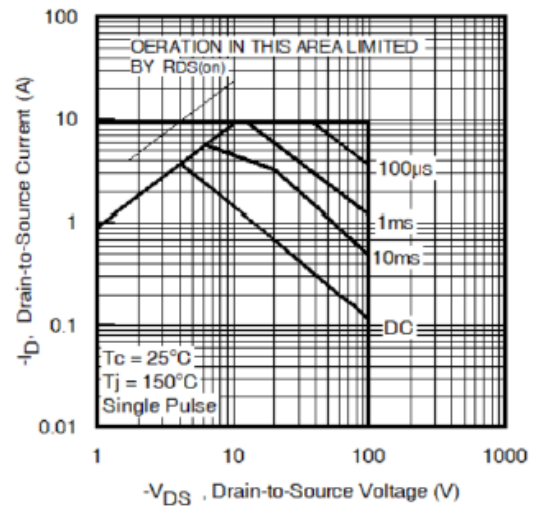


Fig 8. Maximum Safe Operating Area

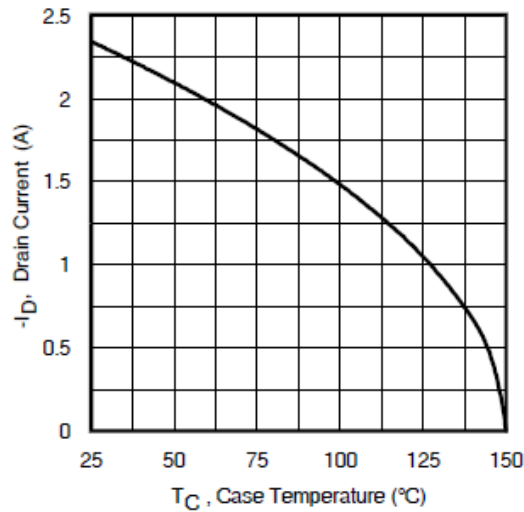


Fig 9. Maximum Drain Current Vs. Case Temperature

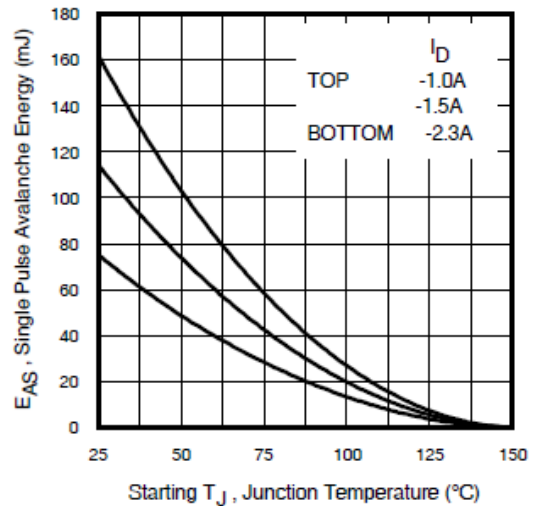


Fig 10. Maximum Avalanche Energy Vs. Drain Current

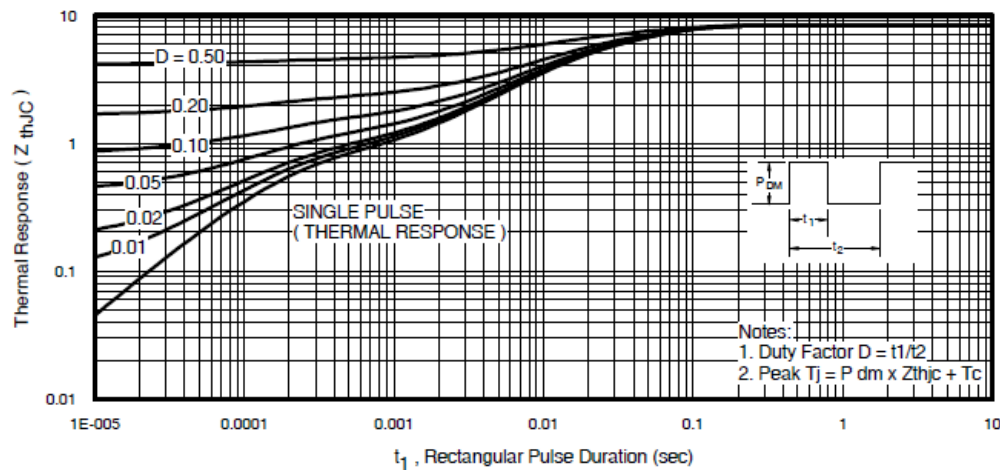


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

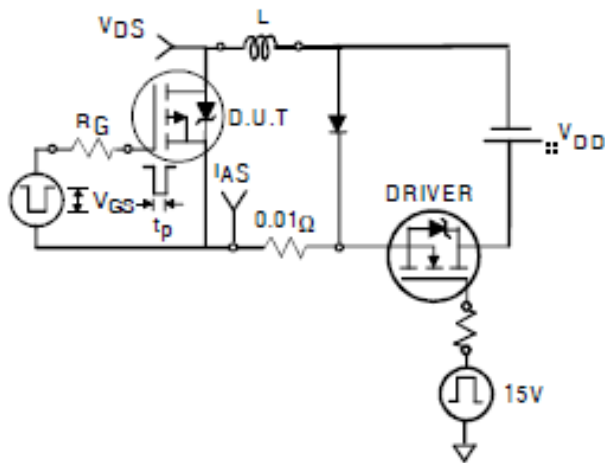


Fig 12a. Unclamped Inductive Test Circuit

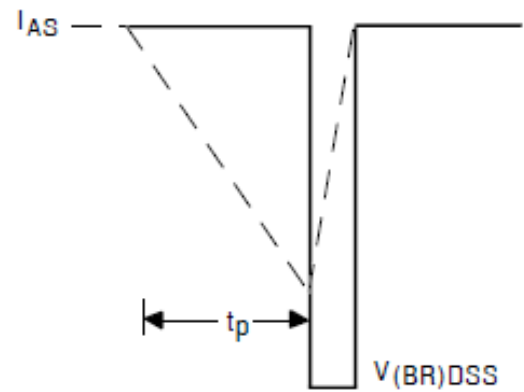


Fig 12b. Unclamped Inductive Waveforms

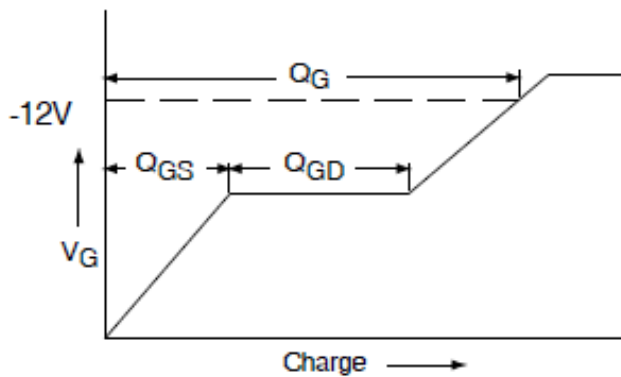


Fig 13a. Gate Charge Waveform

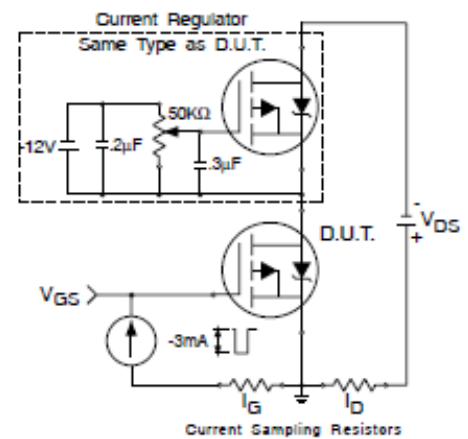


Fig 13b. Gate Charge Test Circuit

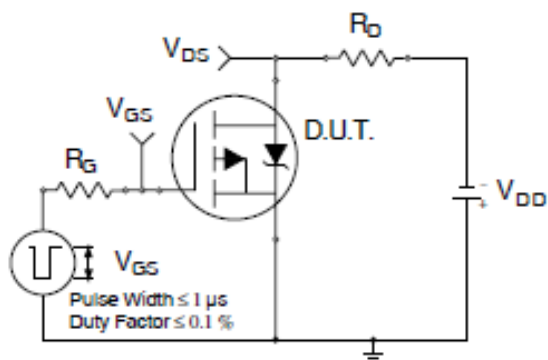


Fig 14a. Switching Time Test Circuit

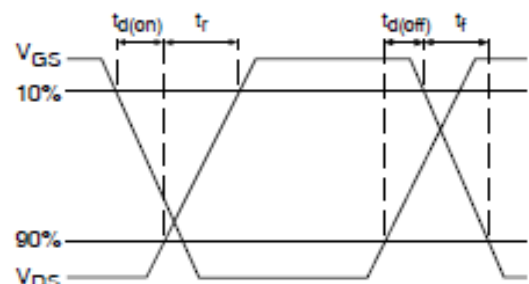
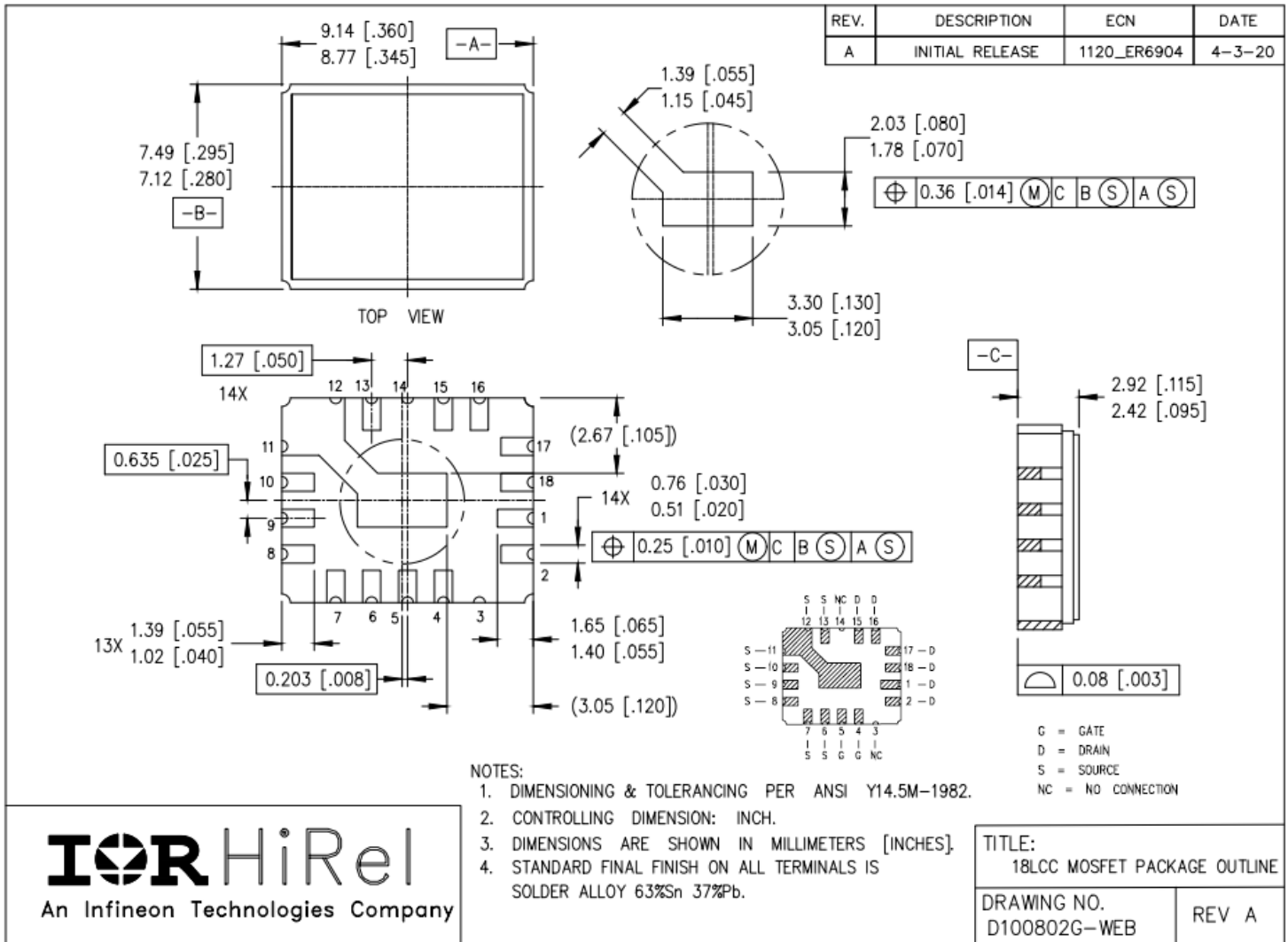


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: LCC-18

Case Outline and Dimensions — LCC-18



IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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