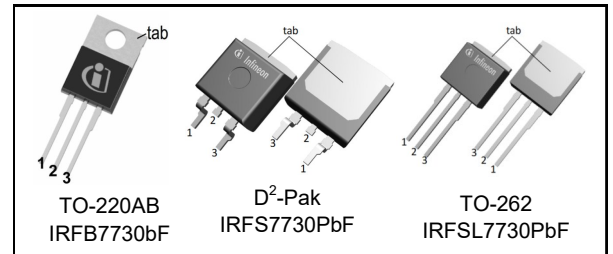
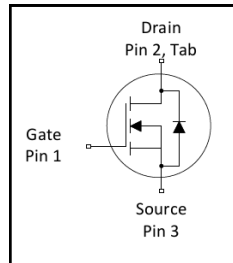


V_{DSS}	75V
$R_{DS(on)}$ typ. max	2.2mΩ
	2.6mΩ
I_D (Silicon Limited)	246A Ⓢ
I_D (Package Limited)	195A



G	D	S
Gate	Drain	Source

Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant, Halogen-Free

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB7730PbF	TO-220	Tube	50	IRFB7730PbF
IRFS7730PbF	D²-Pak	Tape and Reel	800	IRFS7730PbF
IRFSL7730PbF	TO-262	Tube	50	IRFSL7730PbF

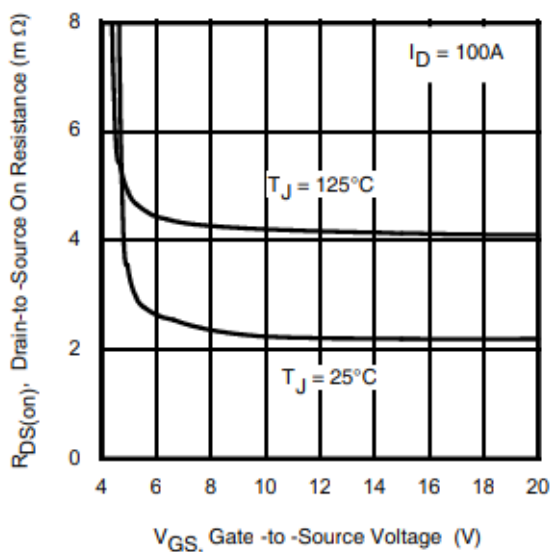


Fig 1. Typical On– Resistance vs. Gate Voltage

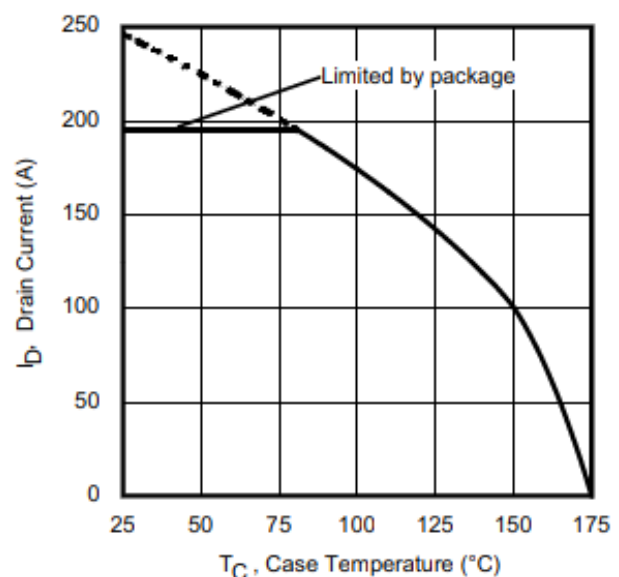


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	246①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	174	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	195	
I_{DM}	Pulsed Drain Current ②	984*	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	465	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ⑨	898	
I_{AR}	Avalanche Current ②	See Fig 15, 15, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.40	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient (TO-220)	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑩	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	40	—	mV/°C	Reference to 25°C , $I_D = 1\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.2	2.6	mΩ	$V_{GS} = 10\text{V}$, $I_D = 100\text{A}$
		—	2.6	—		$V_{GS} = 6.0\text{V}$, $I_D = 50\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	2.1	—	Ω	

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
 - ② Repetitive rating; pulse width limited by max. junction temperature.
 - ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 93\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$.
 - ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1626\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
 - ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
 - ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 - ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 - ⑧ R_θ is measured at T_J approximately 90°C .
 - ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1.0\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 42\text{A}$, $V_{GS} = 10\text{V}$.
 - ⑩ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note # [AN-994](#) for more details:
- * Pulse drain current is limited at 780A by source bonding technology.

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	249	—	—	S	$V_{DS} = 10V, I_D = 100A$
Q_g	Total Gate Charge	—	271	407	nC	$I_D = 100A$ $V_{DS} = 38V$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source Charge	—	55	—		
Q_{gd}	Gate-to-Drain Charge	—	79	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	192	—		
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$V_{DD} = 38V$ $I_D = 100A$ $R_G = 2.7\Omega$ $V_{GS} = 10V$ ⑤
t_r	Rise Time	—	120	—		
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		
t_f	Fall Time	—	115	—		
C_{iss}	Input Capacitance	—	13660	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig.7
C_{oss}	Output Capacitance	—	1120	—		
C_{rss}	Reverse Transfer Capacitance	—	690	—		
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	1060	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$ ⑦
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	1275	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$ ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	246①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	984*		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 100A, V_{GS} = 0V$ ⑤
dv/dt	Peak Diode Recovery dv/dt ④	—	16	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 100A, V_{DS} = 75V$
t_{rr}	Reverse Recovery Time	—	44	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 64V$
		—	51	—		$T_J = 125^\circ\text{C}$ $I_F = 100A$,
Q_{rr}	Reverse Recovery Charge	—	70	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	97	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.6	—	A	$T_J = 25^\circ\text{C}$

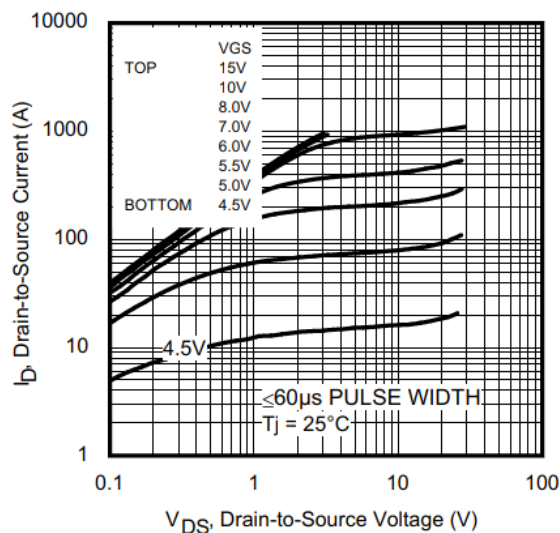


Fig 3. Typical Output Characteristics

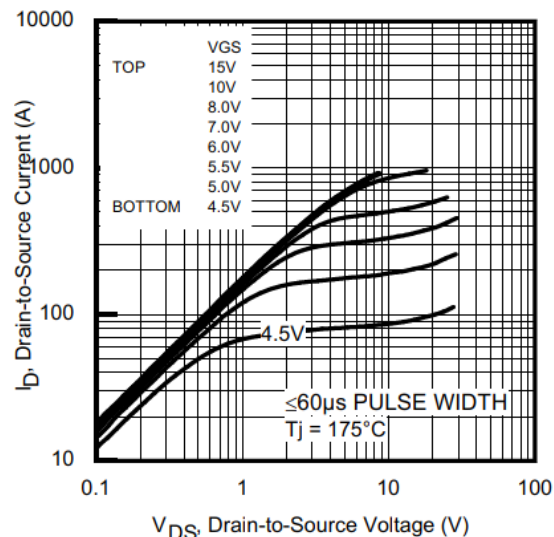


Fig 4. Typical Output Characteristics

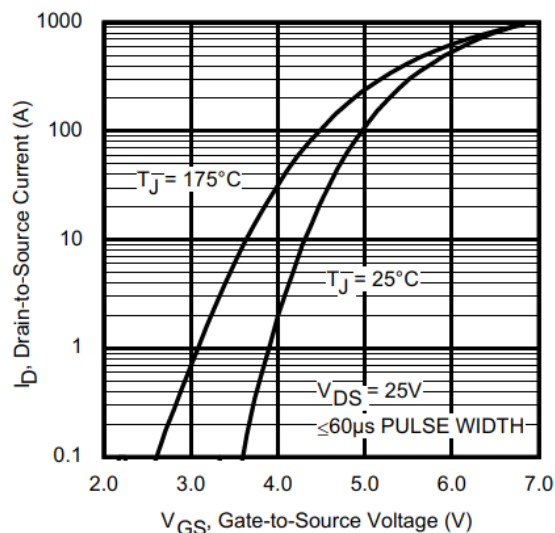


Fig 5. Typical Transfer Characteristics

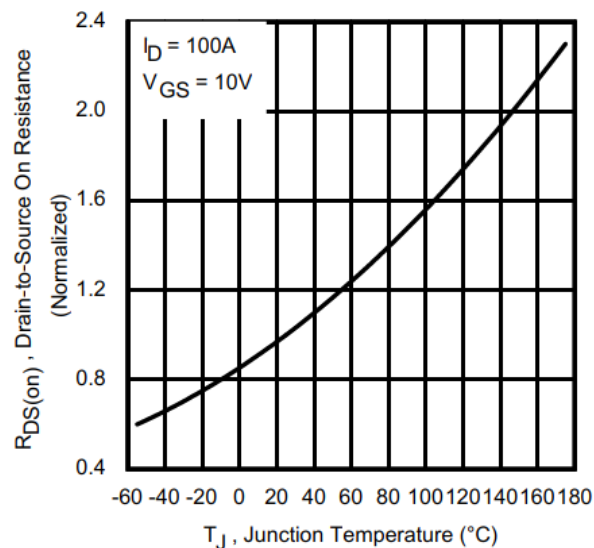


Fig 6. Normalized On-Resistance vs. Temperature

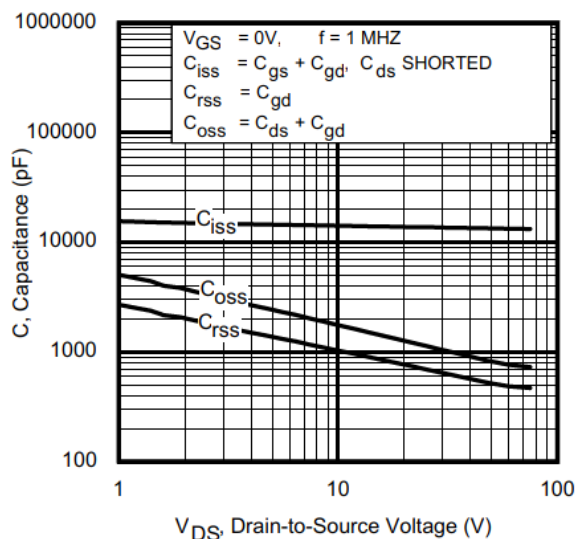


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

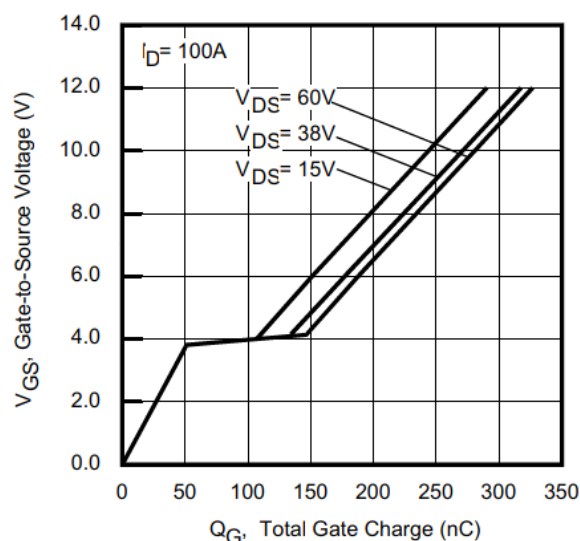


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

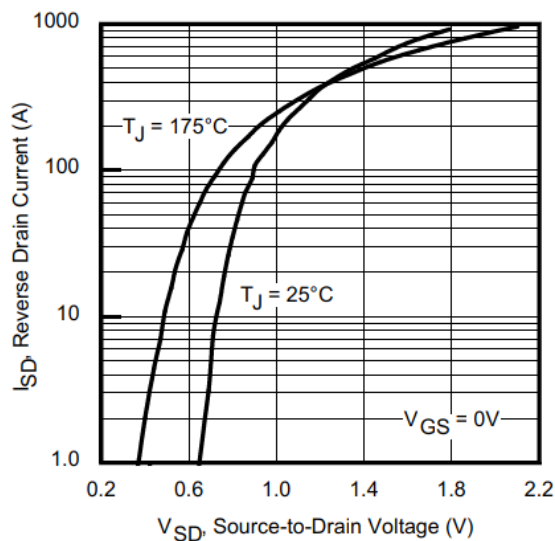


Fig 9. Typical Source-Drain Diode Forward Voltage

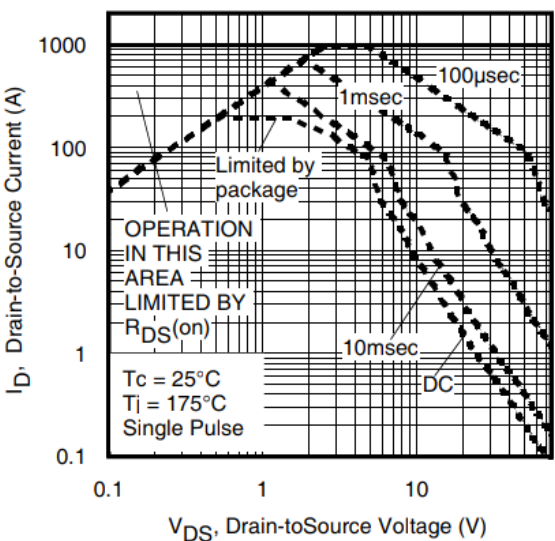


Fig 10. Maximum Safe Operating Area

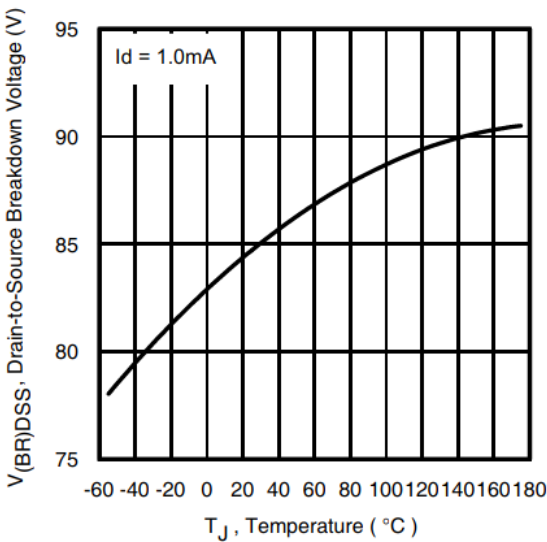


Fig 11. Drain-to-Source Breakdown Voltage

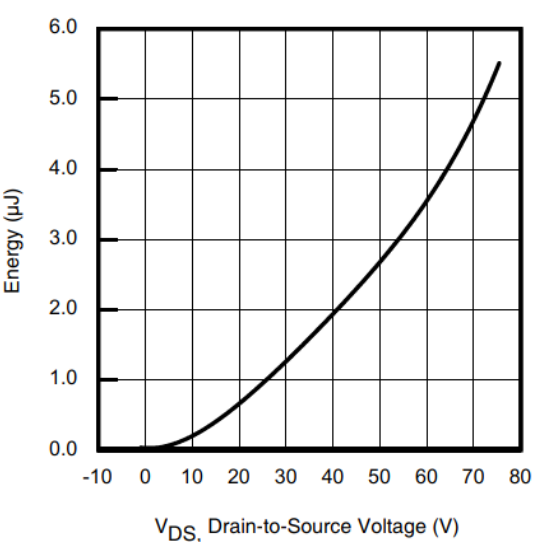


Fig 12. Typical C_{oss} Stored Energy

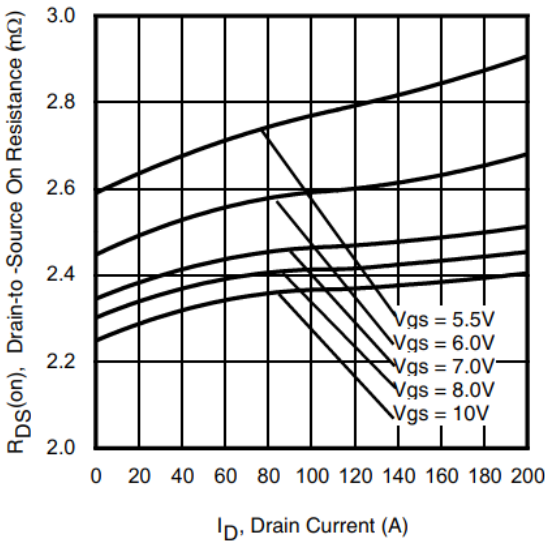


Fig 13. Typical On-Resistance vs. Drain Current

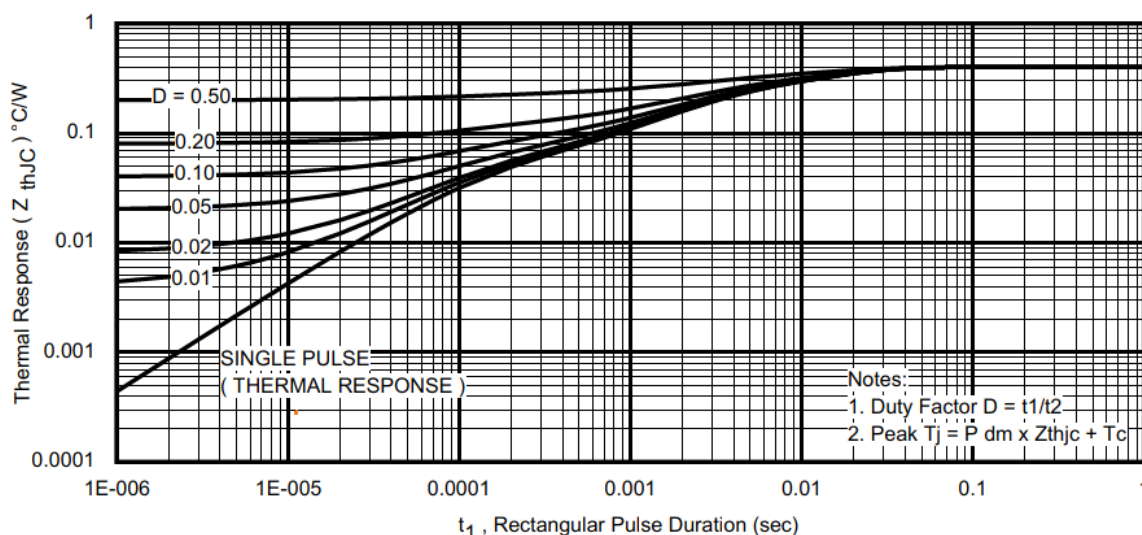


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

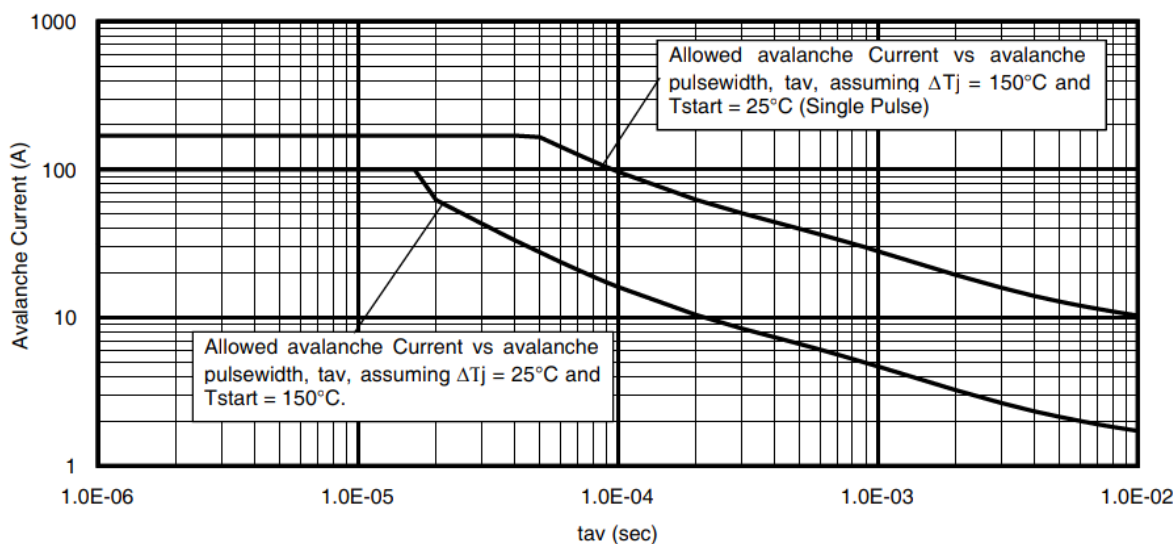


Fig 15. Avalanche Current vs. Pulse Width

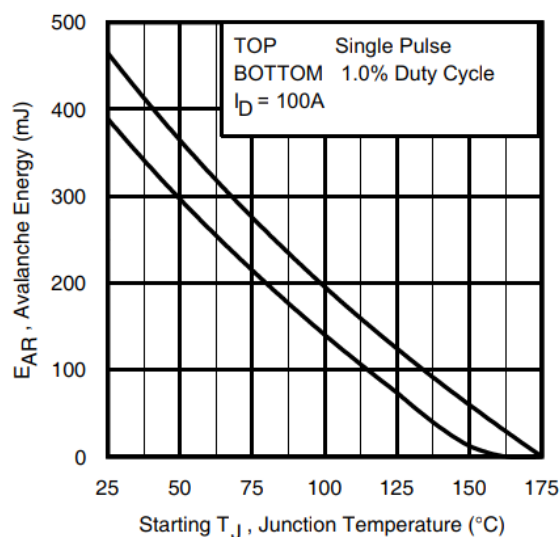


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

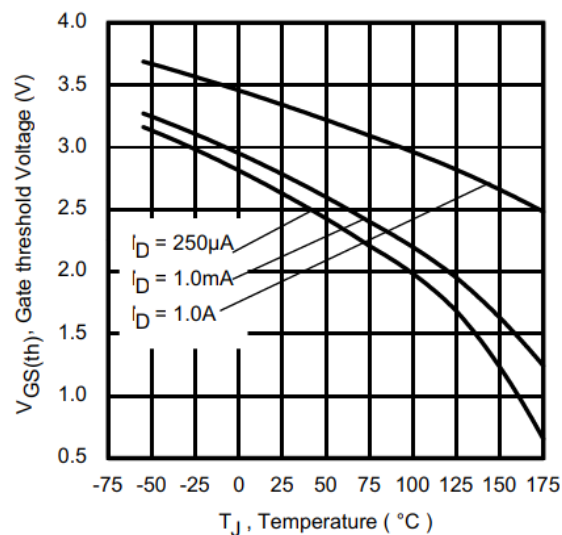


Fig 17. Threshold Voltage vs. Temperature

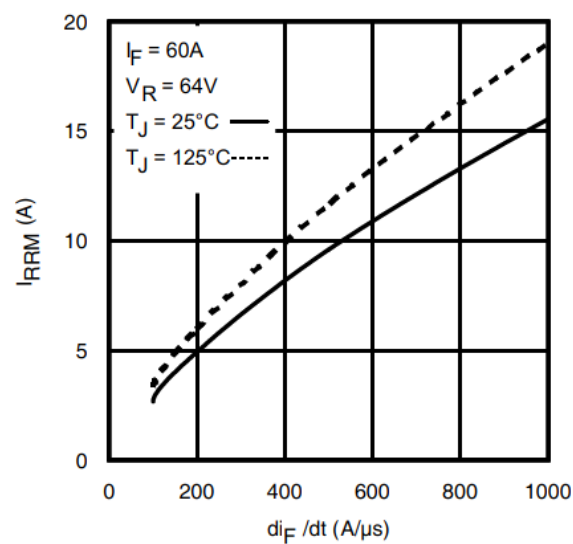


Fig 18. Typical Recovery Current vs. dif/dt

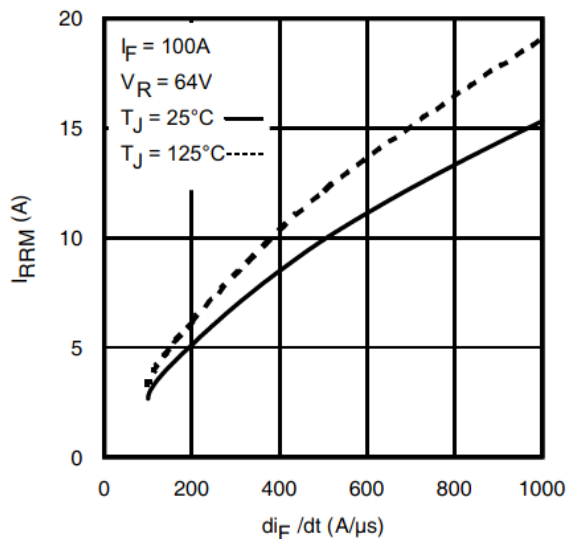


Fig 19. Typical Recovery Current vs. dif/dt

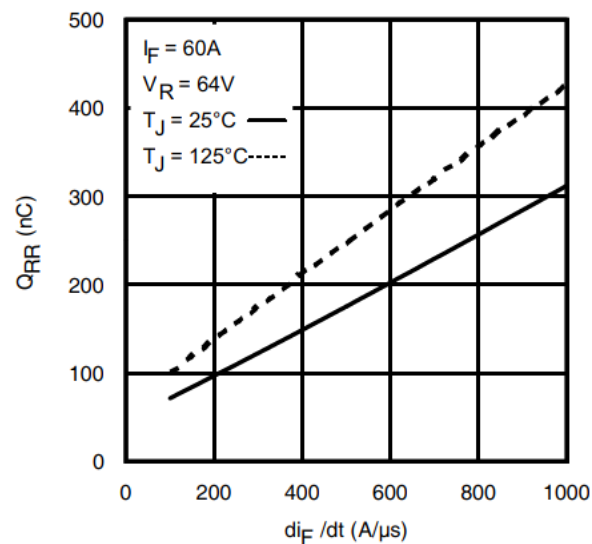


Fig 20. Typical Stored Charge vs. dif/dt

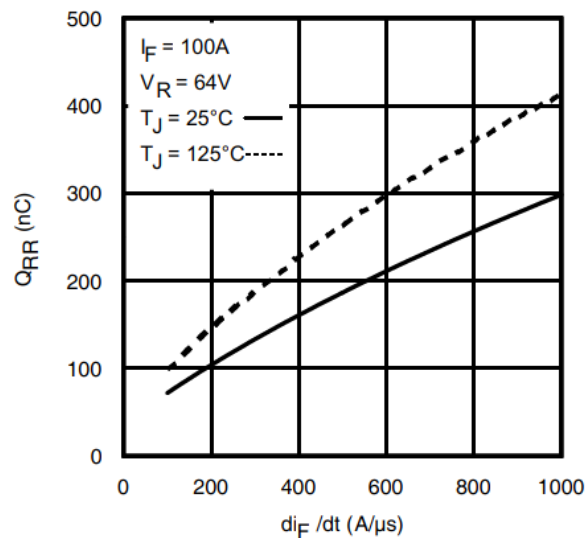


Fig 21. Typical Stored Charge vs. dif/dt

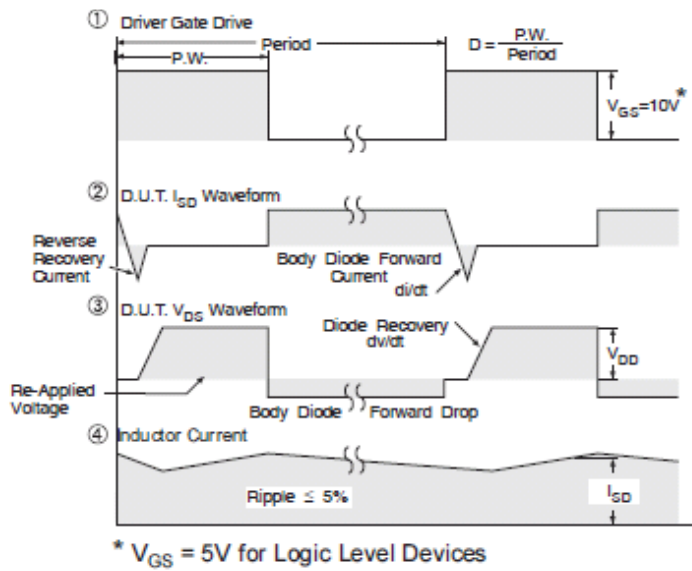
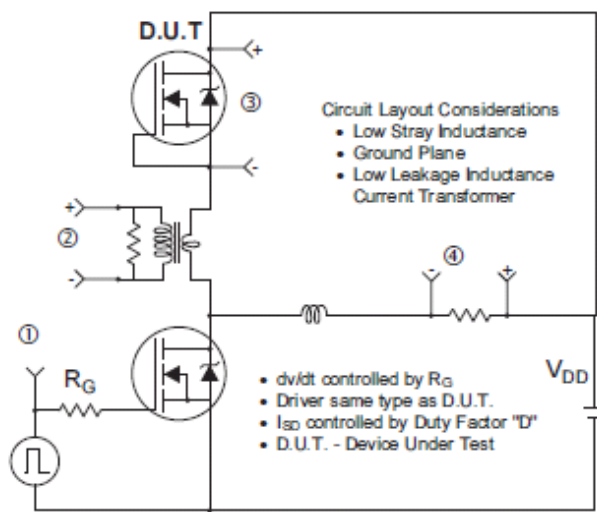


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

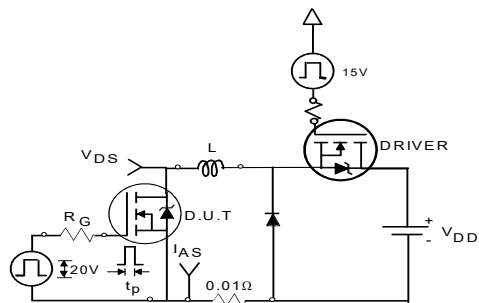


Fig 23a. Unclamped Inductive Test Circuit

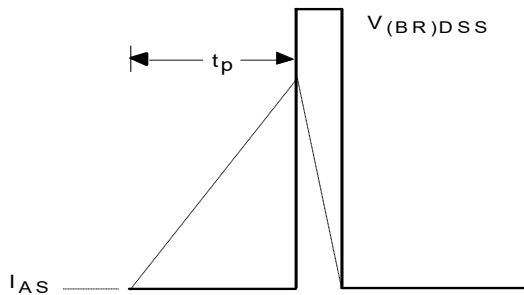


Fig 23b. Unclamped Inductive Waveforms

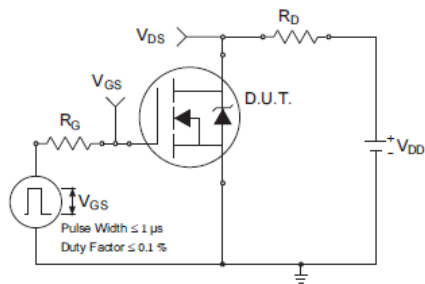


Fig 24a. Switching Time Test Circuit

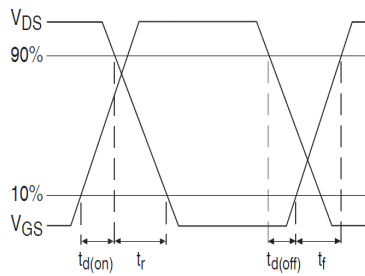


Fig 24b. Switching Time Waveforms

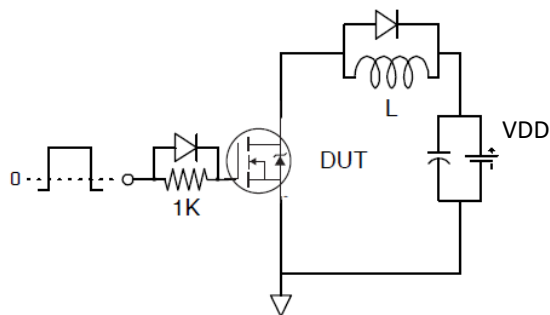


Fig 25a. Gate Charge Test Circuit

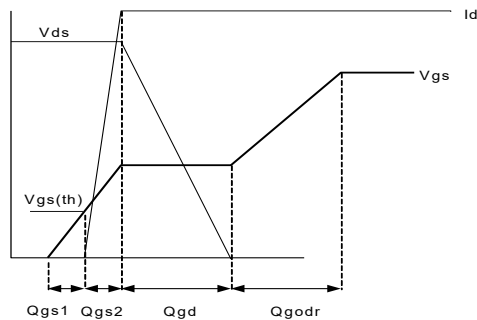
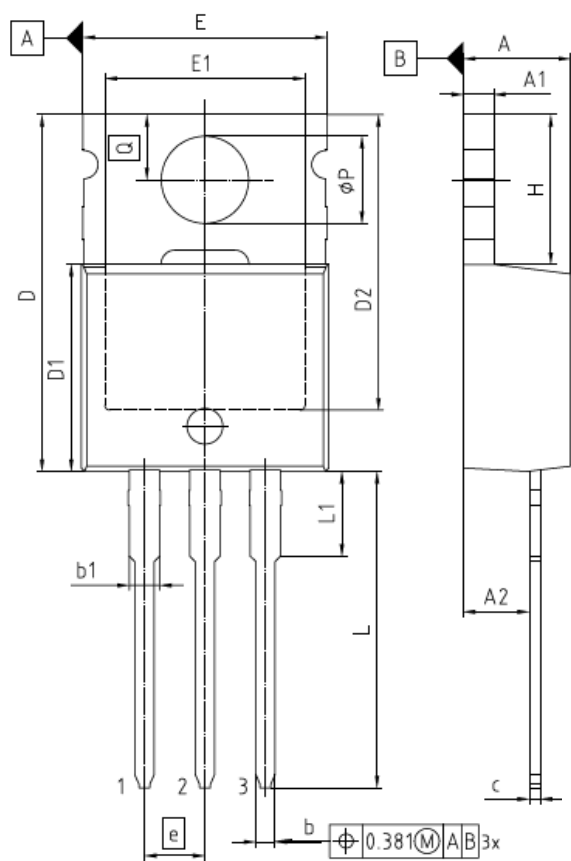


Fig 25b. Gate Charge Waveform

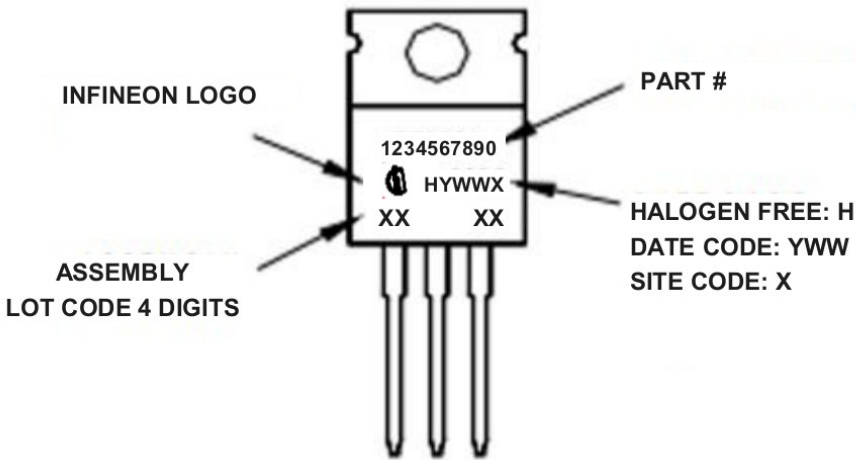
TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

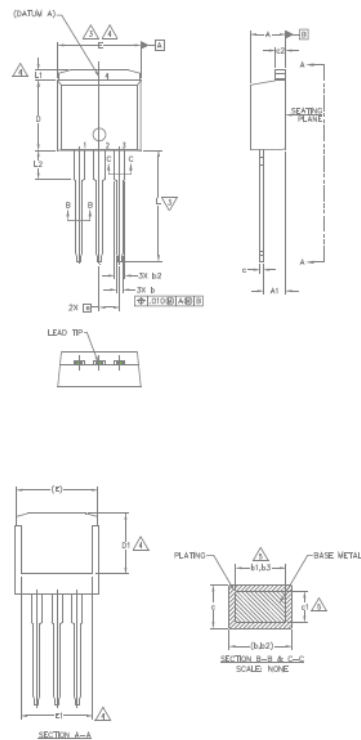
PACKAGE - GROUP NUMBER: PG-TO220-3-U05		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
ØP	3.54	4.08
Q	2.54	3.42

TO-220AB Part Marking Information



TO-220AB packages are not recommended for Surface Mount Application.

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	5
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	4

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. CONTROLLING DIMENSION: INCH.
 7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

- 1.— GATE
- 2.— COLLECTOR
- 3.— EMITTER
- 4.— COLLECTOR

HEXFET

- 1.— GATE
- 2.— DRAIN
- 3.— SOURCE
- 4.— DRAIN

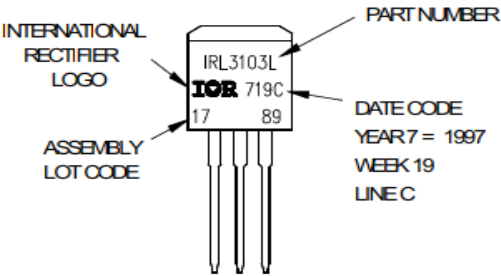
DIODES

- 1.— ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.— CATHODE
- 3.— ANODE

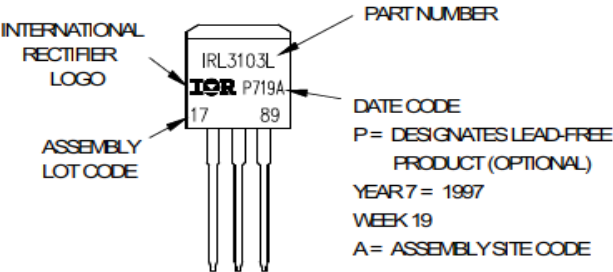
TO-262 Part Marking Information

EXAMPLE THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON VWV19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"



OR



Technical drawing of a lead tip assembly, showing multiple views and details.

Top View: Shows the overall dimensions and features. Key dimensions include L_1 , L_2 , L_3 , L_4 , L_5 , L_6 , L_7 , L_8 , L_9 , L_{10} , L_{11} , L_{12} , L_{13} , L_{14} , L_{15} , L_{16} , L_{17} , L_{18} , L_{19} , L_{20} , L_{21} , L_{22} , L_{23} , L_{24} , L_{25} , L_{26} , L_{27} , L_{28} , L_{29} , L_{30} , L_{31} , L_{32} , L_{33} , L_{34} , L_{35} , L_{36} , L_{37} , L_{38} , L_{39} , L_{40} , L_{41} , L_{42} , L_{43} , L_{44} , L_{45} , L_{46} , L_{47} , L_{48} , L_{49} , L_{50} , L_{51} , L_{52} , L_{53} , L_{54} , L_{55} , L_{56} , L_{57} , L_{58} , L_{59} , L_{60} , L_{61} , L_{62} , L_{63} , L_{64} , L_{65} , L_{66} , L_{67} , L_{68} , L_{69} , L_{70} , L_{71} , L_{72} , L_{73} , L_{74} , L_{75} , L_{76} , L_{77} , L_{78} , L_{79} , L_{80} , L_{81} , L_{82} , L_{83} , L_{84} , L_{85} , L_{86} , L_{87} , L_{88} , L_{89} , L_{90} , L_{91} , L_{92} , L_{93} , L_{94} , L_{95} , L_{96} , L_{97} , L_{98} , L_{99} , L_{100} . Key features include **DATUM A**, **2x b2**, **2x b1**, **2x b3**, **2x b4**, **2x b5**, **2x b6**, **2x b7**, **2x b8**, **2x b9**, **2x b10**, **2x b11**, **2x b12**, **2x b13**, **2x b14**, **2x b15**, **2x b16**, **2x b17**, **2x b18**, **2x b19**, **2x b20**, **2x b21**, **2x b22**, **2x b23**, **2x b24**, **2x b25**, **2x b26**, **2x b27**, **2x b28**, **2x b29**, **2x b30**, **2x b31**, **2x b32**, **2x b33**, **2x b34**, **2x b35**, **2x b36**, **2x b37**, **2x b38**, **2x b39**, **2x b40**, **2x b41**, **2x b42**, **2x b43**, **2x b44**, **2x b45**, **2x b46**, **2x b47**, **2x b48**, **2x b49**, **2x b50**, **2x b51**, **2x b52**, **2x b53**, **2x b54**, **2x b55**, **2x b56**, **2x b57**, **2x b58**, **2x b59**, **2x b60**, **2x b61**, **2x b62**, **2x b63**, **2x b64**, **2x b65**, **2x b66**, **2x b67**, **2x b68**, **2x b69**, **2x b70**, **2x b71**, **2x b72**, **2x b73**, **2x b74**, **2x b75**, **2x b76**, **2x b77**, **2x b78**, **2x b79**, **2x b80**, **2x b81**, **2x b82**, **2x b83**, **2x b84**, **2x b85**, **2x b86**, **2x b87**, **2x b88**, **2x b89**, **2x b90**, **2x b91**, **2x b92**, **2x b93**, **2x b94**, **2x b95**, **2x b96**, **2x b97**, **2x b98**, **2x b99**, **2x b100**. Key features include **DATUM A**, **2x b2**, **2x b1**, **2x b3**, **2x b4**, **2x b5**, **2x b6**, **2x b7**, **2x b8**, **2x b9**, **2x b10**, **2x b11**, **2x b12**, **2x b13**, **2x b14**, **2x b15**, **2x b16**, **2x b17**, **2x b18**, **2x b19**, **2x b20**, **2x b21**, **2x b22**, **2x b23**, **2x b24**, **2x b25**, **2x b26**, **2x b27**, **2x b28**, **2x b29**, **2x b30**, **2x b31**, **2x b32**, **2x b33**, **2x b34**, **2x b35**, **2x b36**, **2x b37**, **2x b38**, **2x b39**, **2x b40**, **2x b41**, **2x b42**, **2x b43**, **2x b44**, **2x b45**, **2x b46**, **2x b47**, **2x b48**, **2x b49**, **2x b50**, **2x b51**, **2x b52**, **2x b53**, **2x b54**, **2x b55**, **2x b56**, **2x b57**, **2x b58**, **2x b59**, **2x b60**, **2x b61**, **2x b62**, **2x b63**, **2x b64**, **2x b65**, **2x b66**, **2x b67**, **2x b68**, **2x b69**, **2x b70**, **2x b71**, **2x b72**, **2x b73**, **2x b74**, **2x b75**, **2x b76**, **2x b77**, **2x b78**, **2x b79**, **2x b80**, **2x b81**, **2x b82**, **2x b83**, **2x b84**, **2x b85**, **2x b86**, **2x b87**, **2x b88**, **2x b89**, **2x b90**, **2x b91**, **2x b92**, **2x b93**, **2x b94**, **2x b95**, **2x b96**, **2x b97**, **2x b98**, **2x b99**, **2x b100**.

Side View: Shows the profile of the lead tip. Key dimensions include H , L , L_1 , L_2 , L_3 , L_4 , L_5 , L_6 , L_7 , L_8 , L_9 , L_{10} , L_{11} , L_{12} , L_{13} , L_{14} , L_{15} , L_{16} , L_{17} , L_{18} , L_{19} , L_{20} , L_{21} , L_{22} , L_{23} , L_{24} , L_{25} , L_{26} , L_{27} , L_{28} , L_{29} , L_{30} , L_{31} , L_{32} , L_{33} , L_{34} , L_{35} , L_{36} , L_{37} , L_{38} , L_{39} , L_{40} , L_{41} , L_{42} , L_{43} , L_{44} , L_{45} , L_{46} , L_{47} , L_{48} , L_{49} , L_{50} , L_{51} , L_{52} , L_{53} , L_{54} , L_{55} , L_{56} , L_{57} , L_{58} , L_{59} , L_{60} , L_{61} , L_{62} , L_{63} , L_{64} , L_{65} , L_{66} , L_{67} , L_{68} , L_{69} , L_{70} , L_{71} , L_{72} , L_{73} , L_{74} , L_{75} , L_{76} , L_{77} , L_{78} , L_{79} , L_{80} , L_{81} , L_{82} , L_{83} , L_{84} , L_{85} , L_{86} , L_{87} , L_{88} , L_{89} , L_{90} , L_{91} , L_{92} , L_{93} , L_{94} , L_{95} , L_{96} , L_{97} , L_{98} , L_{99} , L_{100} . Key features include **DATUM A**, <

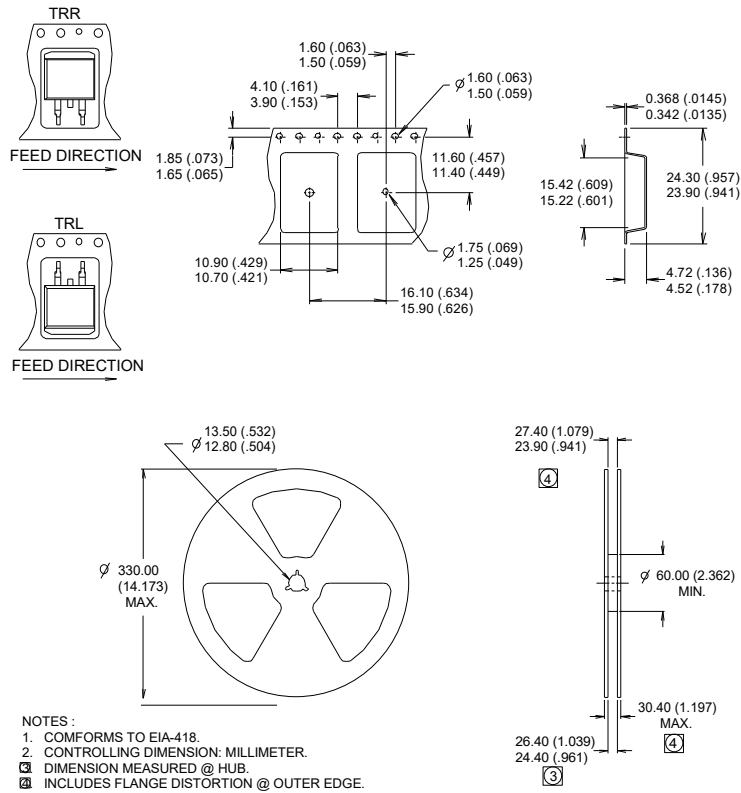
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	3
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25	BSC	.010	BSC	

1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

Diagram illustrating the identification codes on the F530S diode package:

- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo on the package.
- PART NUMBER**: Points to the F530S marking.
- DATE CODE**: Points to the P002A marking.
- P = DESIGNATES LEAD - FREE PRODUCT (OPTIONAL)**: Explains the meaning of the letter P in the date code.
- YEAR 0 = 2000**: Explains the meaning of the digit 0 in the date code.
- WEEK 02**: Explains the meaning of the digits 02 in the date code.
- A = ASSEMBLY SITE CODE**: Explains the meaning of the letter A in the date code.
- ASSEMBLY LOT CODE**: Points to the 80 marking.

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))



Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-220	N/A
	D ² Pak	MSL 1
	TO-262	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site: <https://www.infineon.com/>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
2026-08-10	2.1	• Update datasheet to Infineon format • Updated Package Outline and Part marking –page 9 • Added disclaimer on last page.

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