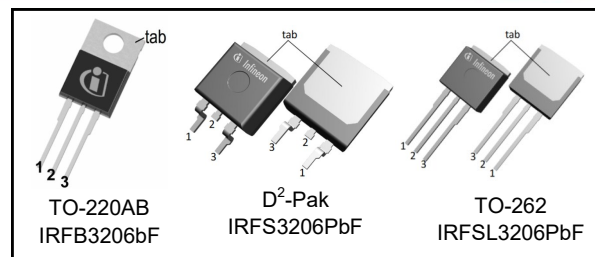
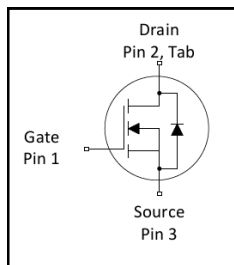


$V_{(BR)DSS}$	60V
$R_{DS(on)}$ typ.	2.4m Ω
max.	3.0m Ω
I_D (Silicon Limited)	210A ^①
I_D (Package Limited)	120A



Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead-Free
- RoHS Compliant, Halogen-Free

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB3206PbF	TO-220	Tube	50	IRFB3206PbF
IRFS3206PbF	D²-Pak	Tape and Reel	800	IRFS3206PbF
IRFSL3206PbF	TO-262	Tube	50	IRFSL3206PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	210 ^①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	150 ^①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ^②	840	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ^④	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Avalanche Characteristics

E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ^③	170	mJ
I_{AR}	Avalanche Current ^②	See Fig.14,15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ^⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑥	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface, TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ^⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount), D² Pak ^{⑧⑨}	—	40	

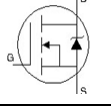
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.4	3.0	m Ω	$V_{GS} = 10V, I_D = 75A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	0.7	—	Ω	

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

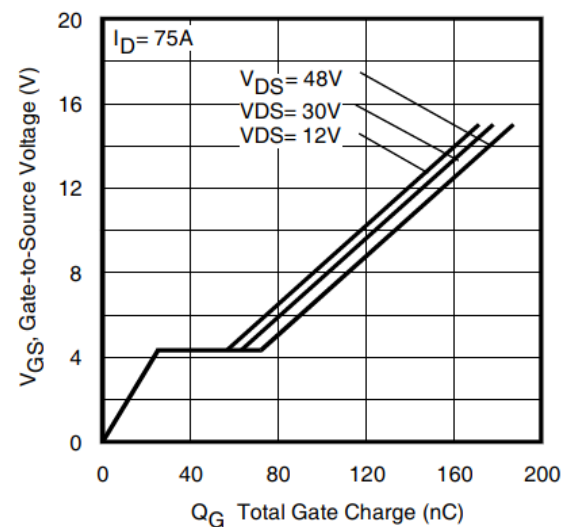
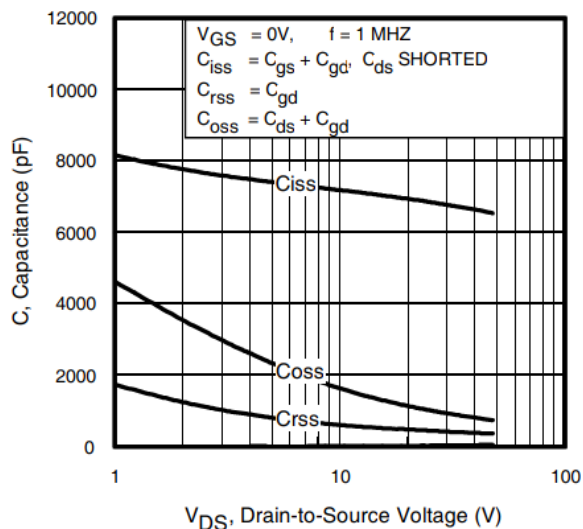
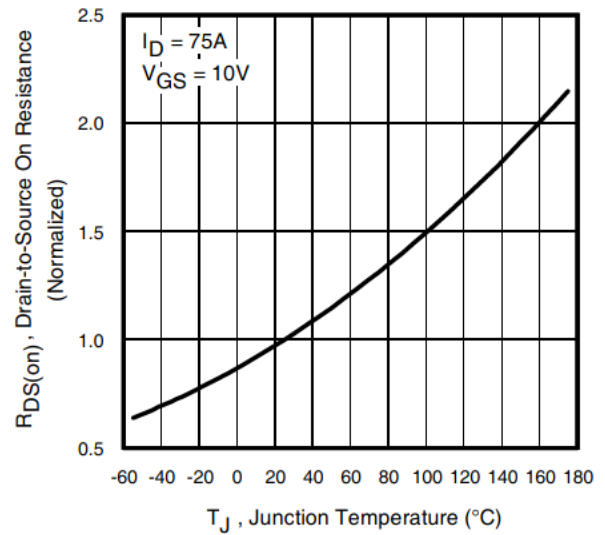
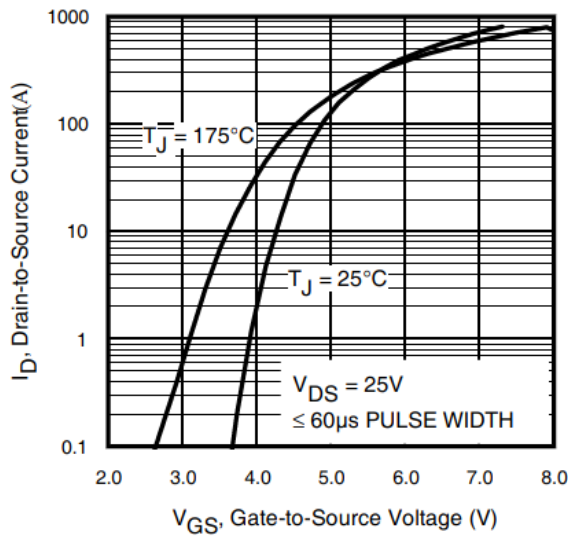
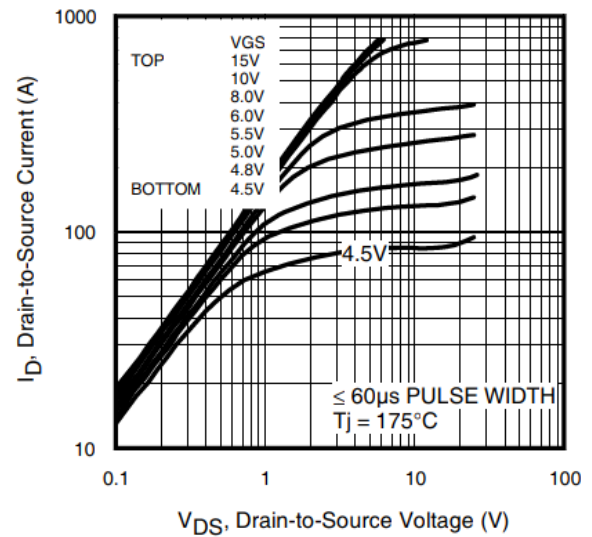
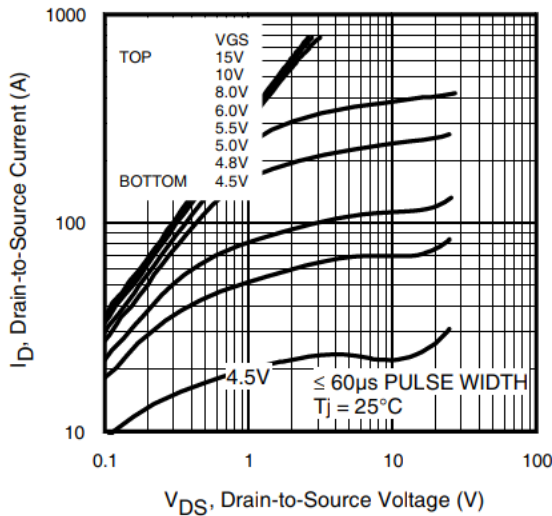
gfs	Forward Trans conductance	210	—	—	S	$V_{DS} = 50V, I_D = 75A$
Q_g	Total Gate Charge	—	120	170	nC	$I_D = 75A$
Q_{gs}	Gate-to-Source Charge	—	29	—		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain Charge	—	35	—		$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	85	—		$I_D = 75A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	$V_{DD} = 30V$
t_r	Rise Time	—	82	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	83	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	6540	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	720	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	360	—		$f = 1.0MHz$, See Fig. 5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	1040	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑦
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	1230	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑧

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	210 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	840		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	33	50	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51V$
		—	37	56		$T_J = 125^\circ\text{C}$ $I_F = 75A$,
Q_{rr}	Reverse Recovery Charge	—	41	62	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	53	80		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.1	—	A	$T_J = 25^\circ\text{C}$

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A. Note that Current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.023mH$, $R_G = 25\Omega$, $I_{AS} = 120A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 75A$, $di/dt \leq 360/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note# [AN-994](#).
- ⑨ R_G is measured at T_J approximately 90°C .



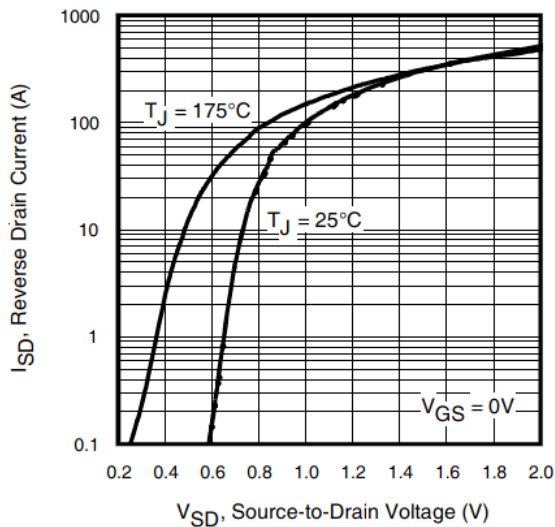


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

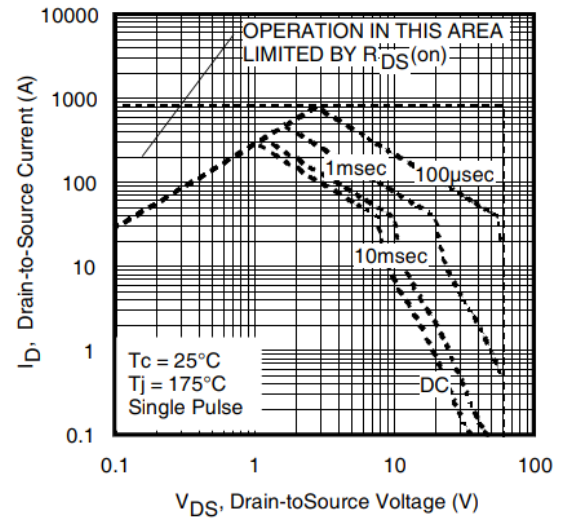


Fig. 8. Maximum Safe Operating Area

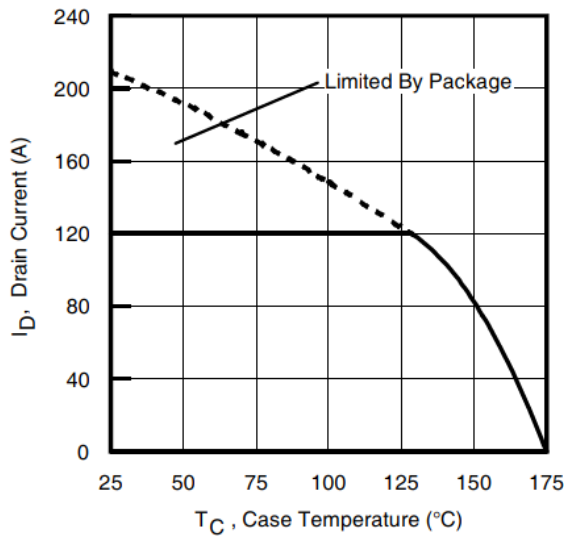


Fig 9. Maximum Drain Current vs. Case Temperature

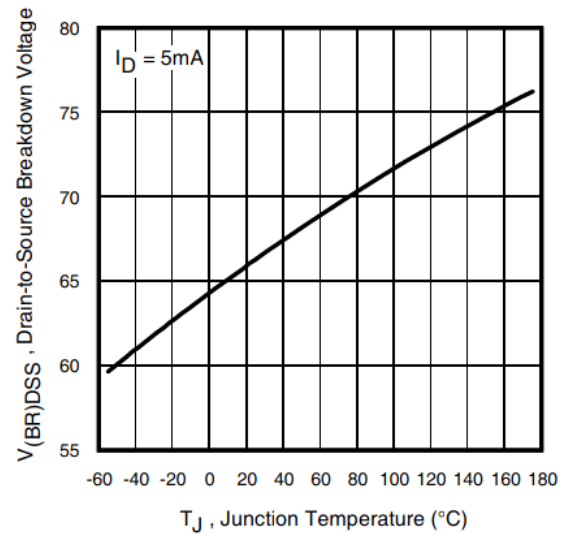


Fig 10. Drain-to-Source Breakdown Voltage

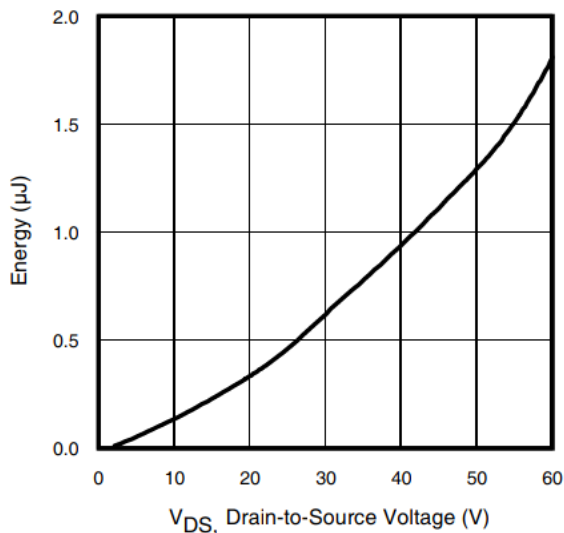


Fig 11. Typical Coss Stored Energy

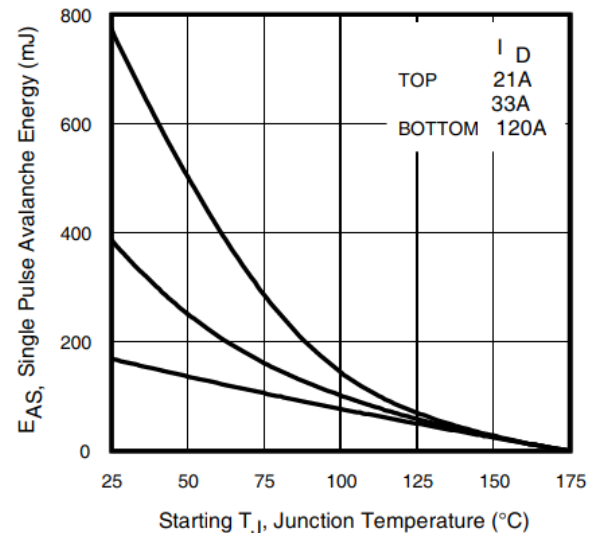


Fig 12. Maximum Avalanche Energy vs. Drain Current

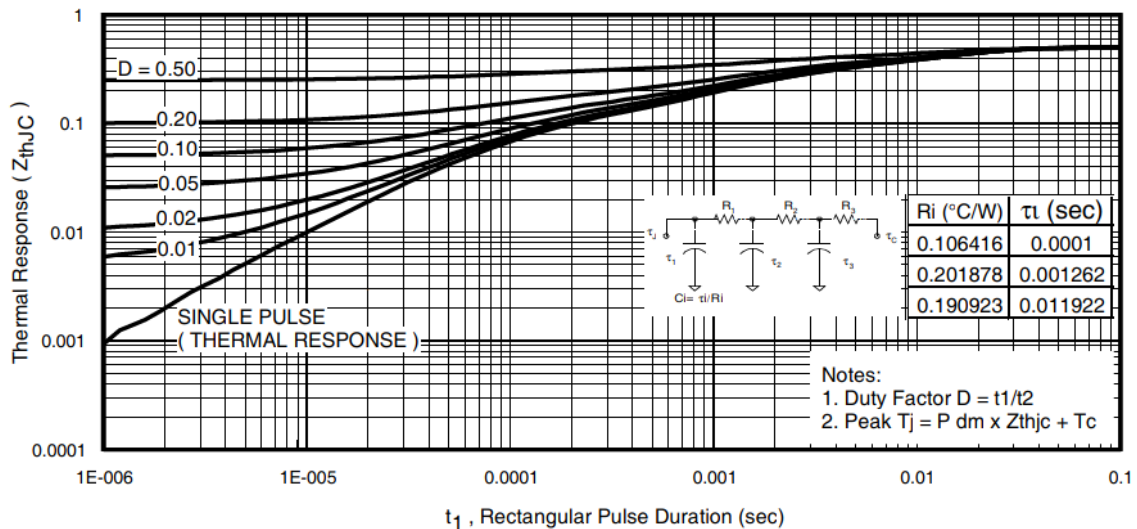


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

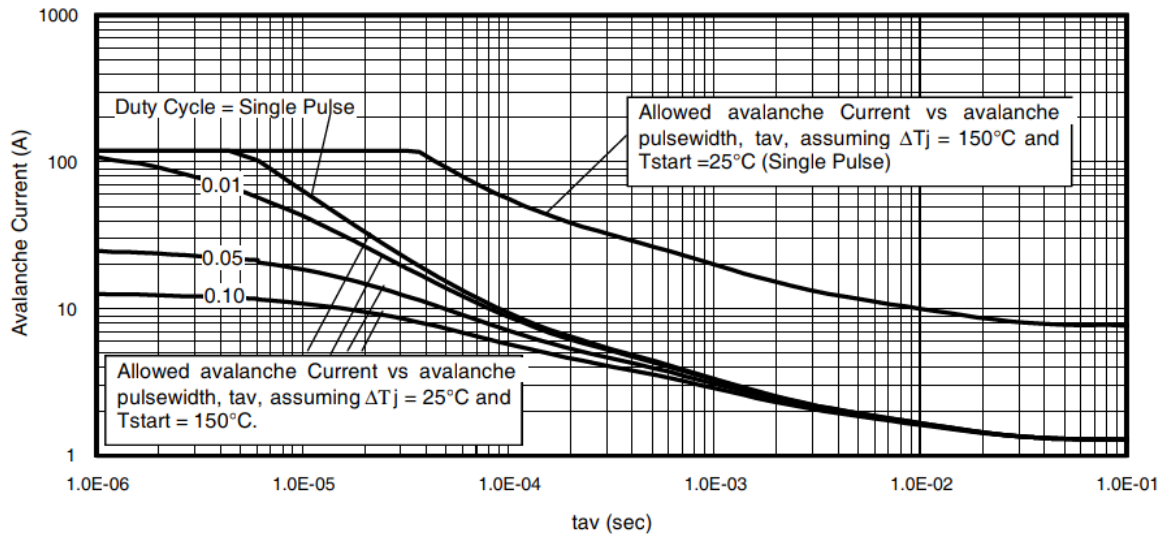


Fig 14. Avalanche Current vs. Pulse width

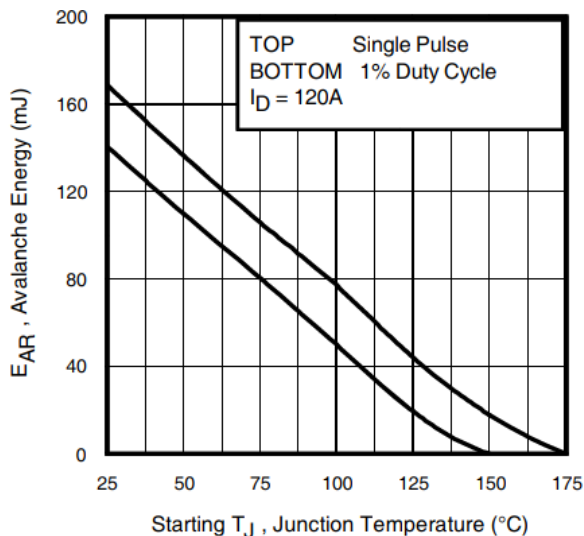


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thjc}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thjc}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thj}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

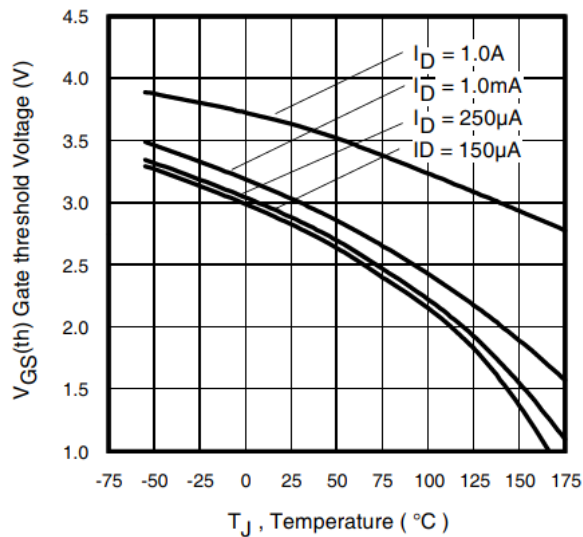


Fig 16. Threshold Voltage vs. Temperature

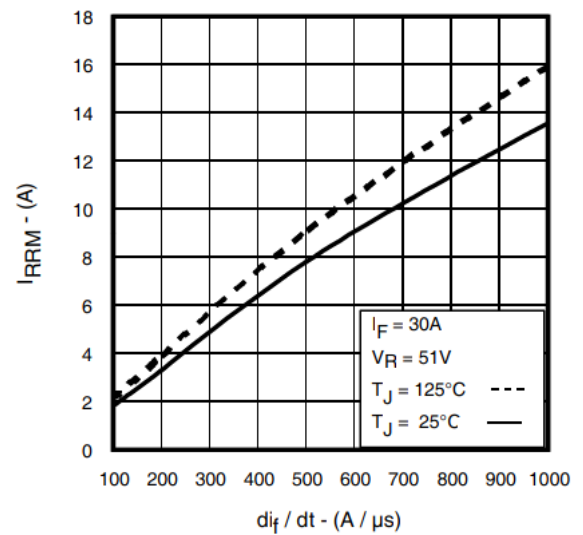


Fig. 17 - Typical Recovery Current vs. di/dt

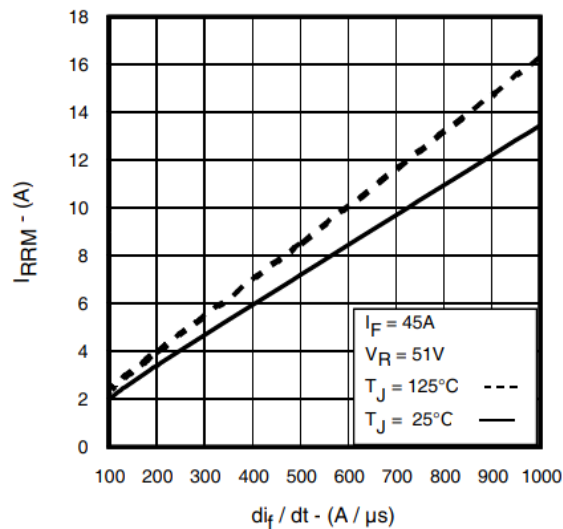


Fig. 18 - Typical Recovery Current vs. di/dt

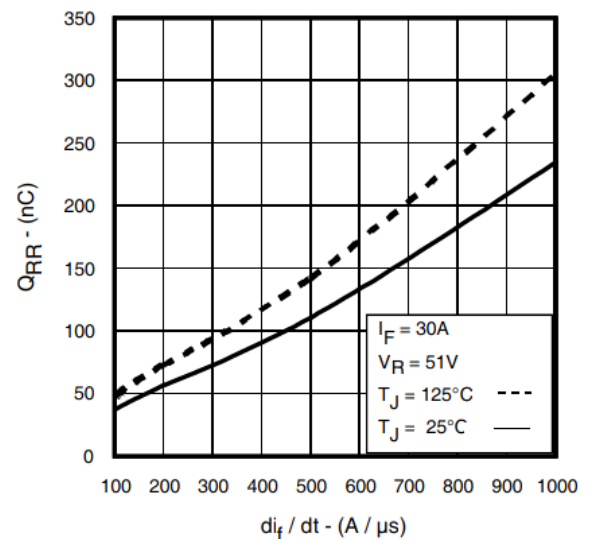


Fig. 19 - Typical Stored Charge vs. di/dt

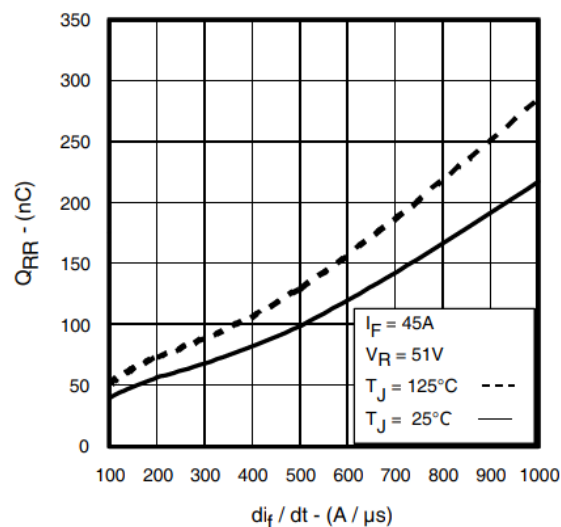
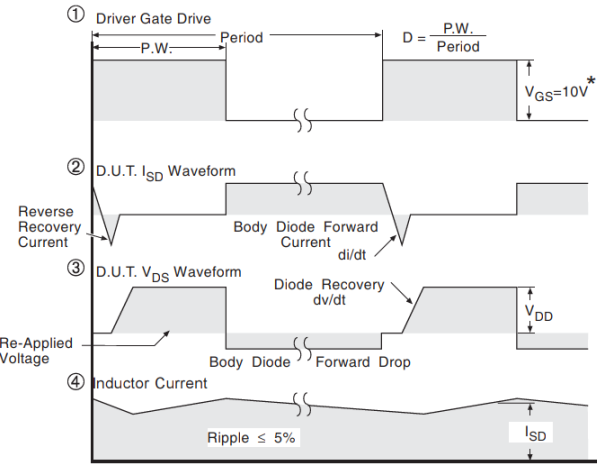
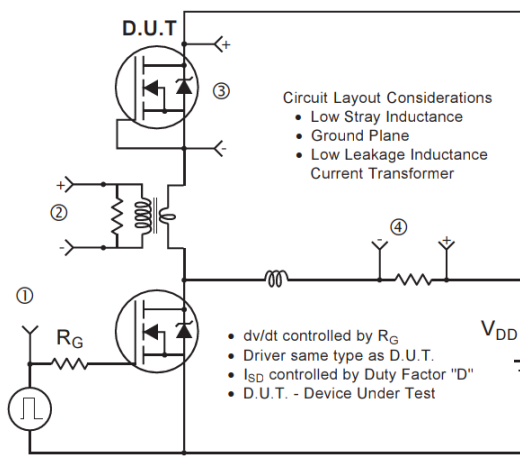


Fig. 20 - Typical Stored Charge vs. di/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

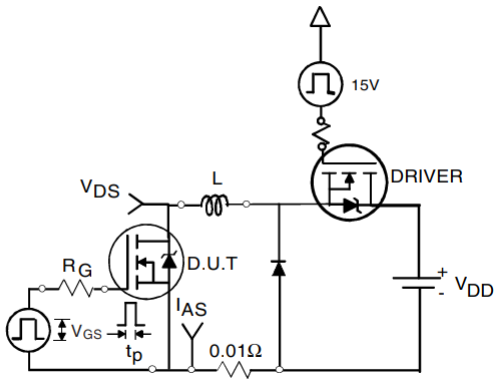


Fig 22a. Unclamped Inductive Test Circuit

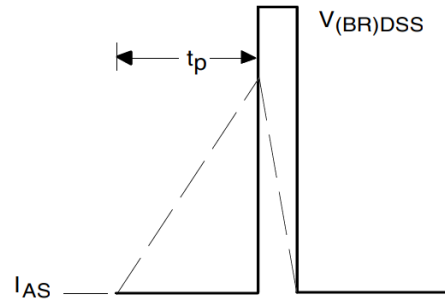


Fig 22b. Unclamped Inductive Waveforms

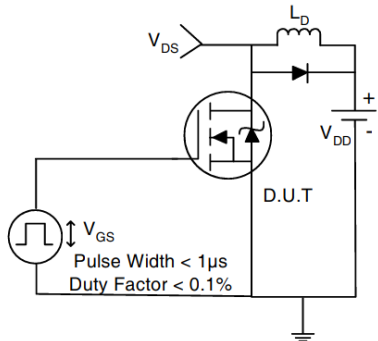


Fig 23a. Switching Time Test Circuit

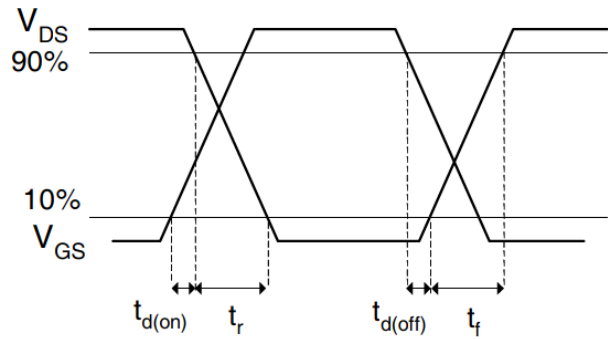


Fig 23b. Switching Time Waveforms

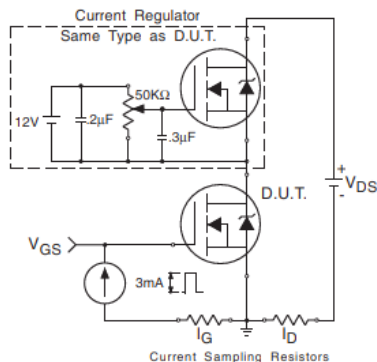


Fig 24a. Gate Charge Test Circuit

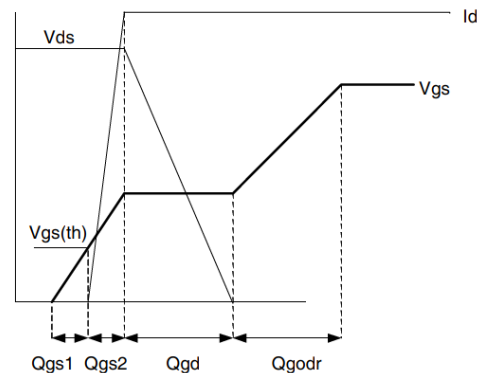
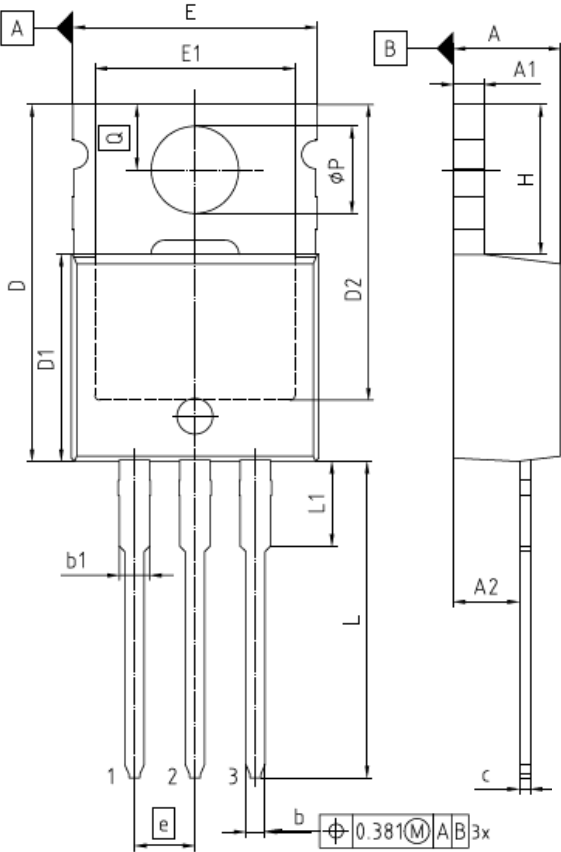


Fig 24b. Gate Charge Waveform

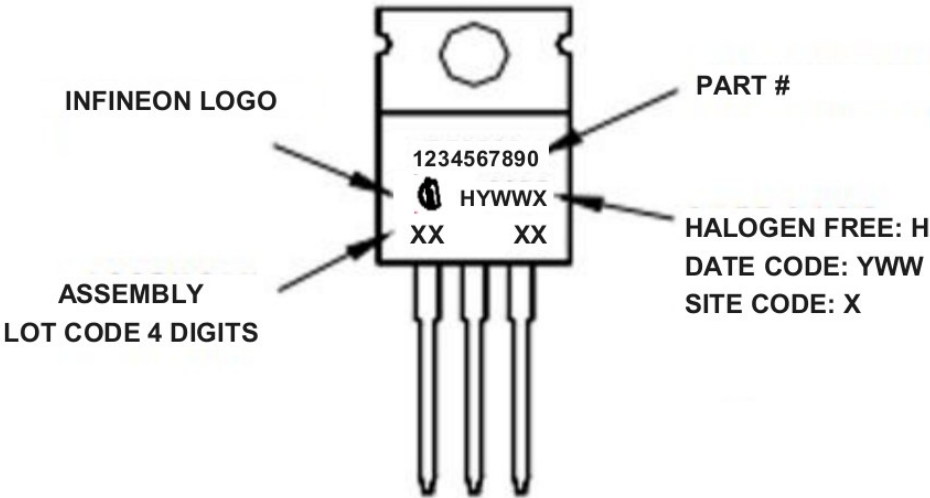
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

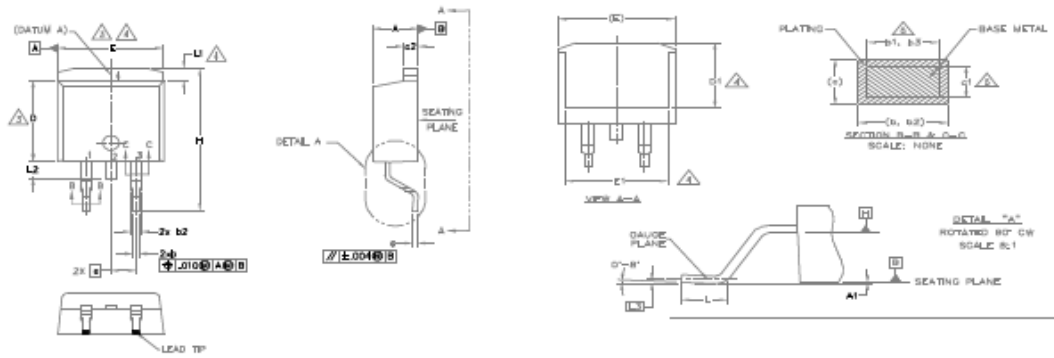
PACKAGE - GROUP NUMBER: PG-TO220-3-U05		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

D² Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

LEAD ASSIGNMENTS

DIODES

- 1.— ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.— CATHODE
- 3.— ANODE

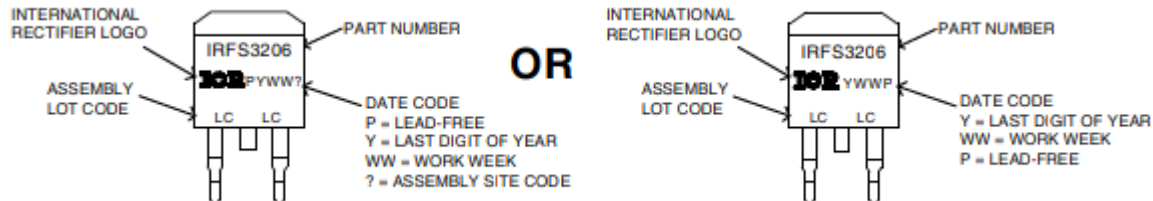
HEXFET

- 1.— GATE
- 2, 4.— DRAIN
- 3.— SOURCE

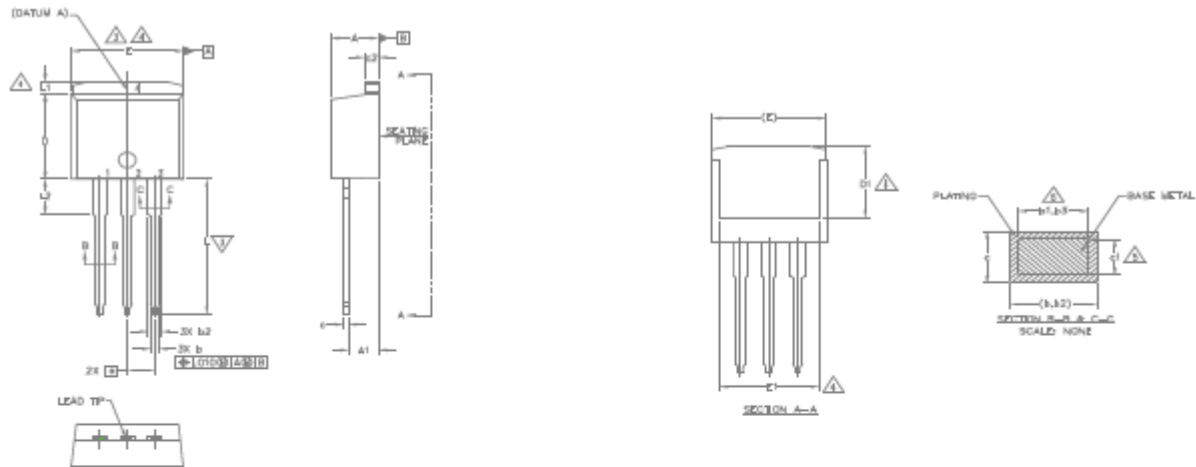
IGBTs, CoPACK

- 1.— GATE
- 2, 4.— COLLECTOR
- 3.— EMITTER

D² Pak (TO-263AB) Part Marking Information



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.), AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

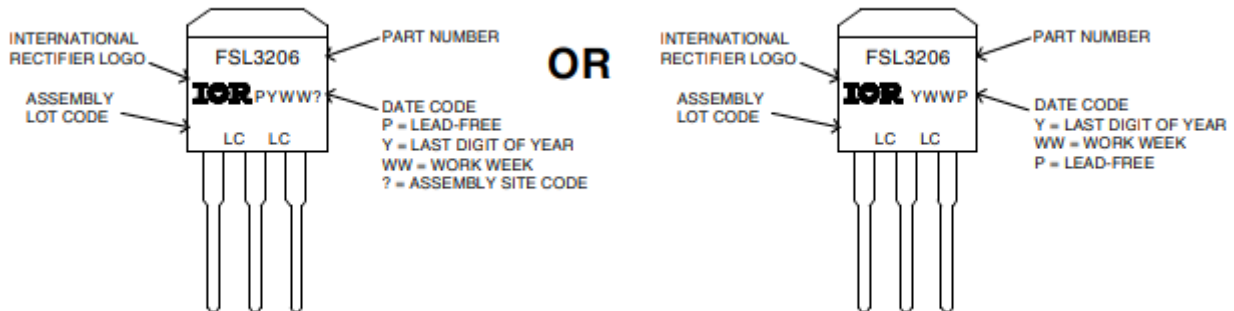
HEXRET

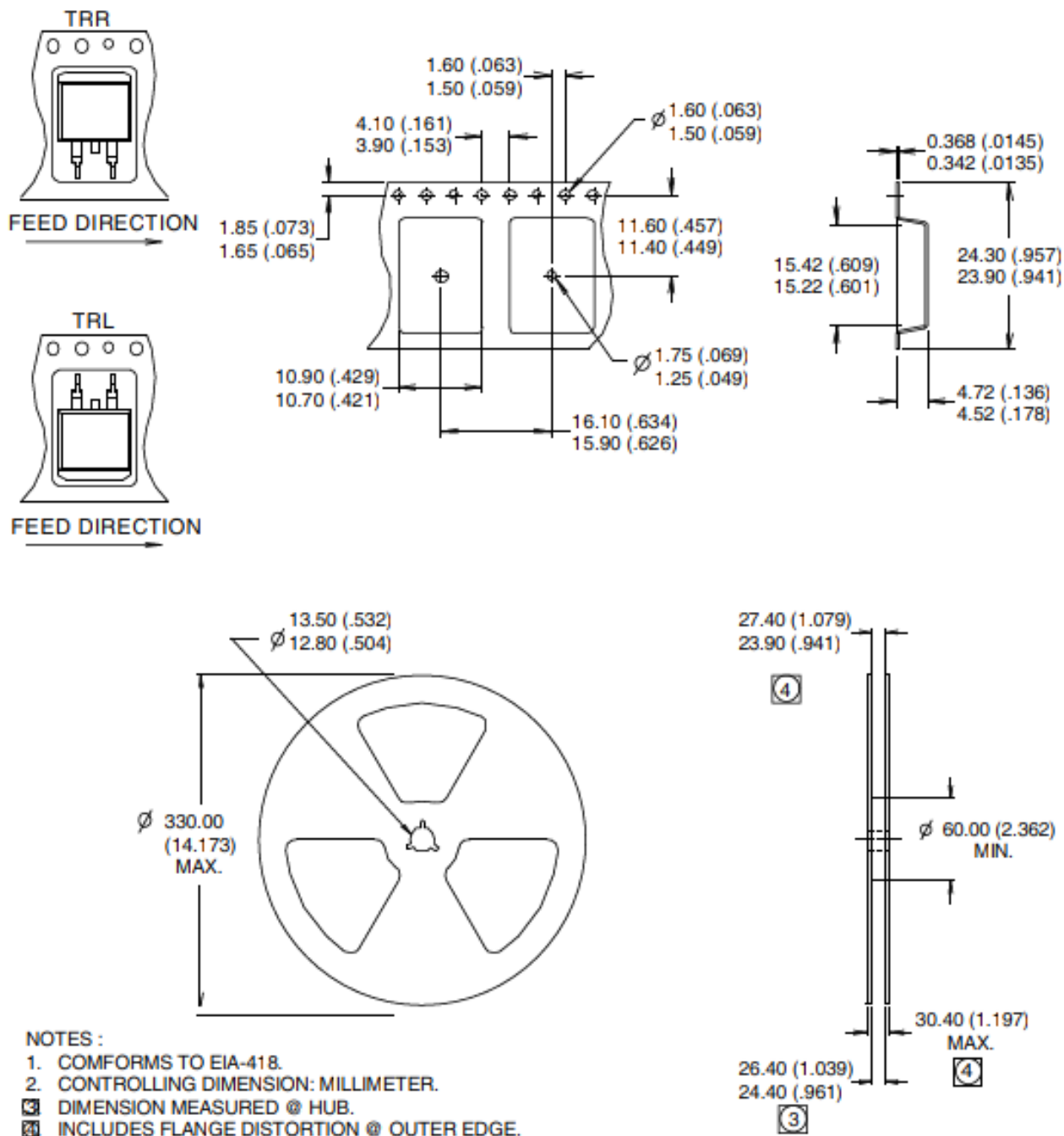
1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIODES

1. ANODE (TWO DIE) / OPEN (ONE DIE)
2. CATHODE
3. ANODE

TO-262 Part Marking Information



D² Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-220	N/A
	D2-Pak	MSL1
	TO-262	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <https://www.infineon.com/>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
2026-09-15	2.1	• Update datasheet to Infineon format • Updated Package Outline and Part marking –page 8 • Added disclaimer on last page.

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