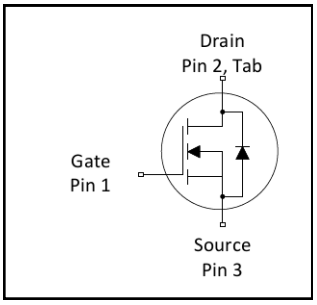
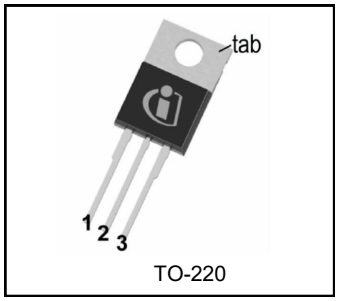
IRFB7546PbF

$V_{(BR)DSS}$	60V
$R_{DS(on)}$ typ.	6.0mΩ
max.	7.3mΩ
$I_{D\ (Silicon\ Limited)}$	75A





G	D	S
Gate	Drain	Source

Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- RoHS Compliant, Halogen-Free*

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB7546PbF	TO-220	Tube	50	IRFB7546PbF

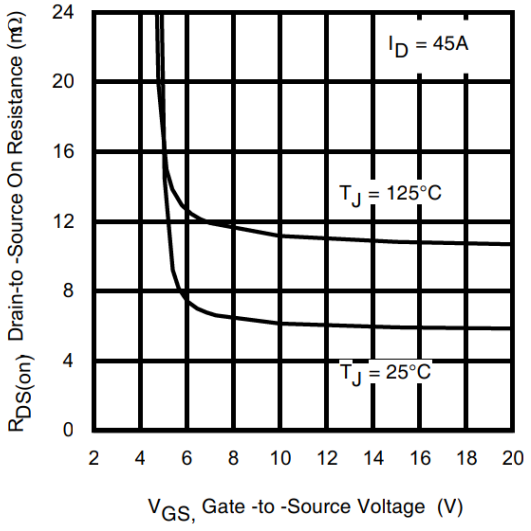


Fig 1. Typical On-Resistance vs. Gate Voltage

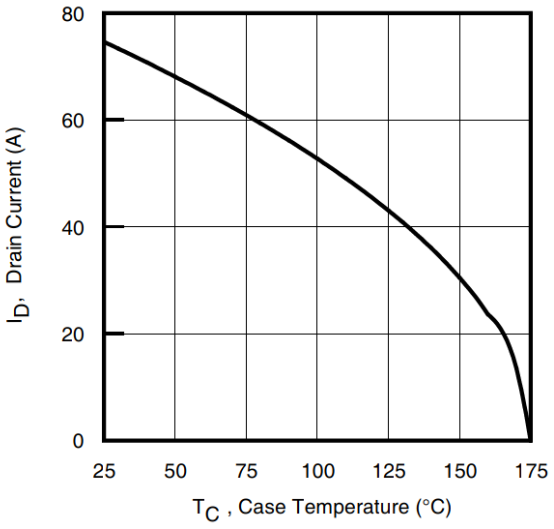


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	75	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	53	
I_{DM}	Pulsed Drain Current ①	300	
P_D @T_C = 25°C	Maximum Power Dissipation	99	W
	Linear Derating Factor	0.7	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	110	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑨	170	
I_{AR}	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	–––	1.52	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	62	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	46	–––	mV/°C	Reference to 25°C, I_D = 1mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	6.0	7.3	mΩ	V_{GS} = 10V, I_D = 45A
		–––	7.5	–––		V_{GS} = 6.0V, I_D = 23A
$V_{GS(th)}$	Gate Threshold Voltage	2.1	–––	3.7	V	V_{DS} = V_{GS}, I_D = 100µA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	µA	V_{DS} =60 V, V_{GS} = 0V
		–––	–––	150		V_{DS} =60V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
R_G	Gate Resistance	–––	1.6	–––	Ω	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 110µH, R_G = 50Ω, I_{AS} = 45A, V_{GS} =10V.

③ $I_{SD} \leq$ 100A, di/dt ≤ 1260A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ R_θ is measured at T_J approximately 90°C.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 19A, V_{GS} =10V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	150	—	—	S	V_{DS} = 10V, I_D = 45A
Q_g	Total Gate Charge	—	58	87	nC	I_D = 45A
Q_{gs}	Gate-to-Source Charge	—	14	—		V_{DS} = 30V
Q_{gd}	Gate-to-Drain Charge	—	18	—		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Qg– Qgd)	—	40	—		
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = 30V
t_r	Rise Time	—	51	—		I_D = 45A
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		R_G= 2.7Ω
t_f	Fall Time	—	34	—		V_{GS} = 10V④
C_{iss}	Input Capacitance	—	3000	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	280	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	180	—		f = 1.0MHz, See Fig.7
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	290	—		V_{GS} = 0V, VDS = 0V to 48V⑥
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	370	—		V_{GS} = 0V, VDS = 0V to 48V⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	300		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C,I_S = 45A,V_{GS} = 0V ④
dv/dt	Peak Diode Recovery dv/dt③	—	7.9	—	V/ns	T_J = 175°C,I_S = 45A,V_{DS} = 60V
t_{rr}	Reverse Recovery Time	—	29	—	ns	T_J = 25°C V_{DD} = 51V
		—	32	—		T_J = 125°C I_F = 45A,
Q_{rr}	Reverse Recovery Charge	—	33	—	nC	T_J = 25°C di/dt = 100A/µs ④
		—	40	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	1.9	—	A	T_J = 25°C

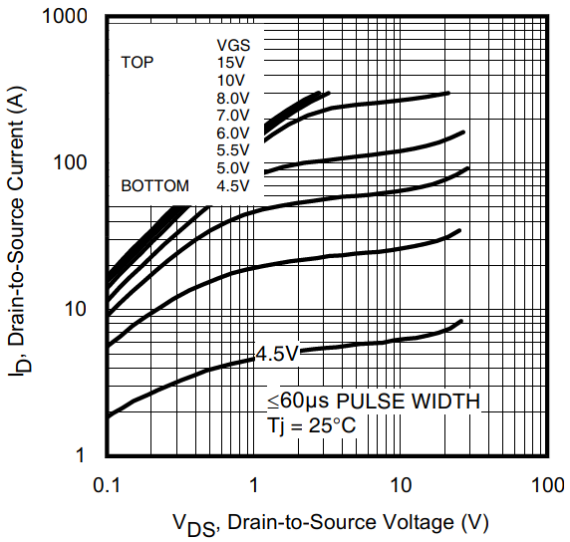


Fig 3. Typical Output Characteristics

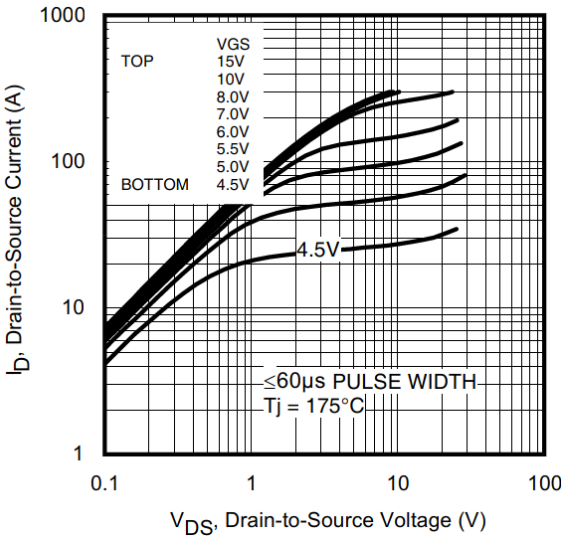


Fig 4. Typical Output Characteristics

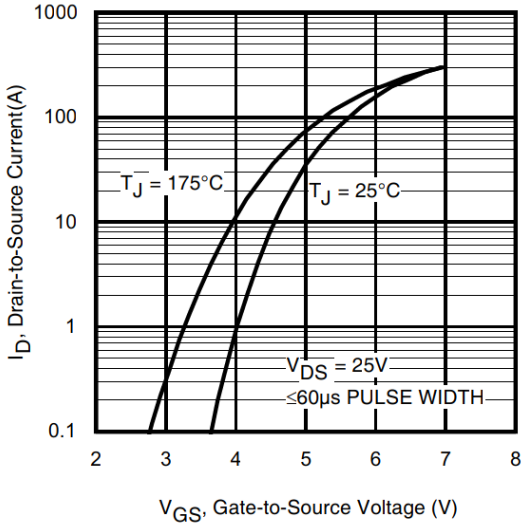


Fig 5. Typical Transfer Characteristics

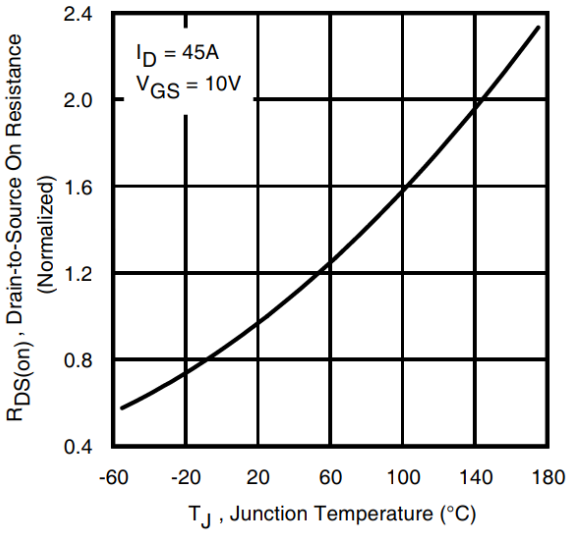


Fig 6. Normalized On-Resistance vs. Temperature

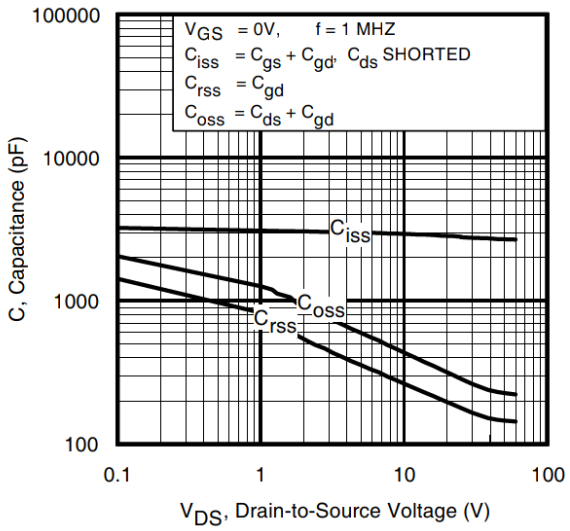


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

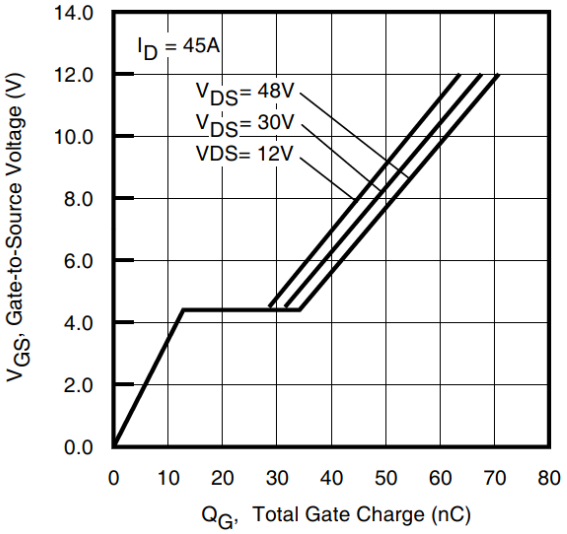


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

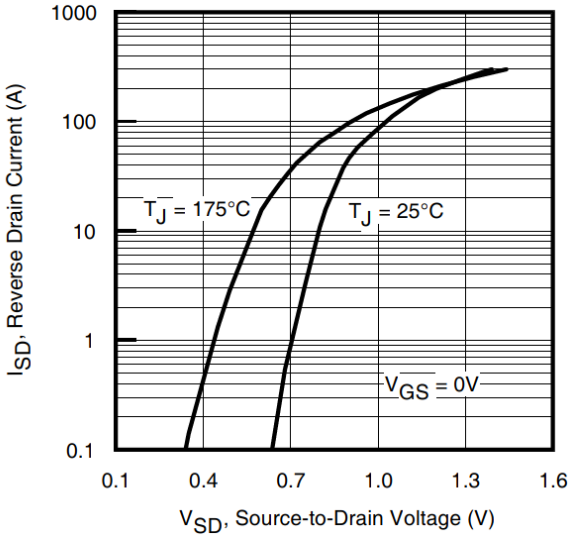


Fig 9. Typical Source-Drain Diode Forward Voltage

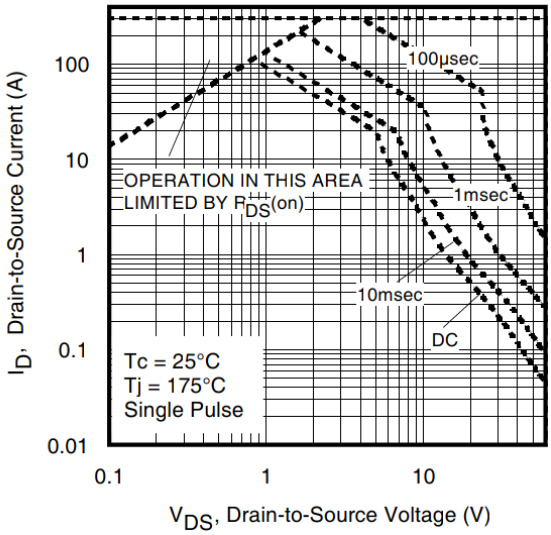


Fig 10. Maximum Safe Operating Area

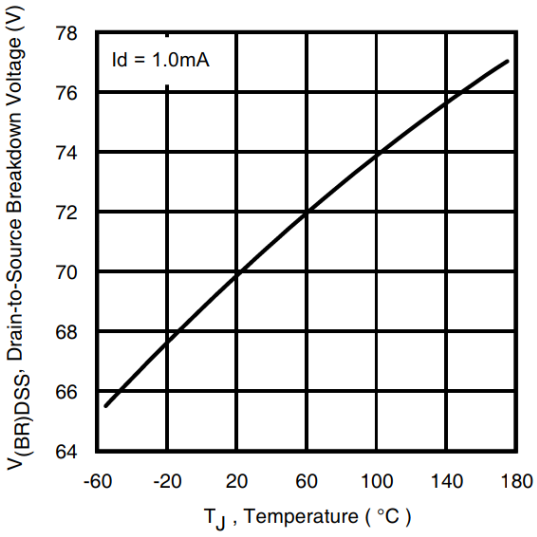


Fig 11. Drain-to-Source Breakdown Voltage

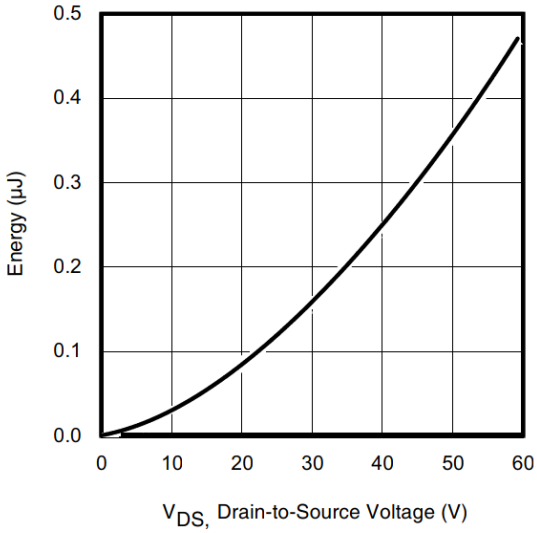


Fig 12. Typical C_{oss} Stored Energy

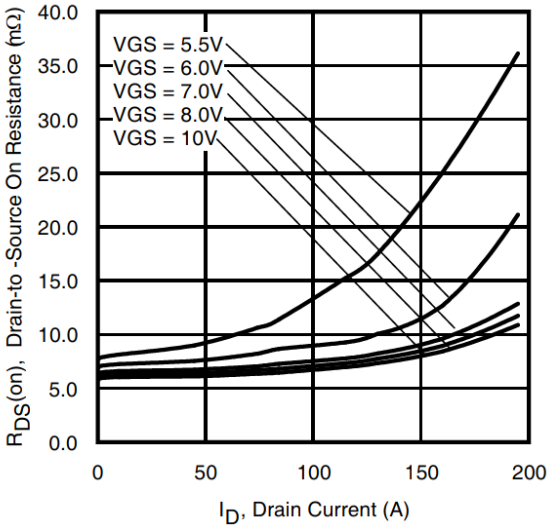


Fig 13. Typical On-Resistance vs. Drain Current

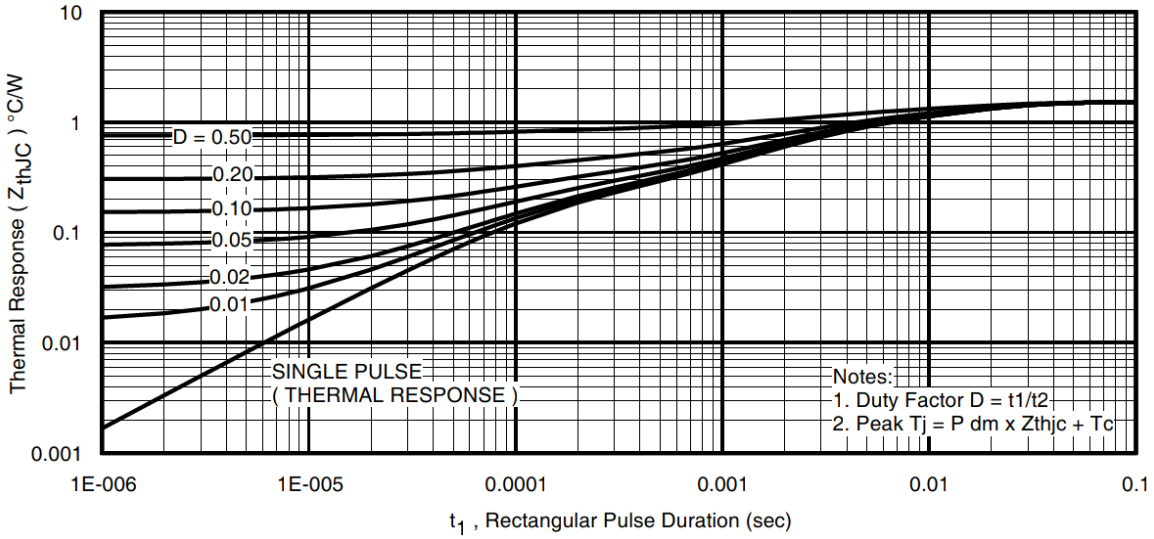


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

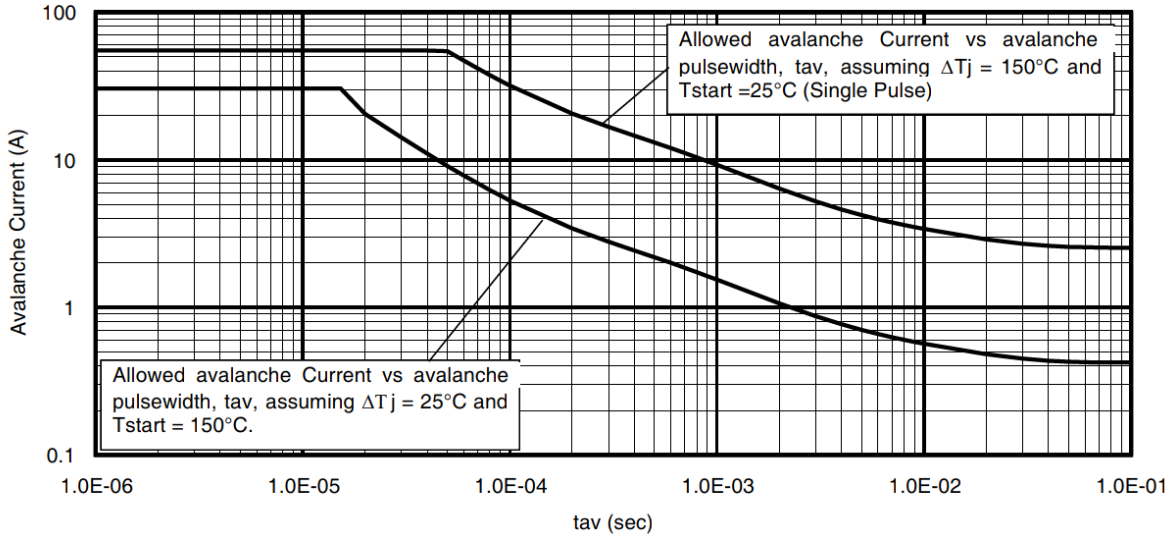


Fig 15. Typical Avalanche Current vs. Pulse Width

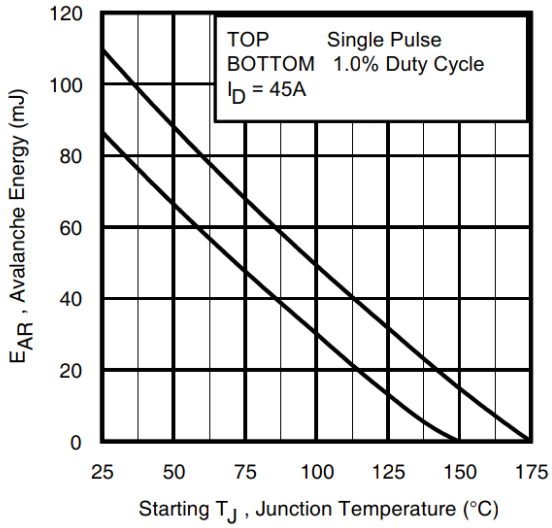


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
   PD (ave) = 1/2 (1.3·BV·I_{av}) = $\Delta T/ Z_{thJC}$
   $I_{av} = 2\Delta T/ [1.3 \cdot BV \cdot Z_{th}]$
   $E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$

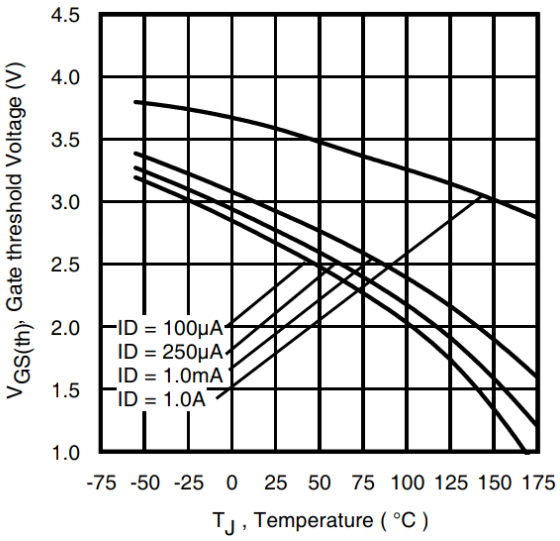


Fig 17. Threshold Voltage vs. Temperature

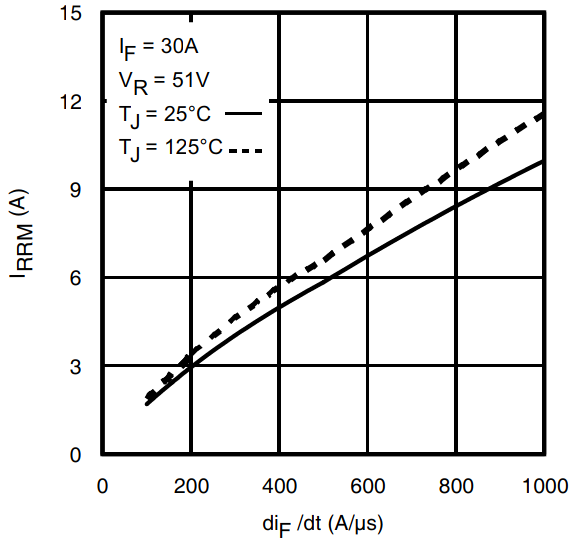


Fig 18. Typical Recovery Current vs. dif/dt

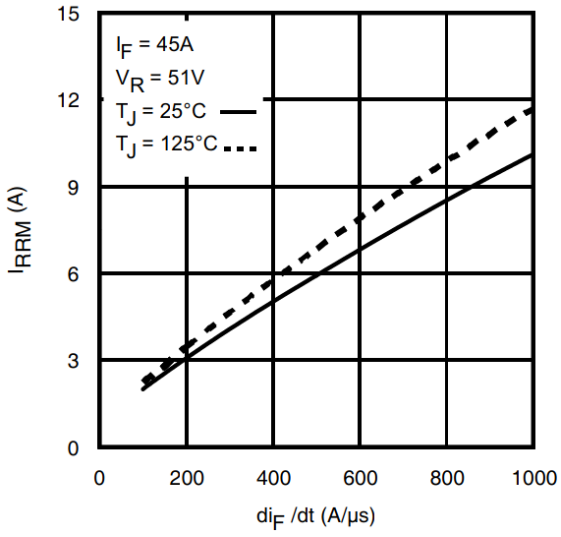


Fig 19. Typical Recovery Current vs. dif/dt

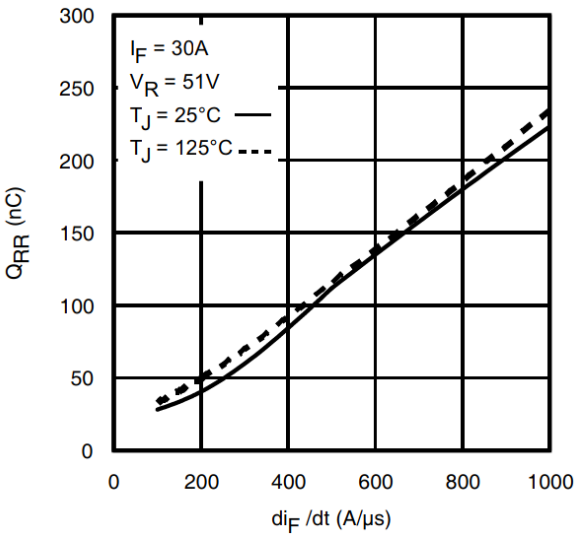


Fig 20. Typical Stored Charge vs. dif/dt

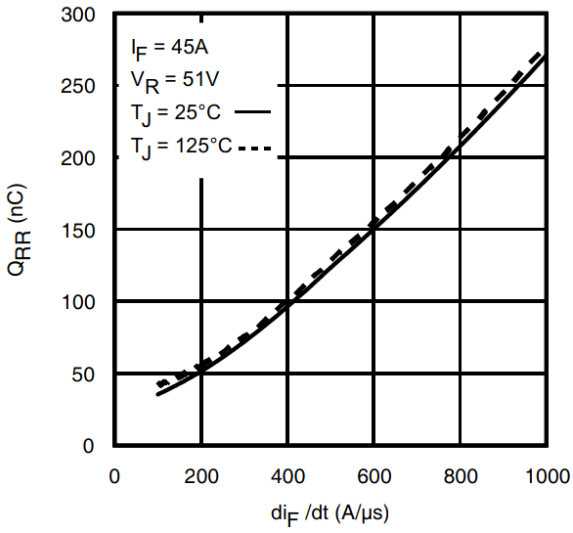


Fig 21. Typical Stored Charge vs. dif/dt

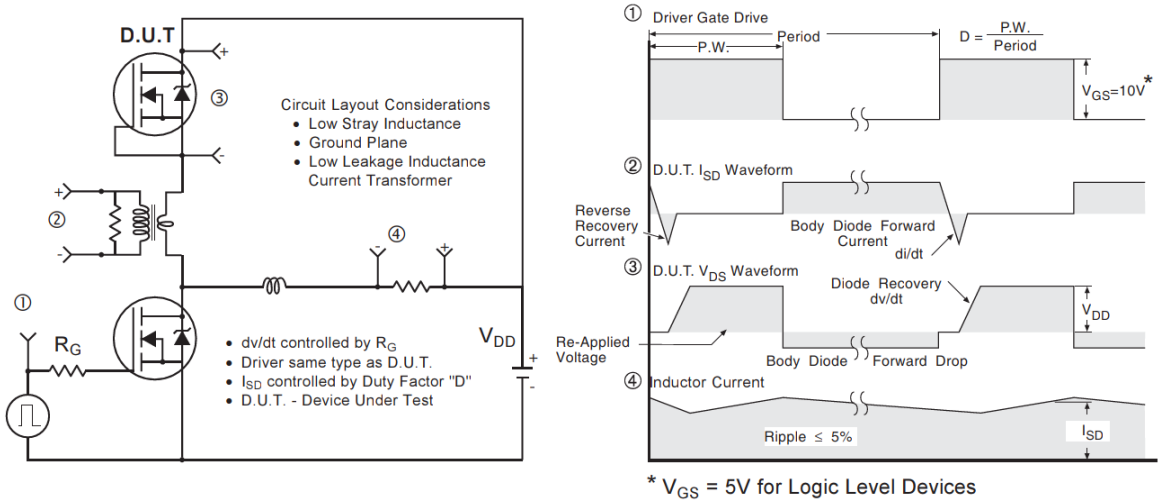


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

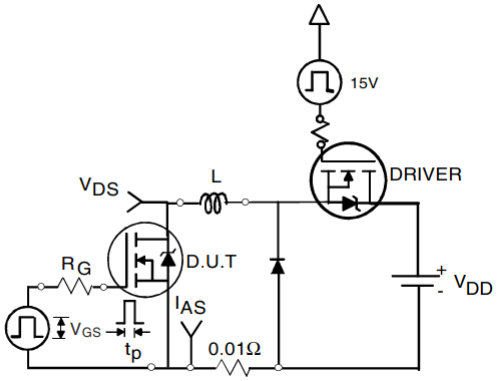


Fig 23a. Unclamped Inductive Test Circuit

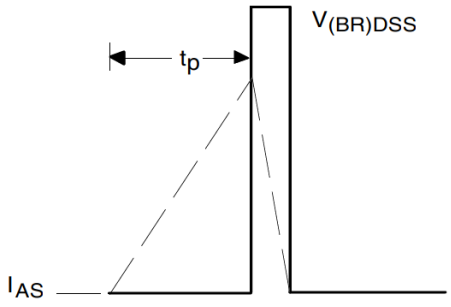


Fig 23b. Unclamped Inductive Waveforms

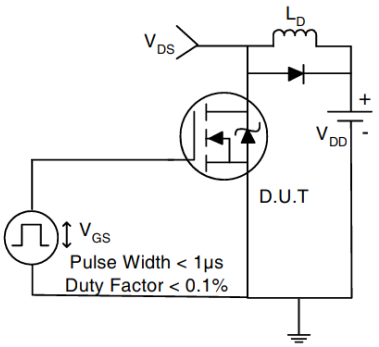


Fig 24a. Switching Time Test Circuit

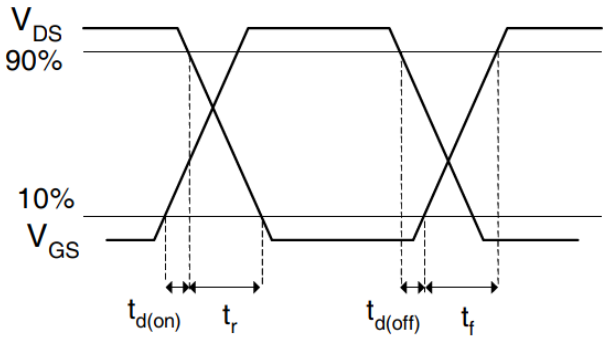


Fig 24b. Switching Time Waveforms

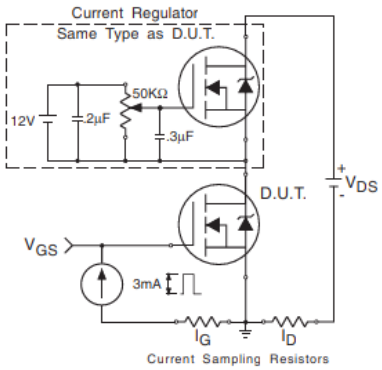


Fig 25a. Gate Charge Test Circuit

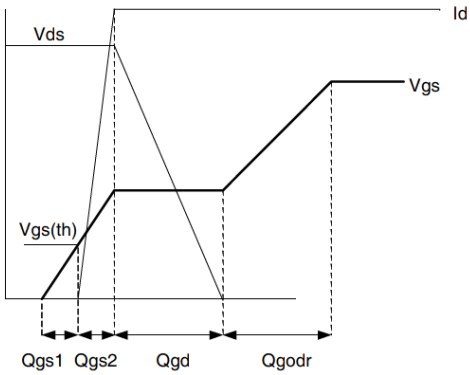
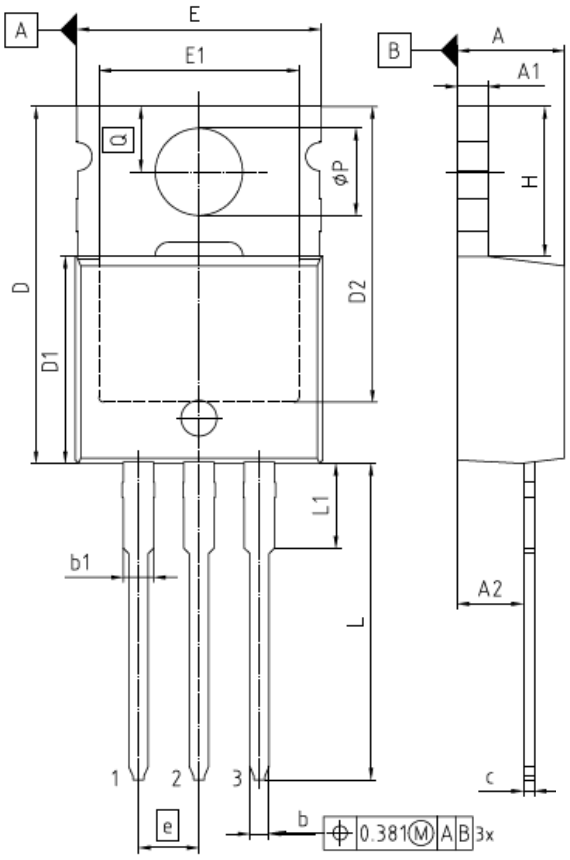


Fig 25b. Gate Charge Waveform

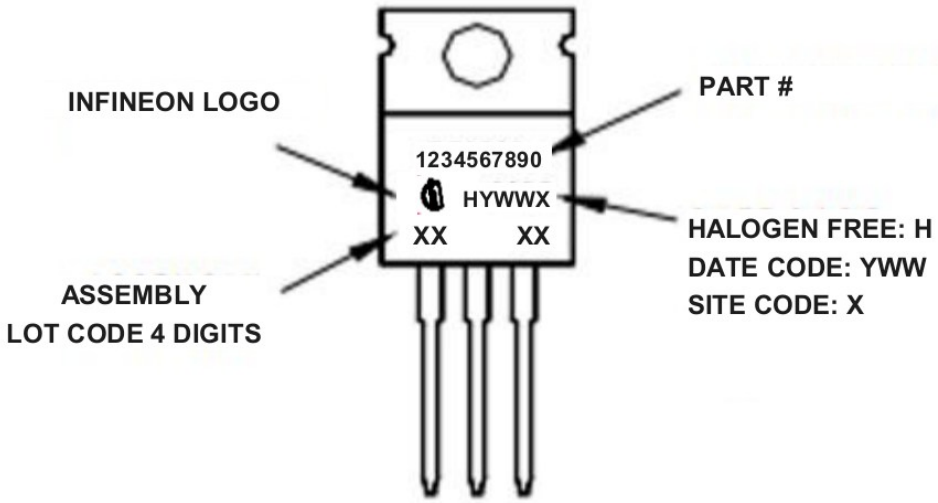
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER:	PG-TO220-3-U05	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	TO-220	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: https://www.infineon.com/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
2026-09-18	2.1	• Update datasheet to Infineon format • Updated Package Outline and Part marking –page 8 • Added disclaimer on last page.

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