

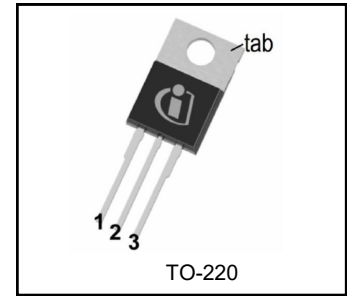
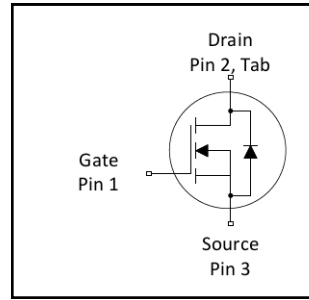
V_{DS} max	150V
R_{DS(ON)} typ. @ 10V	32mΩ
Q_g typ.	26nC
Q_{SW} typ.	11nC
R_{G(int)} typ	2.7Ω
T_J max	175°C

Features

- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low R_{DS(ON)} for Improved Efficiency
- Low Q_G and Q_{SW} for Better THD and Improved Efficiency
- Low Q_{RR} for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Can Deliver up to 300W per Channel into 4Ω Load in Half-Bridge Configuration Amplifier

Description

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MOSFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for ClassD audio amplifier applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB5615PbF	TO-220	Tube	50	IRFB5615PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	150	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	35	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	25	
I _{DM}	Pulsed Drain Current ①	140	
P _D @ T _C = 25°C	Power Dissipation ③	144	W
P _D @ T _C = 100°C	Power Dissipation	72	
	Linear Derating Factor	0.96	W/°C
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

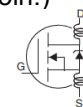
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ④	—	1.045	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient ④	—	62	

Notes ① through ⑥ are on page 7

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	32	39	m Ω	$V_{GS} = 10V, I_D = 21A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	—	-13	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
gfs	Forward Trans conductance	35	—	—	S	$V_{DS} = 50V, I_D = 21A$
Q_g	Total Gate Charge	—	26	40	nC	$I_D = 21A,$ $V_{DS} = 75V$ $V_{GS} = 10V$ ③ See Fig. 6 and 19
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	6.4	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	2.2	—		
Q_{gd}	Gate-to-Drain Charge	—	9.0	—		
Q_{godr}	Gate Charge Overdrive	—	8.9	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	11	—		
$R_{G(int)}$	Internal Gate Resistance	—	2.7	5.0	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	8.9	—	ns	$V_{DD} = 75V$ $I_D = 21A$ $R_G = 2.4\Omega$ $V_{GS} = 10V$ ③
t_r	Rise Time	—	23.1	—		
$t_{d(off)}$	Turn-Off Delay Time	—	17.2	—		
t_f	Fall Time	—	13.1	—		
C_{iss}	Input Capacitance	—	1750	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz$, See Fig.5 $V_{GS} = 0V, V_{DS} = 0V$ to $120V$
C_{oss}	Output Capacitance	—	155	—		
C_{rss}	Reverse Transfer Capacitance	—	40	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	175	—		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		



Avalanche Characteristics

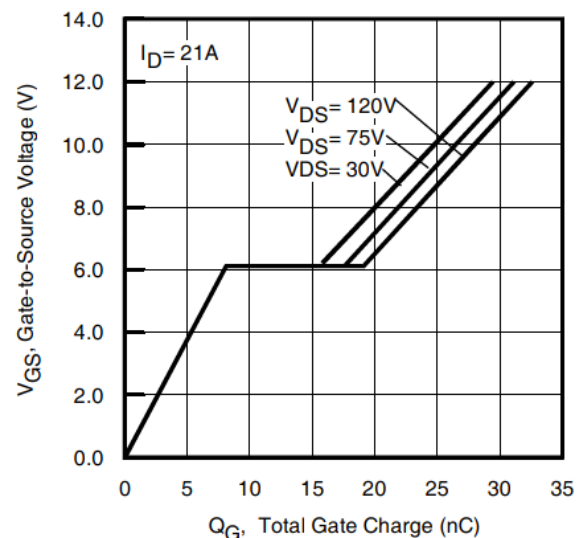
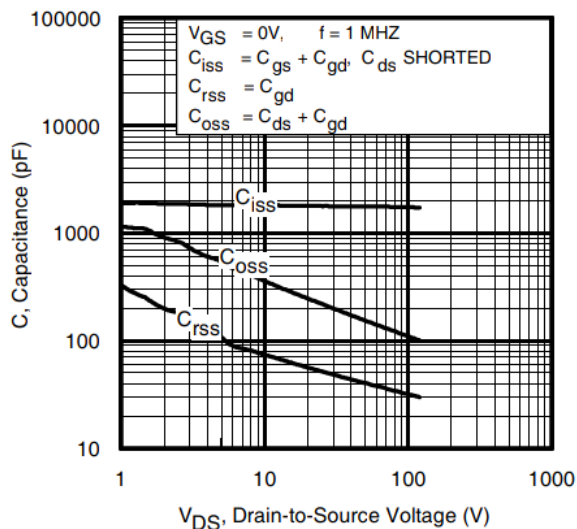
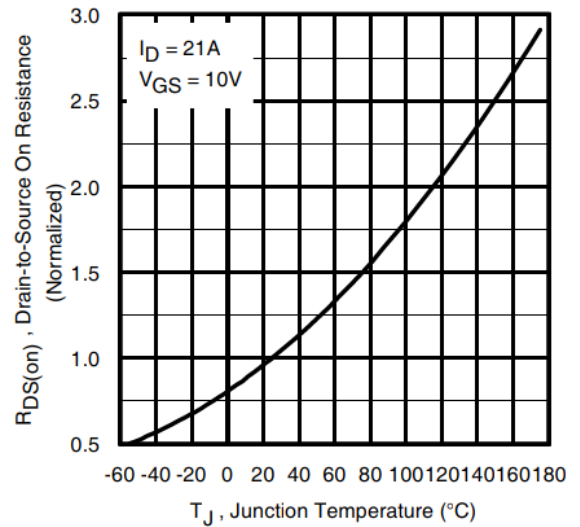
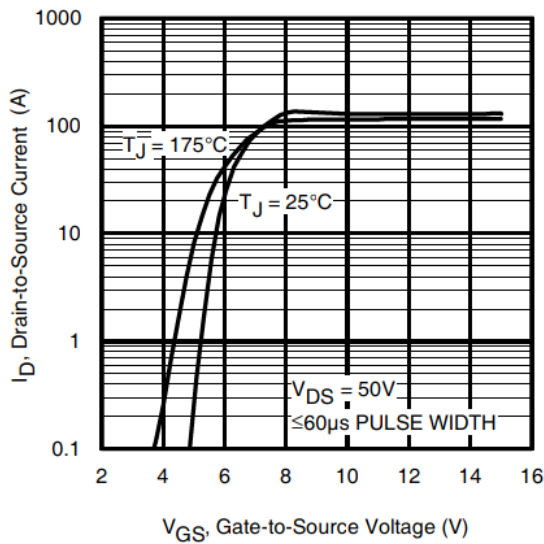
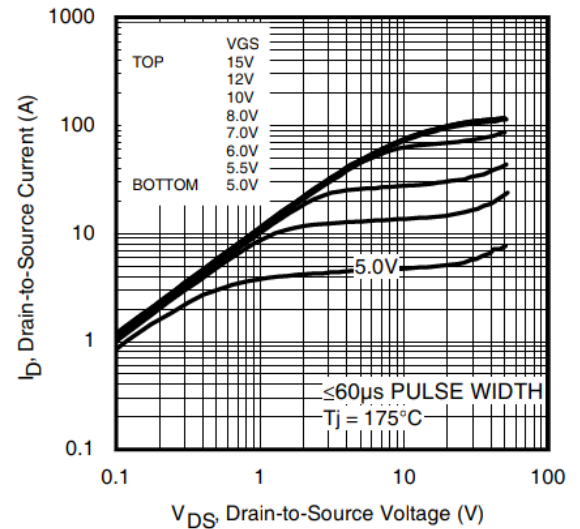
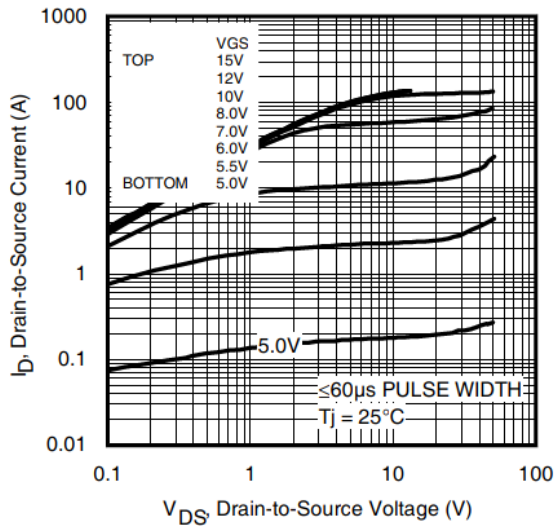
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	—	109	mJ
I_{AR}	Avalanche Energy ⑤	See Fig. 14, 15, 17a, 17b		A
E_{AR}	Repetitive Avalanche Current ⑤			A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S @ $T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	35	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 21A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	80	120	ns	$T_J = 25^\circ\text{C}, I_F = 21A, V_{DD} = 120V$
Q_{rr}	Reverse Recovery Charge	—	312	468	nC	$di/dt = 100A/\mu s$ ③

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting $T_J = 25^\circ\text{C}$, $L = 0.51mH$, $R_G = 25\Omega$, $I_{AS} = 21A$.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J approximately 90°C .
- ⑤ Limited by T_{Jmax} . See Figs. 14, 15, 17a, 17b for repetitive avalanche information



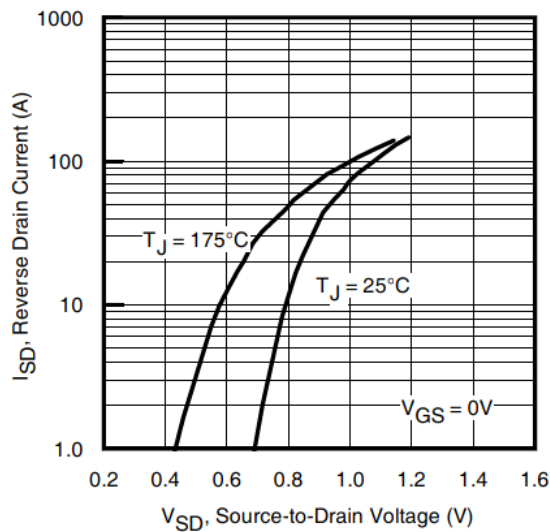


Fig. 7 Typical Source-Drain Diode Forward Voltage

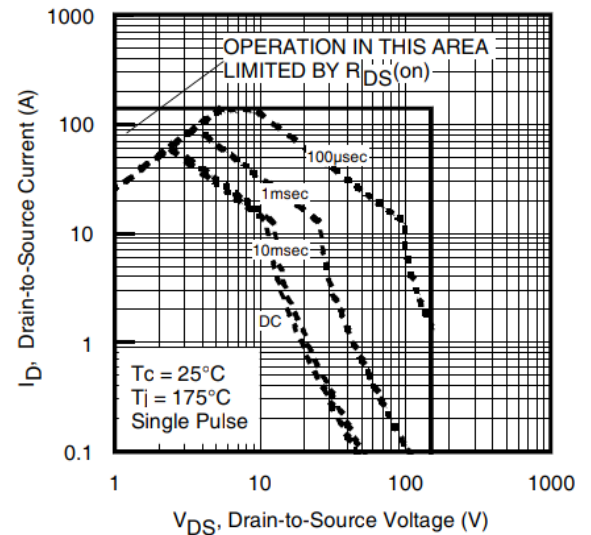


Fig 8. Maximum Safe Operating Area

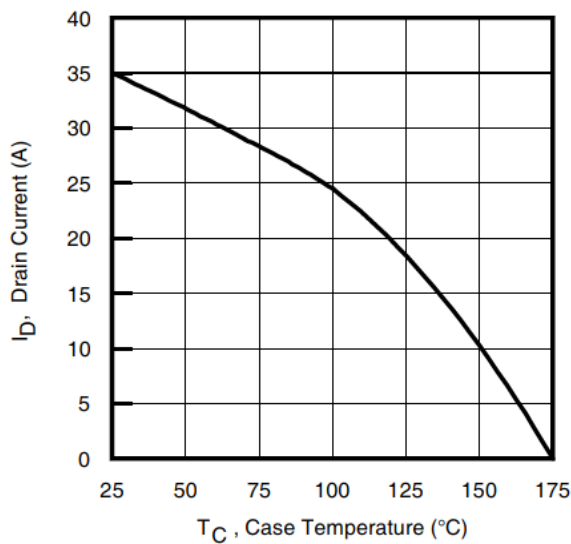


Fig 9. Maximum Drain Current vs. Case Temperature

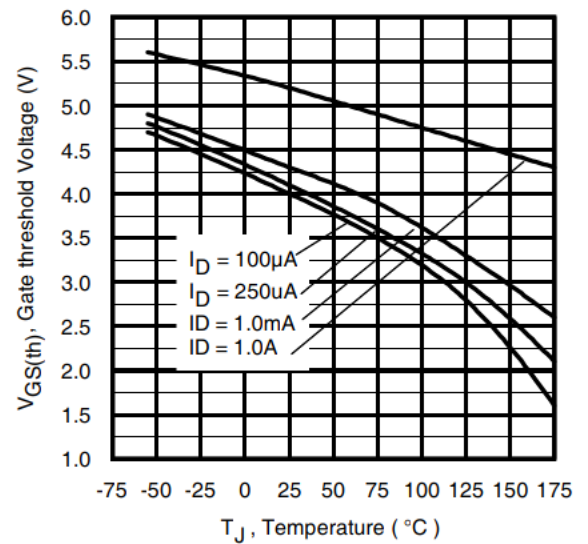


Fig 10. Threshold Voltage vs. Temperature

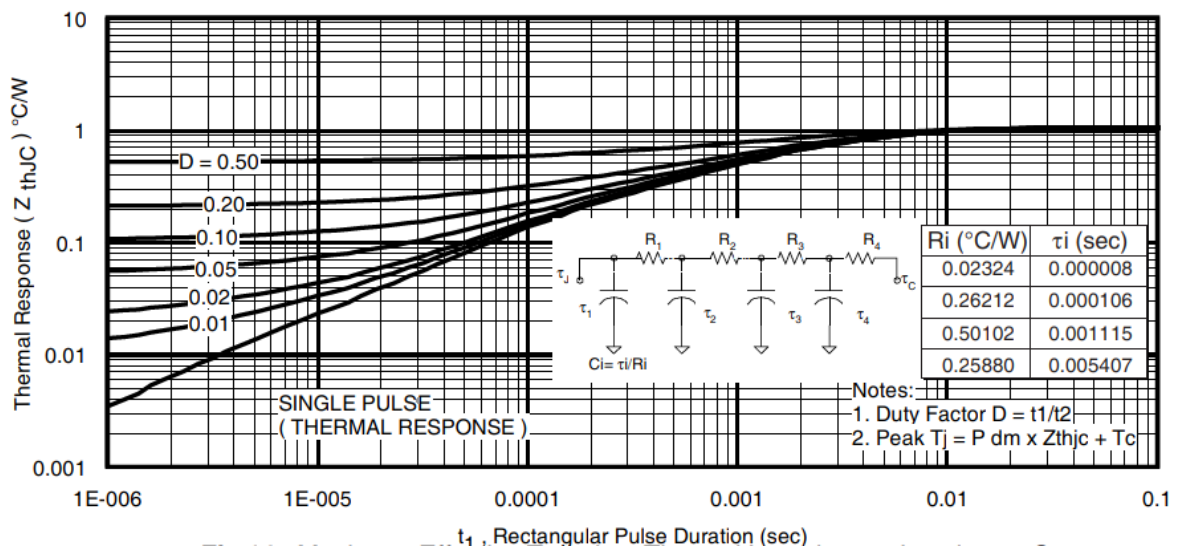


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

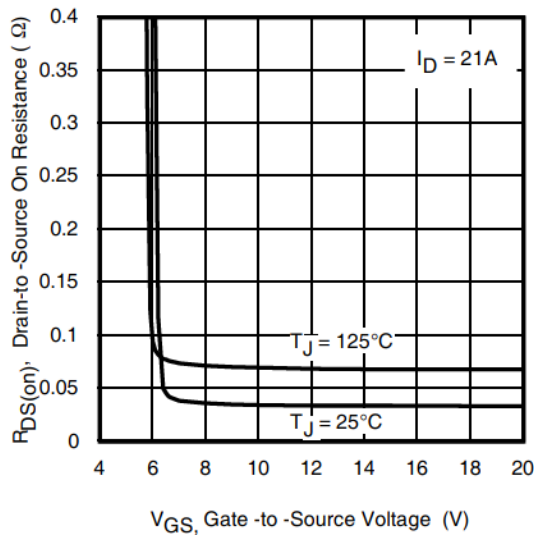


Fig. 12. On-Resistance Vs. Gate Voltage

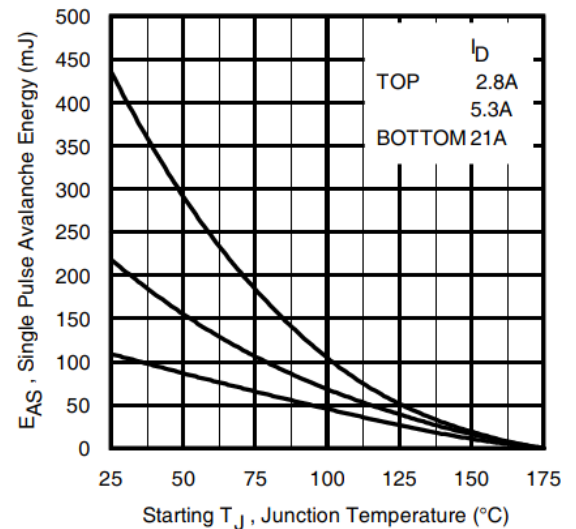


Fig 13. Maximum Avalanche Energy Vs. Temperature

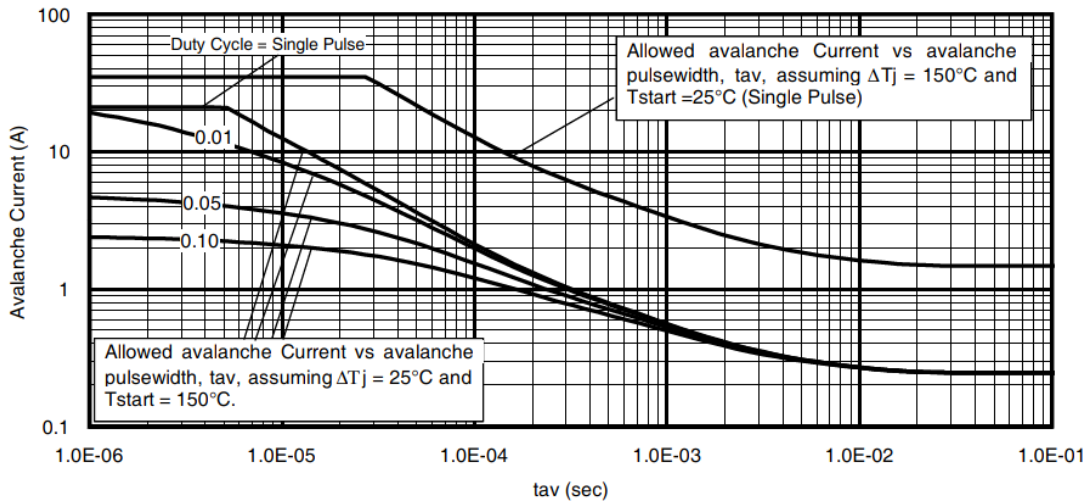


Fig 14. Typical Avalanche Current vs. Pulse width

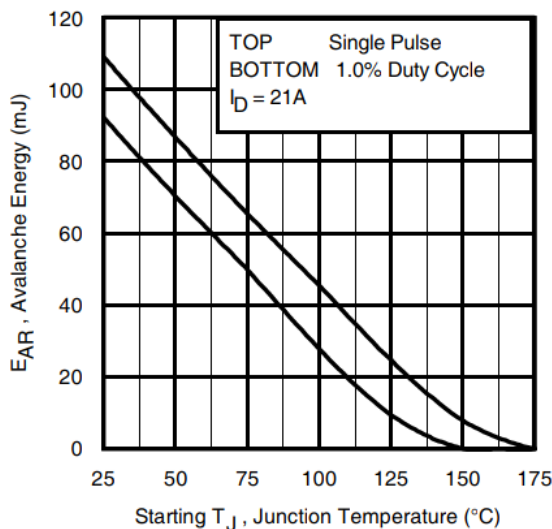


Fig 15. Maximum Avalanche Energy vs. Temperature

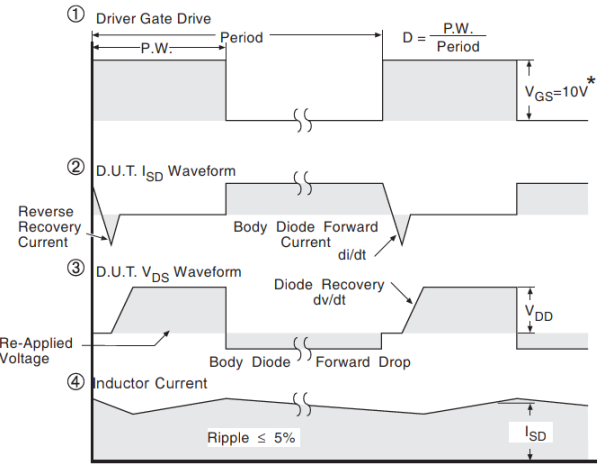
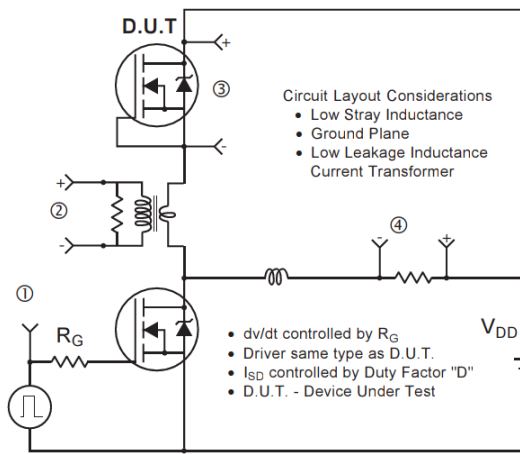
Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{Jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{Jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{Jmax} (assumed as 25°C in Figure 13, 14).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

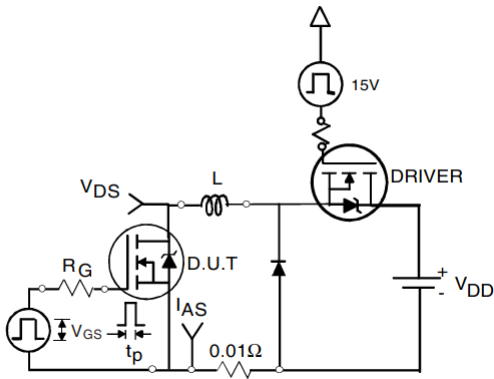


Fig 17a. Unclamped Inductive Test Circuit

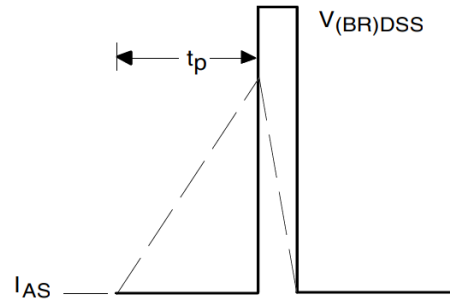


Fig 17b. Unclamped Inductive Waveforms

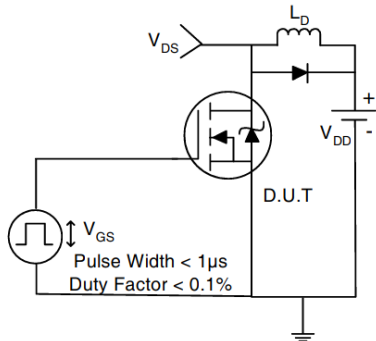


Fig 18a. Switching Time Test Circuit

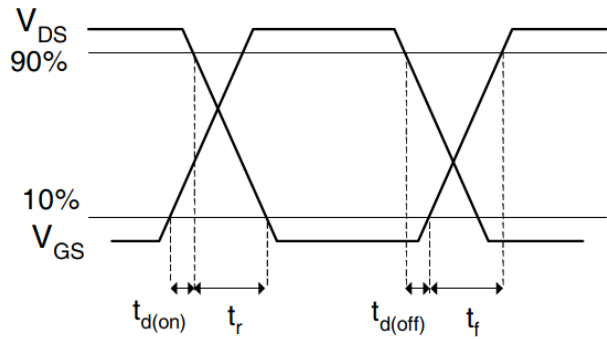


Fig 18b. Switching Time Waveforms

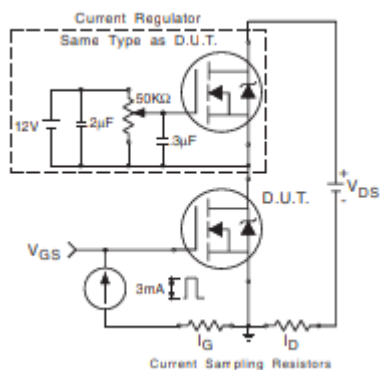


Fig 19a. Gate Charge Test Circuit

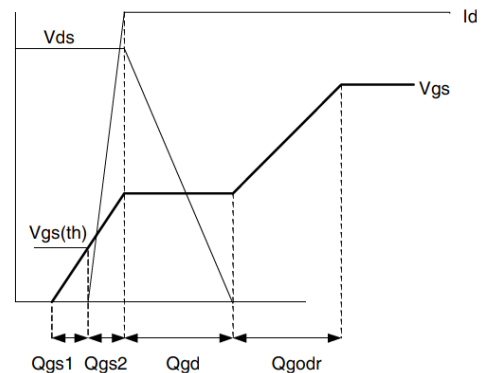
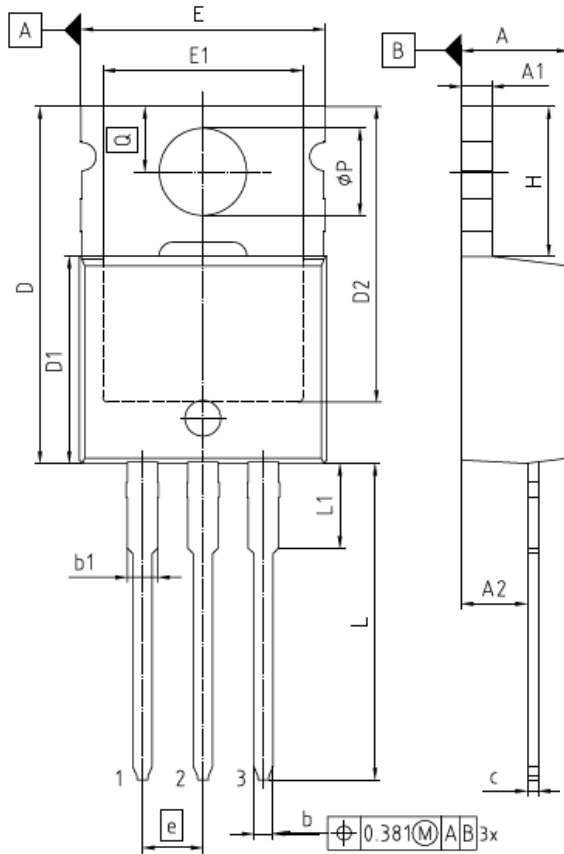


Fig 19b. Gate Charge Waveform

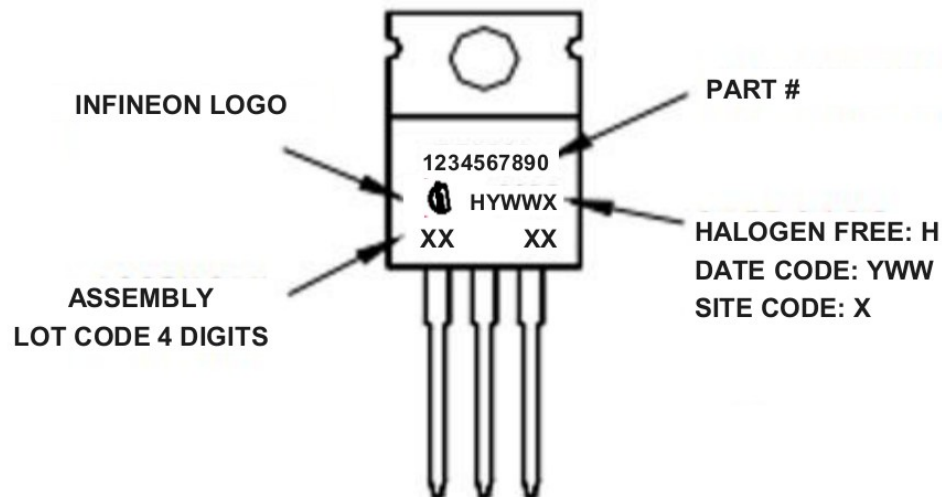
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER: PG-TO220-3-U05		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2026-09-18	2.1	- Update datasheet to Infineon format - Updated Package Outline and Part marking –page 7 - Added disclaimer on last page.

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