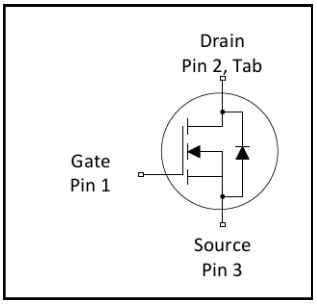
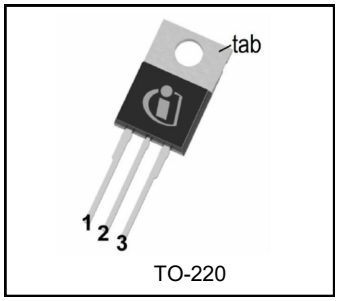
IRFB3077PbF

$V_{(BR)DSS}$	75V
$R_{DS(on)}$ typ.	2.8mΩ
max.	3.3mΩ
$I_{D\ (Silicon\ Limited)}$	210A①
$I_{D\ (Package\ Limited)}$	120A





G	D	S
Gate	Drain	Source

Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Worldwide Best $R_{DS(on)}$ in TO-220
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB3077PbF	TO-220	Tube	50	IRFB3077PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	210①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	150①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	120	
I_{DM}	Pulsed Drain Current ②	850	
P_D @T_C = 25°C	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Avalanche Characteristics

E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	200	mJ
I_{AR}	Avalanche Current ②	See Fig.14,15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.402	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧⑨	—	62	

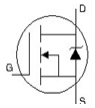
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.091	—	V/°C	Reference to 25°C, I_D = 5mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.8	3.3	mΩ	V_{GS} = 10V, I_D = 75A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 75V, V_{GS} = 0V
		—	—	250		V_{DS} = 75V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
R_G	Gate Resistance	—	1.2	—	Ω	f = 1.0MHz, open drain

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

gfs	Forward Trans conductance	160	—	—	S	V_{DS} = 50V, I_D = 75A
Q_g	Total Gate Charge	—	160	220	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge	—	37	—		V_{DS} = 38V
Q_{gd}	Gate-to-Drain Charge	—	42	—		V_{GS} = 10V⑤
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	V_{DD} = 38V
t_r	Rise Time	—	87	—		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	69	—		R_G= 2.1Ω
t_f	Fall Time	—	95	—		V_{GS} = 10V⑤
C_{iss}	Input Capacitance	—	9400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	820	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	350	—		f = 1.0MHz, See Fig. 5
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	1090	—		V_{GS} = 0V, V_{DS} = 0V to 60V⑦
$C_{oss\ eff.(TR)}$	Effective Output Capacitance (Time Related)	—	1260	—		V_{GS} = 0V, V_{DS} = 0V to 60V⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	210①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	850		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 75A,V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	42	63	ns	T_J = 25°C V_{DD} = 64V
		—	50	75		T_J = 125°C I_F = 75A,
Q_{rr}	Reverse Recovery Charge	—	59	89	nC	T_J = 25°C di/dt = 100A/µs ⑤
		—	86	130		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	2.5	—	A	T_J = 25°C

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.028mH, R_G = 25Ω, I_{AS} = 120A, V_{GS} =10V. Part not recommended for use above this value.

④ I_{SD} ≤ 75A, di/dt ≤ 400A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note# AN-994.

⑨ R_θ is measured at T_J approximately 90°C.

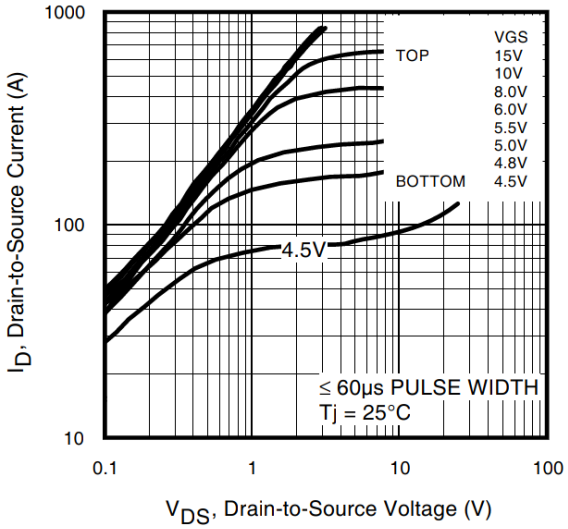


Fig. 1 Typical Output Characteristics

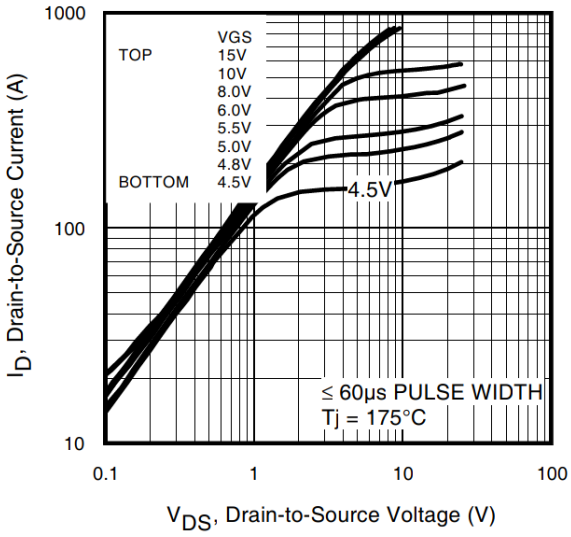


Fig. 2 Typical Output Characteristics

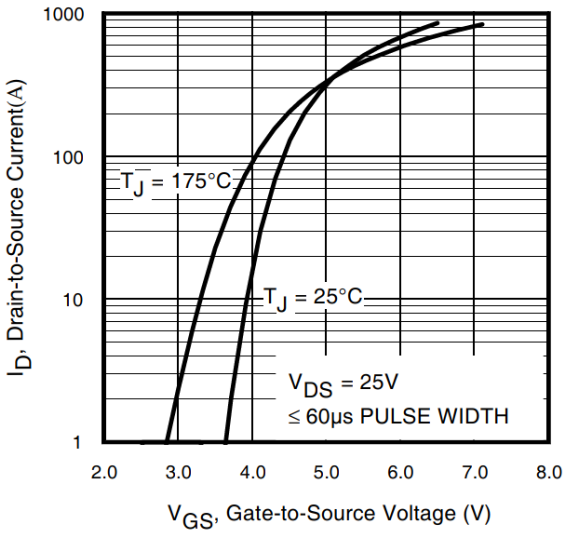


Fig. 3 Typical Transfer Characteristics

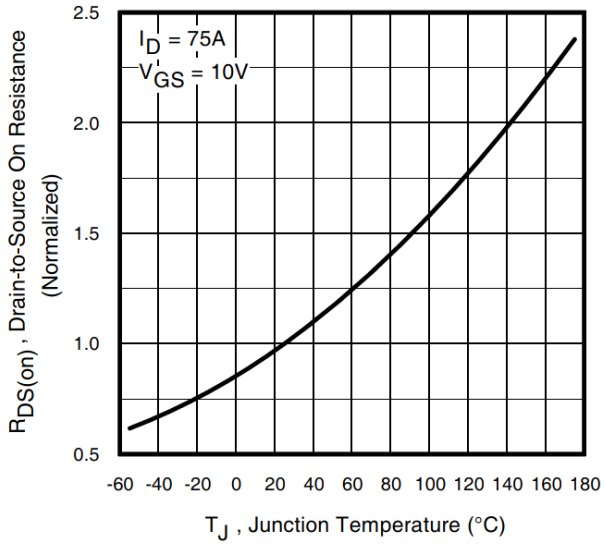


Fig. 4 Normalized On-Resistance vs. Temperature

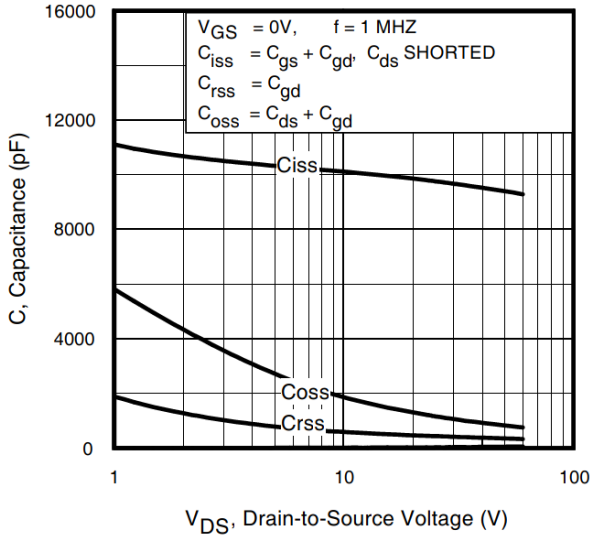


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

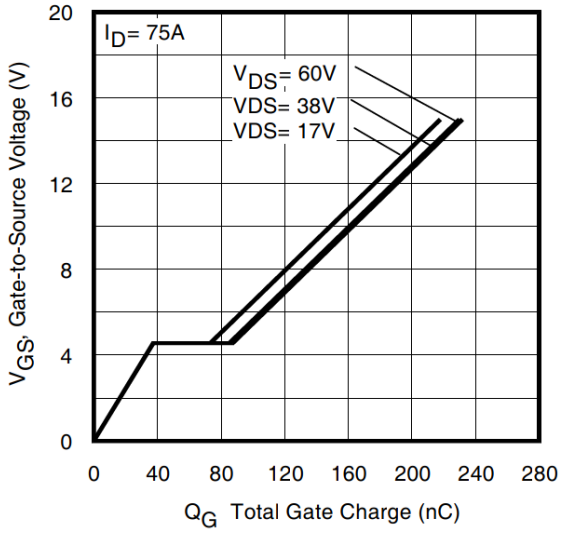


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

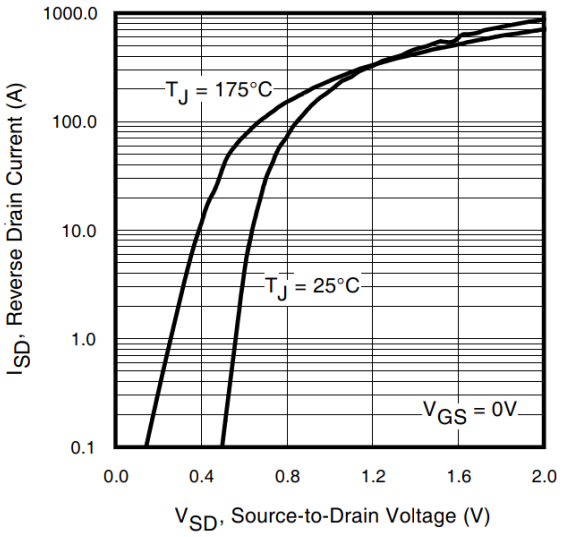


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

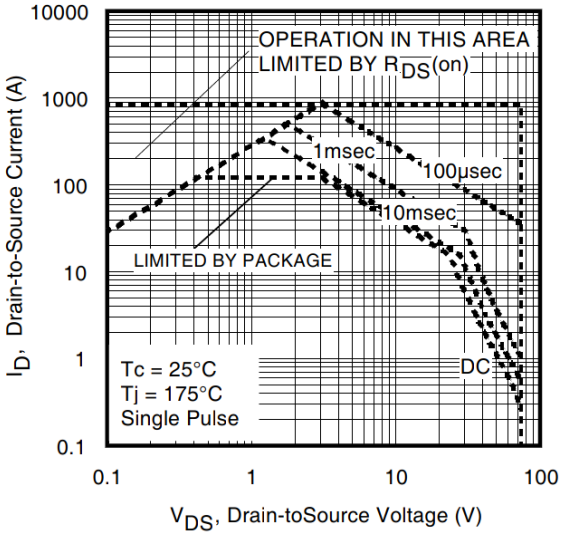


Fig 8. Maximum Safe Operating Area

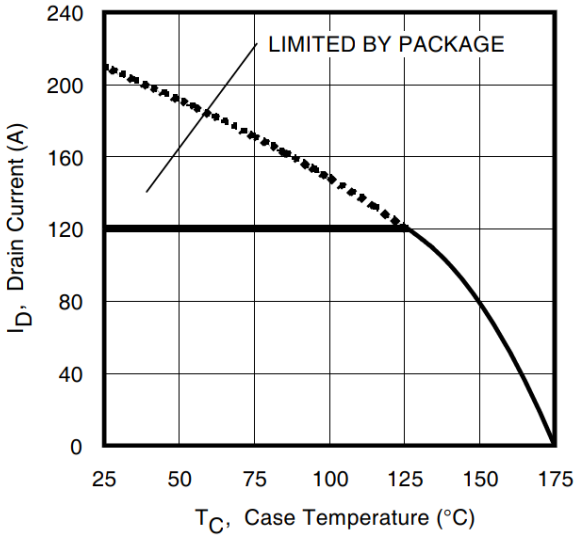


Fig 9. Maximum Drain Current vs. Case Temperature

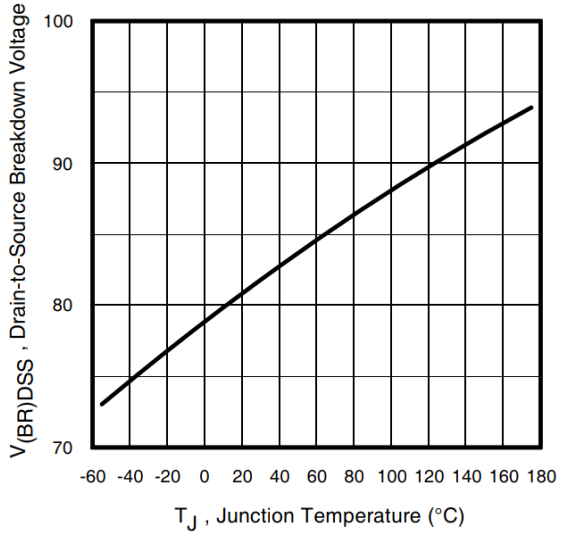


Fig 10. Drain-to-Source Breakdown Voltage

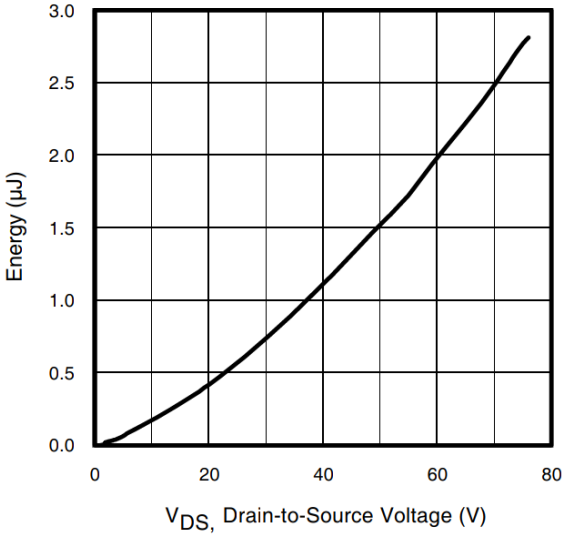


Fig 11. Typical Coss Stored Energy

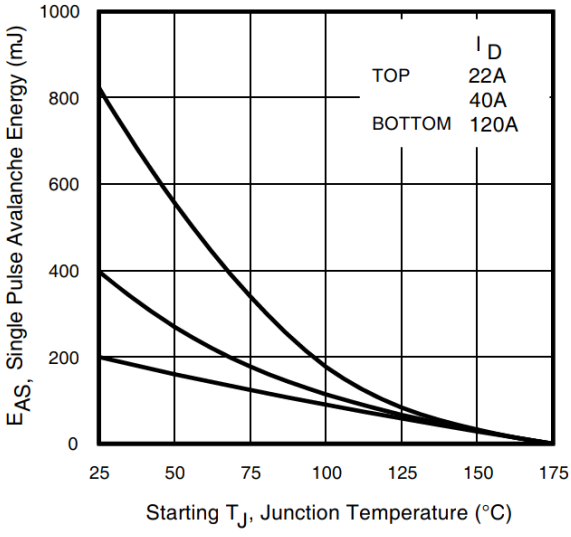


Fig 12. Maximum Avalanche Energy vs. Drain Current

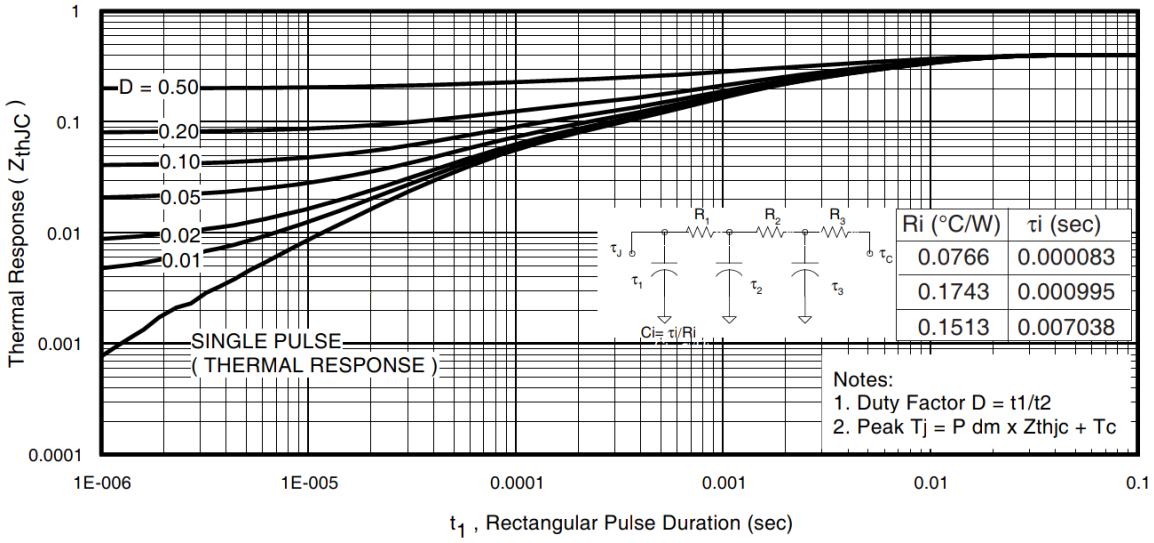


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

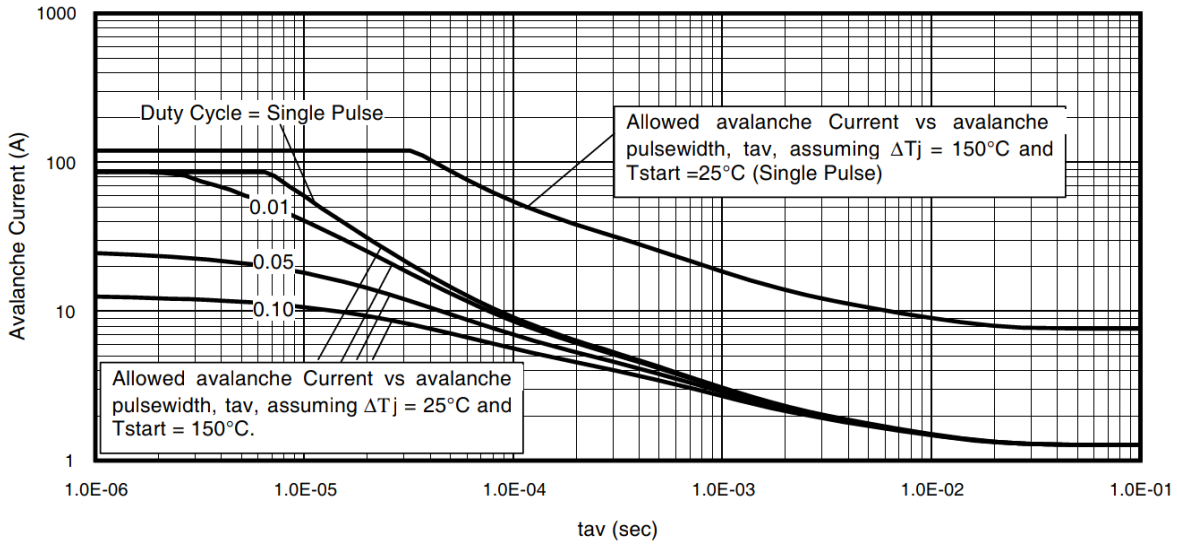


Fig 14. Avalanche Current vs. Pulse width

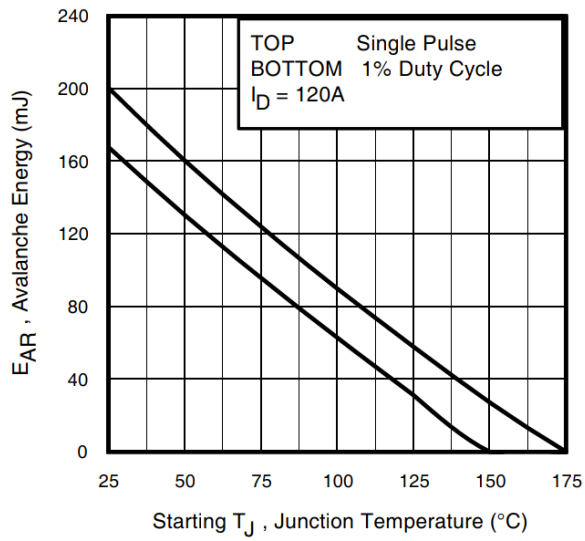


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

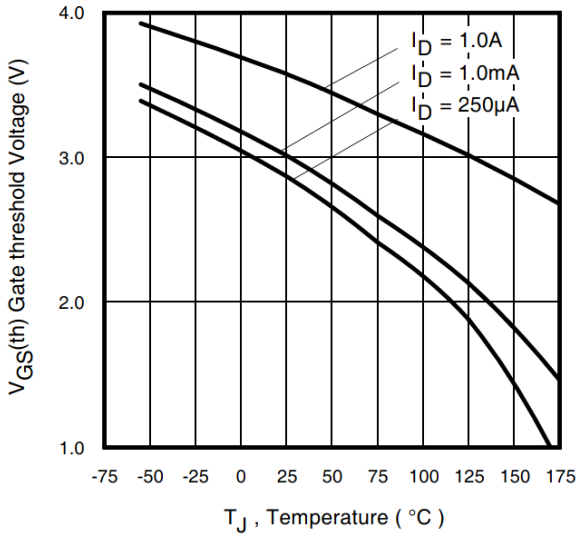


Fig 16. Threshold Voltage vs. Temperature

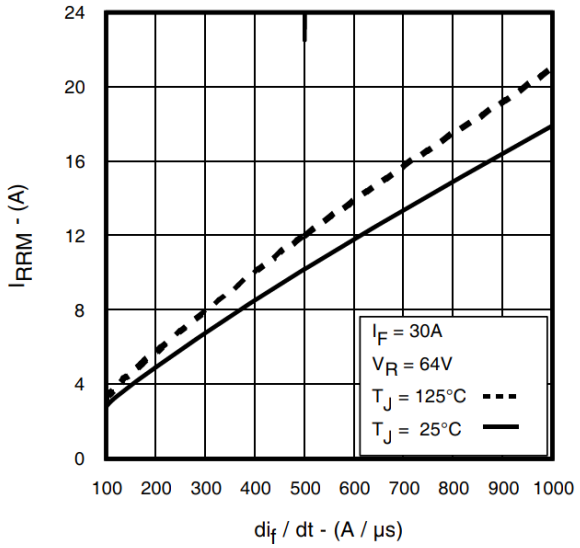


Fig. 17 - Typical Recovery Current vs. dif/dt

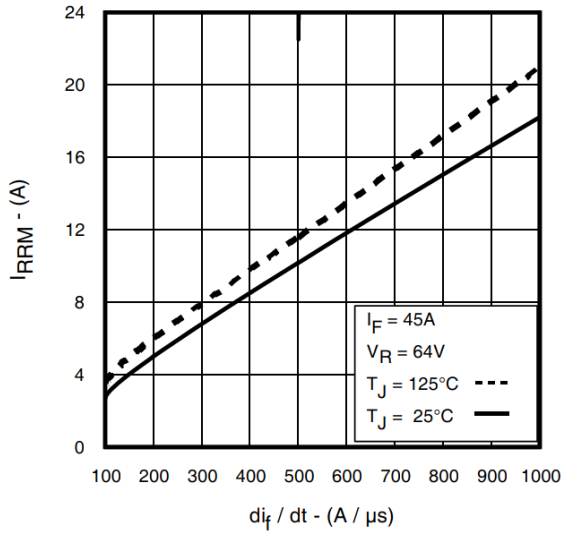


Fig. 18 - Typical Recovery Current vs. dif/dt

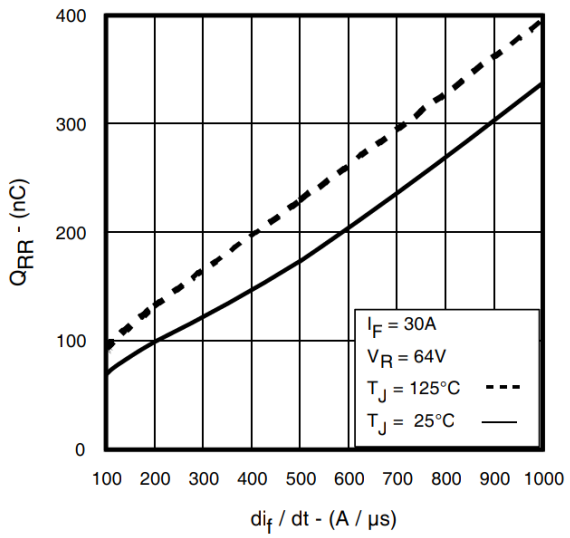


Fig. 19 - Typical Stored Charge vs. dif/dt

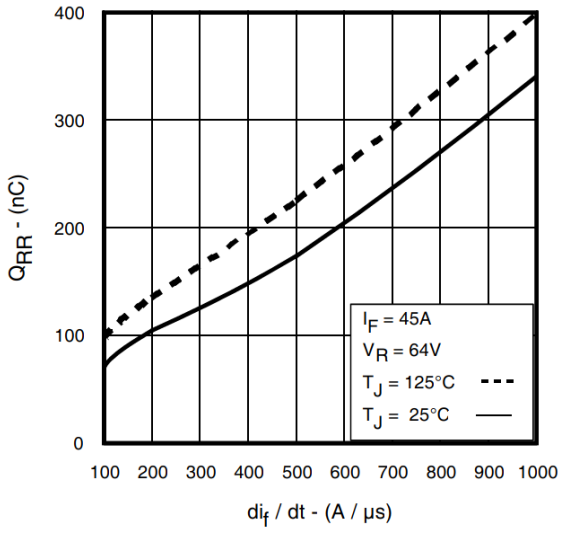


Fig. 20 - Typical Stored Charge vs. dif/dt

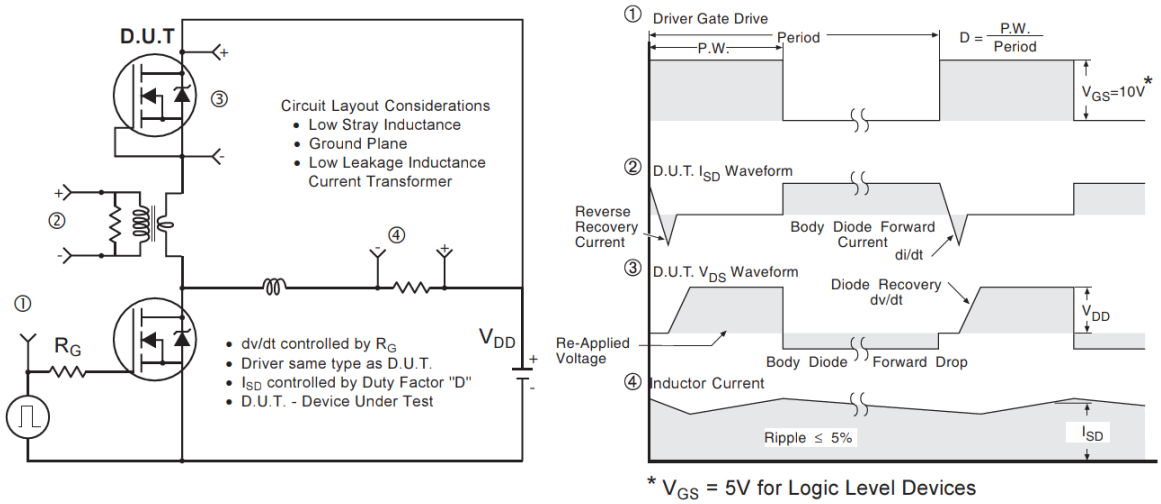


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

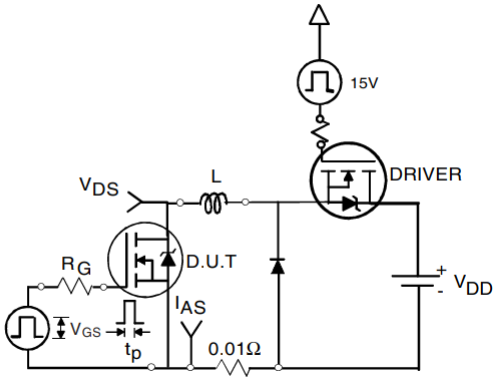


Fig 22a. Unclamped Inductive Test Circuit

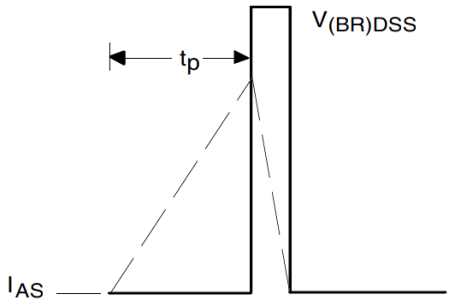


Fig 22b. Unclamped Inductive Waveforms

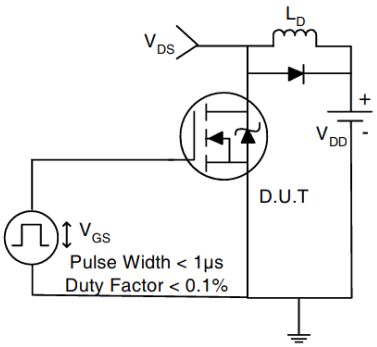


Fig 23a. Switching Time Test Circuit

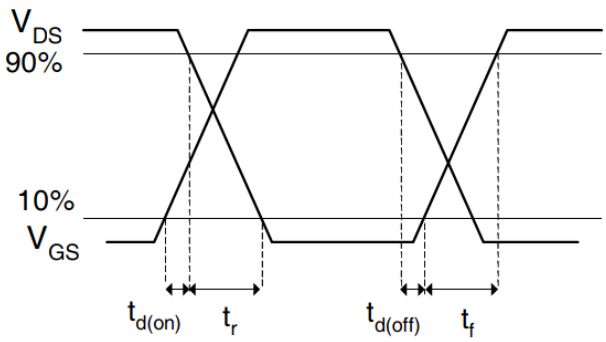


Fig 23b. Switching Time Waveforms

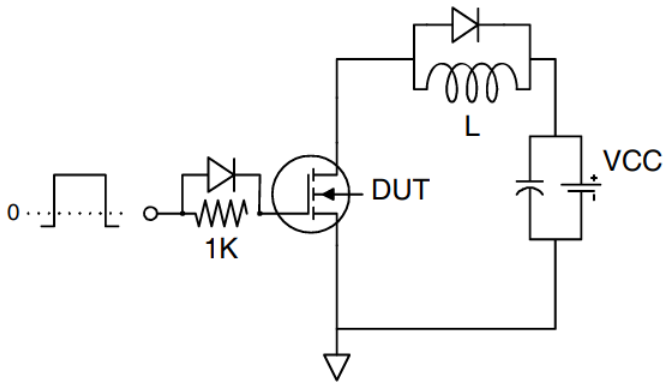


Fig 24a. Gate Charge Test Circuit

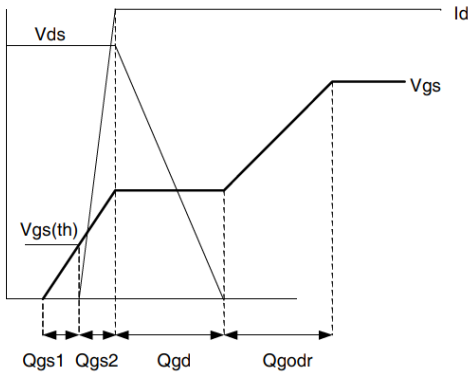
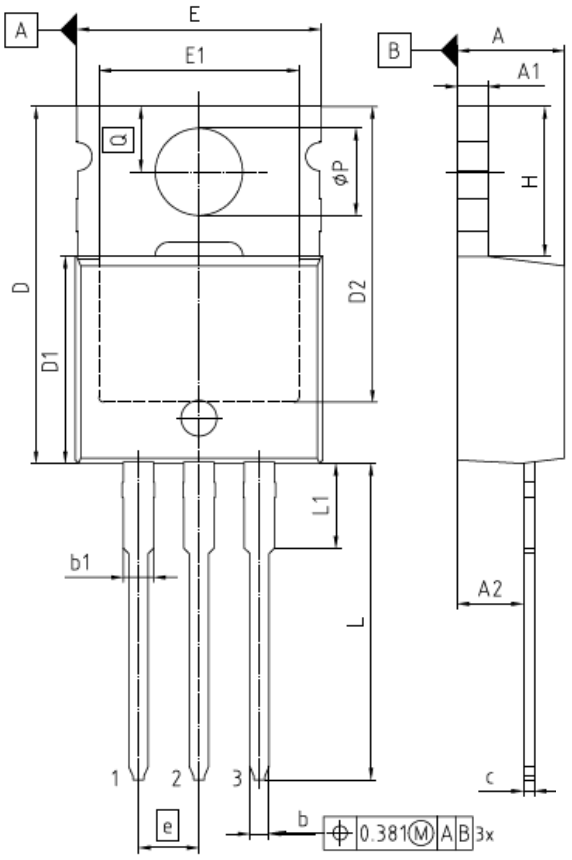


Fig 24b. Gate Charge Waveform

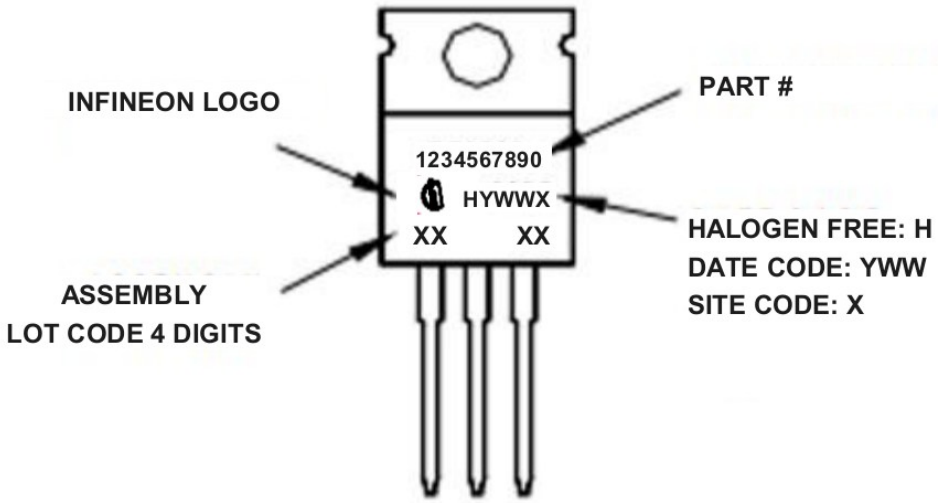
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER:	PG-TO220-3-U05	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2026-07-28	2.1	• Update datasheet to Infineon format • Updated Package Outline and Part marking –page 8 • Added disclaimer on last page.

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