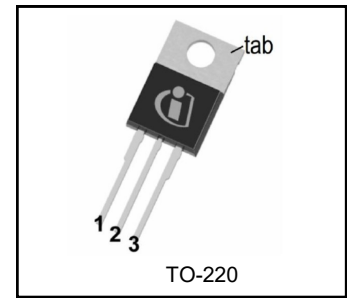
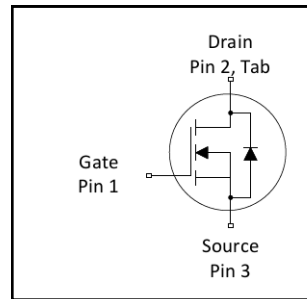


$V_{(BR)DSS}$	200V
$R_{DS(on)}$ max.	0.040Ω
I_D	56A



G	D	S
Gate	Drain	Source

Applications

- High frequency DC-DC converters
- Lead-Free

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB260NPbF	TO-220	Tube	50	IRFB260NPbF

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	56	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	40	
I_{DM}	Pulsed Drain Current ①	220	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	450	mJ
I_{AR}	Avalanche Current ①	34	A
E_{AR}	Repetitive Avalanche Energy ①	38	mJ
dv/dt	Peak Diode Recovery dv/dt ③	10	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.40	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	$V_{GS} = 10V, I_D = 34A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Trans conductance	29	—	—	S	$V_{DS} = 50V, I_D = 34A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

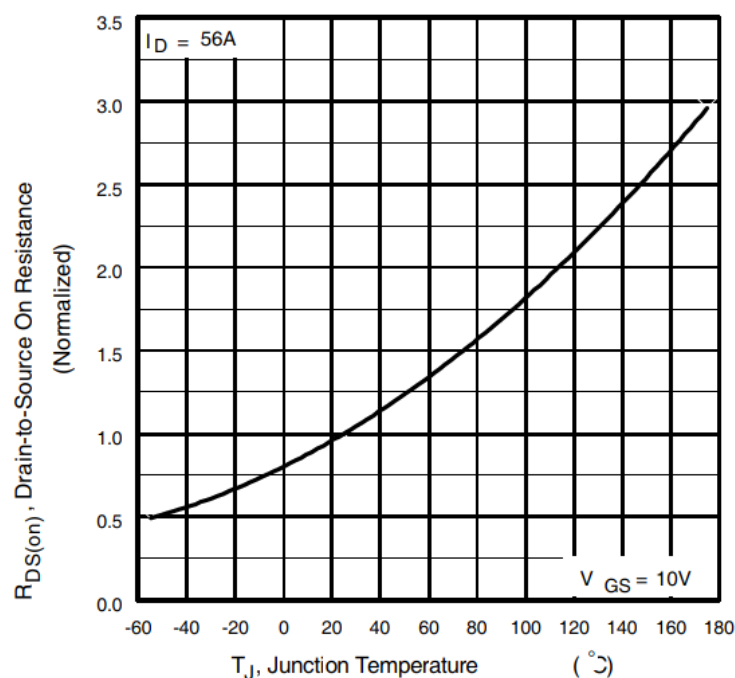
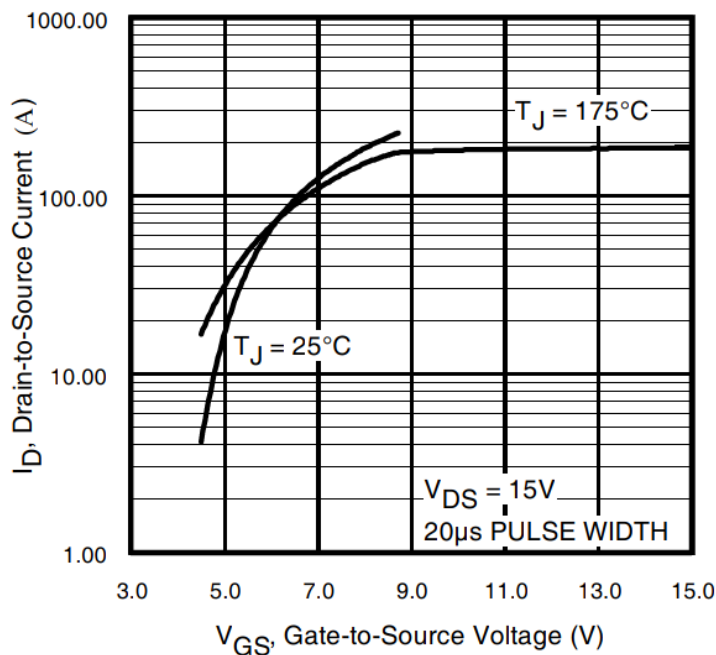
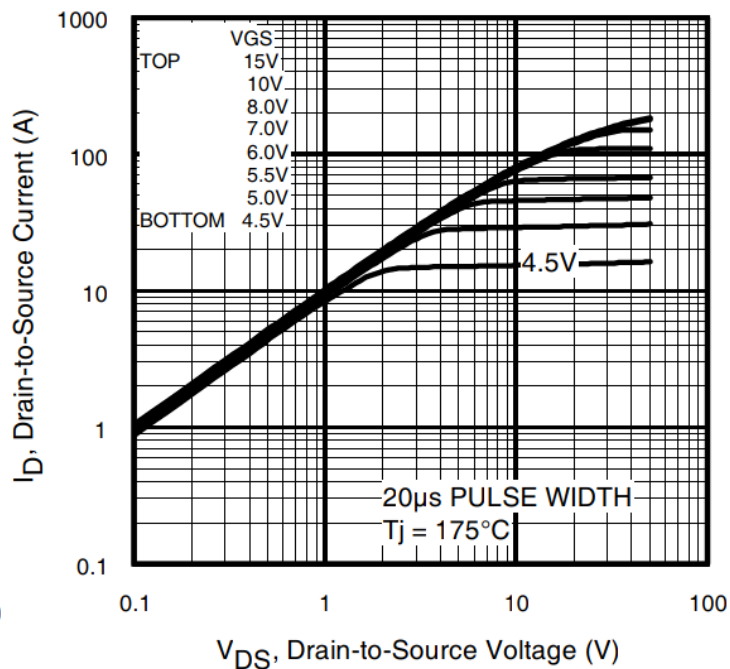
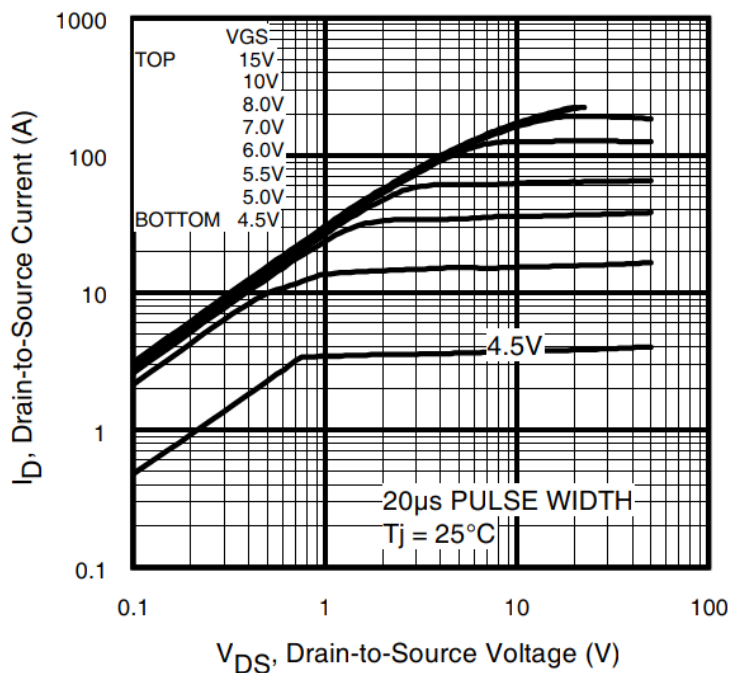
Q_g	Total Gate Charge	—	150	220	nC	$I_D = 34A$ $V_{DS} = 160V$ $V_{GS} = 10V$, See Fig. 6 and 13
Q_{gs}	Gate-to-Source Charge	—	24	37		
Q_{gd}	Gate-to-Drain Charge	—	67	100		
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 100V$ $I_D = 34A$ $R_G = 1.8\Omega$ $V_{GS} = 10V$, See Fig. 10 ④
t_r	Rise Time	—	64	—		
$t_{d(off)}$	Turn-Off Delay Time	—	52	—		
t_f	Fall Time	—	50	—		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	4220	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig.5
C_{oss}	Output Capacitance	—	580	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ③
C_{rss}	Reverse Transfer Capacitance	—	140	—		
C_{oss}	Output Capacitance	—	5080	—		
C_{oss}	Output Capacitance	—	230	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	500	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 34A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	240	360	ns	$T_J = 25^\circ\text{C}, I_F = 34A$
Q_{rr}	Reverse Recovery Charge	—	2.1	3.2	μC	$di/dt = 100A/\mu s$ ④

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.78\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 34A$
- ③ $I_{SD} \leq 34A$, $di/dt \leq 480A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .



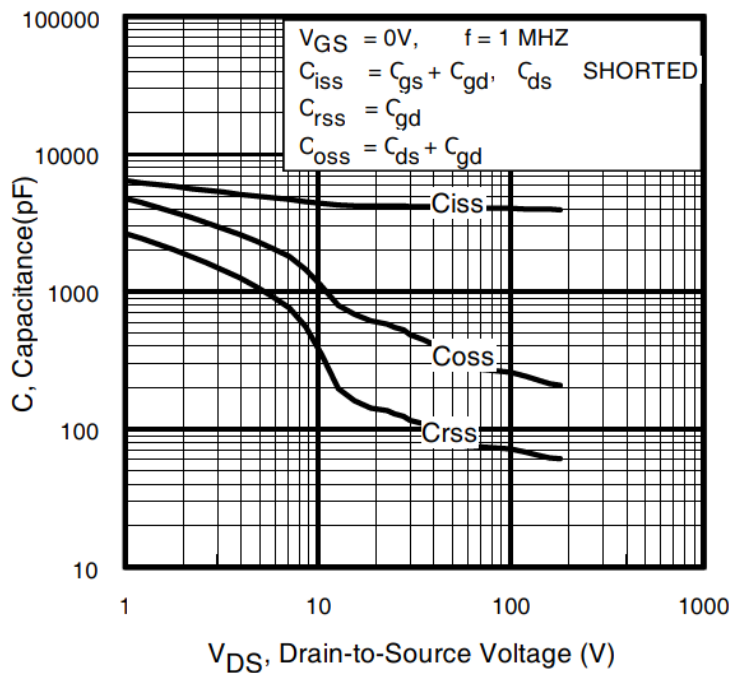


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

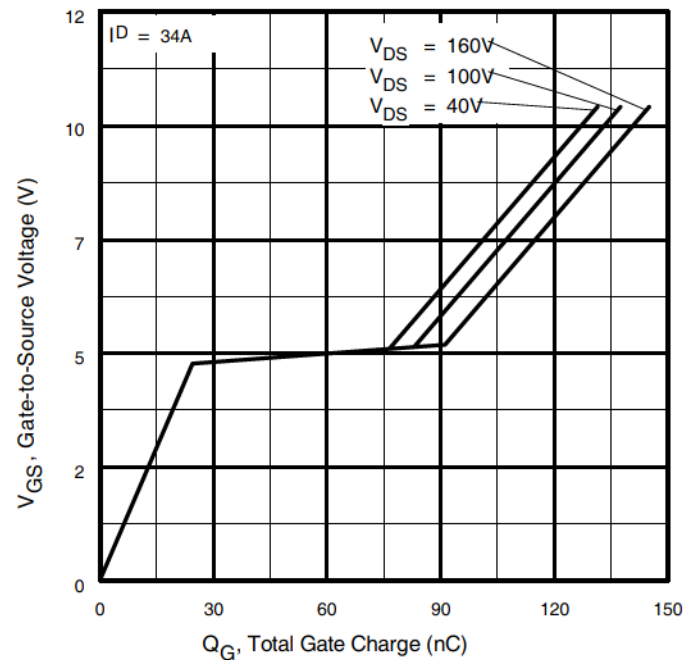


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

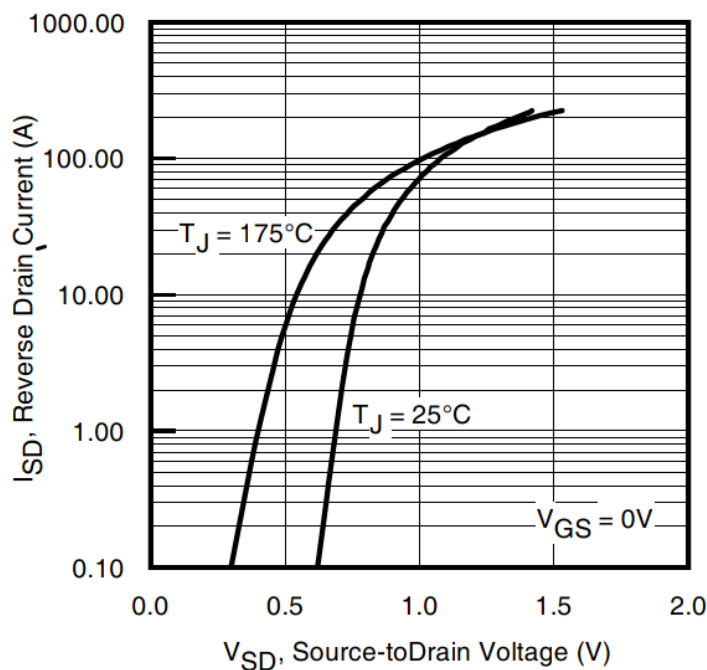


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

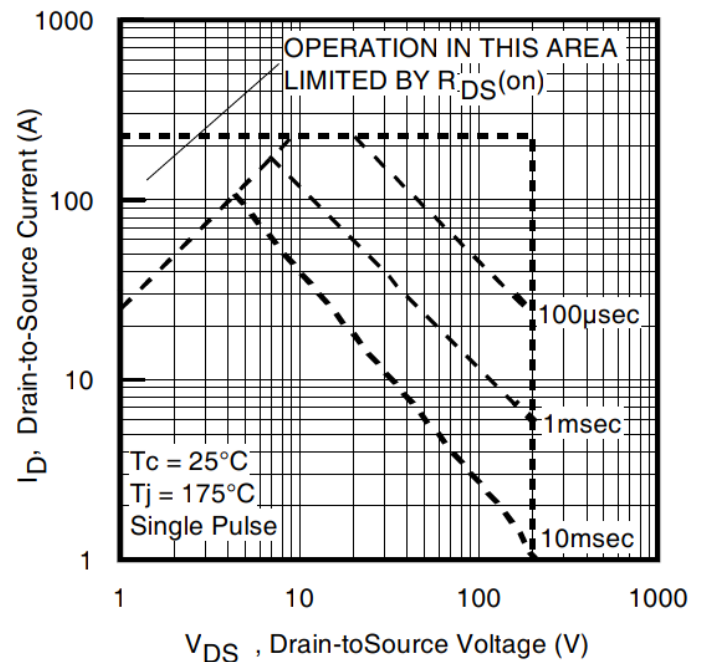


Fig 8. Maximum Safe Operating Area

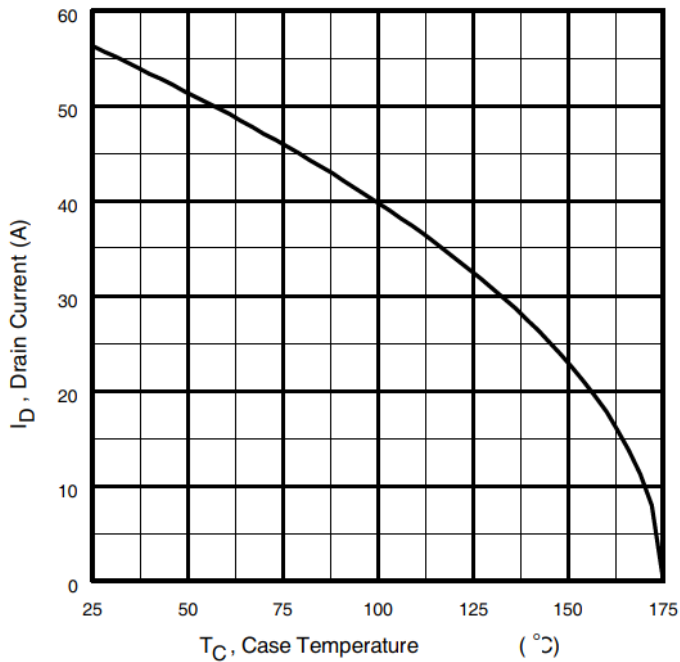


Fig 9. Maximum Drain Current vs. Case Temperature

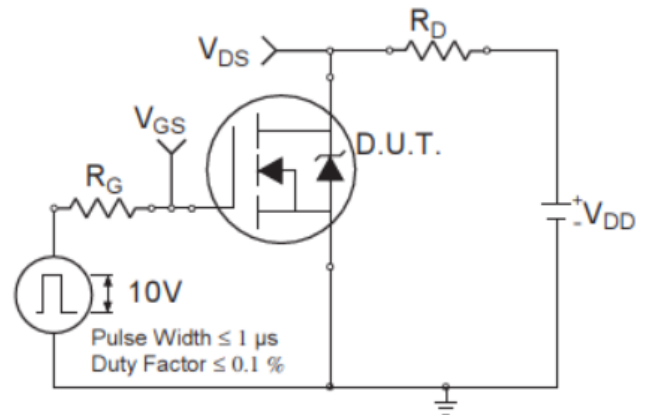


Fig 10b. Switching Time Test Circuit

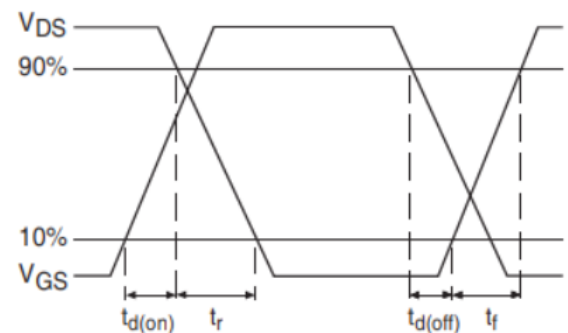


Fig 10b. Switching Time Waveforms

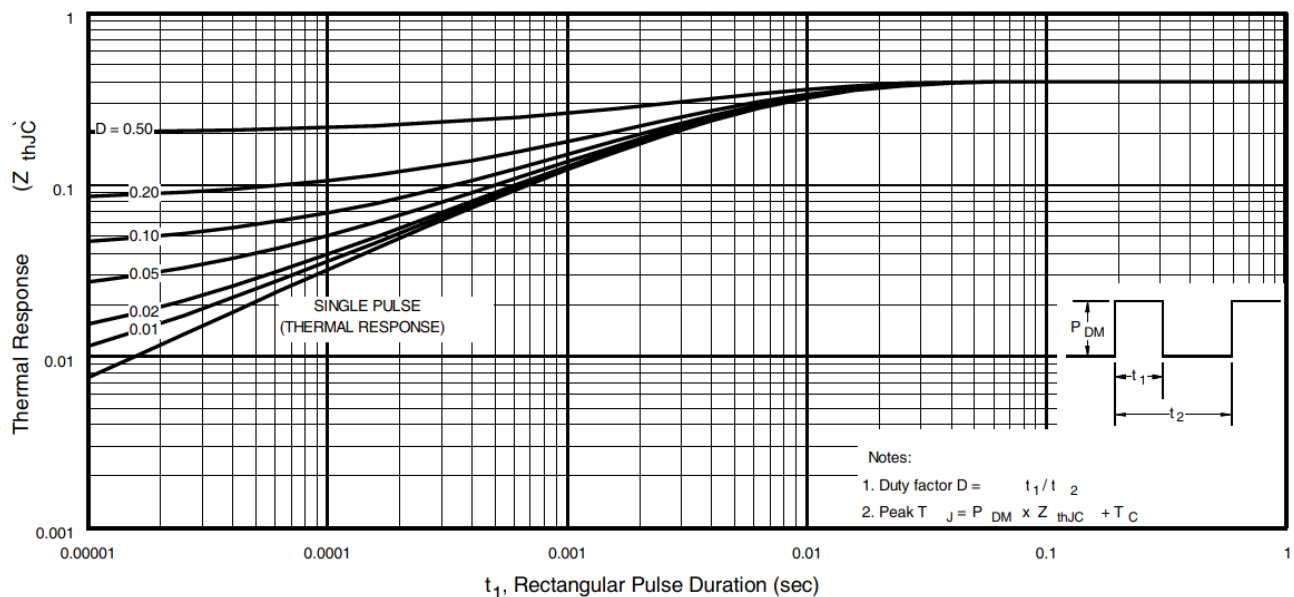


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

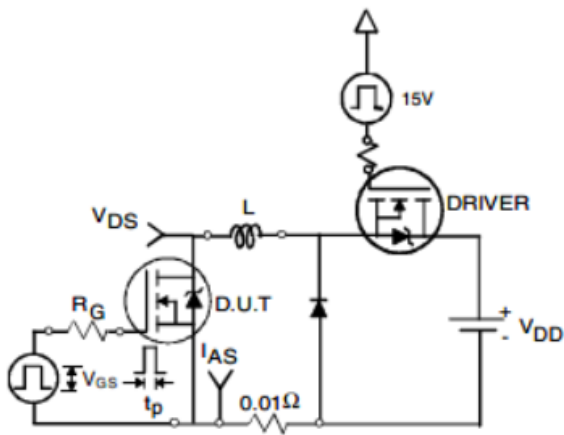


Fig. 12a. Unclamped Inductive Test Circuit

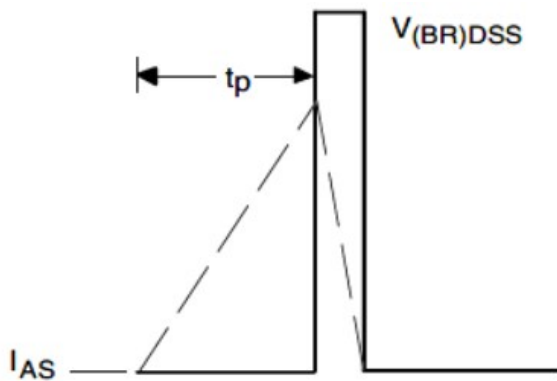


Fig. 12b. Unclamped Inductive Waveforms

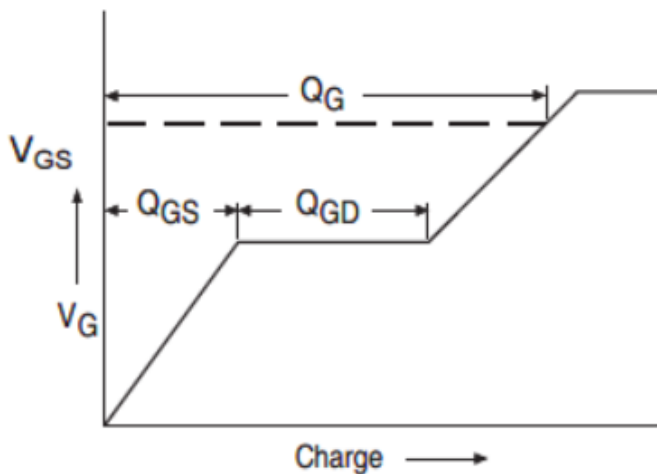


Fig 13a. Basic Gate Charge Waveform

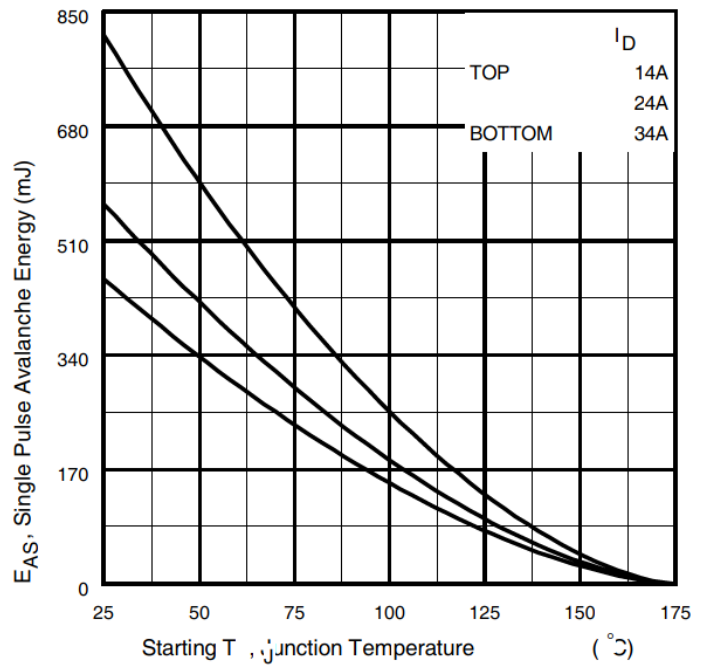


Fig 12c. Maximum Avalanche Energy vs. Drain Current

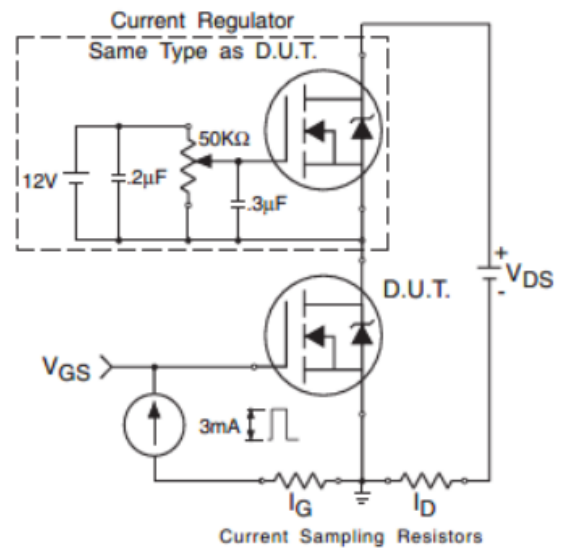


Fig 13b. Gate Charge Test Circuit

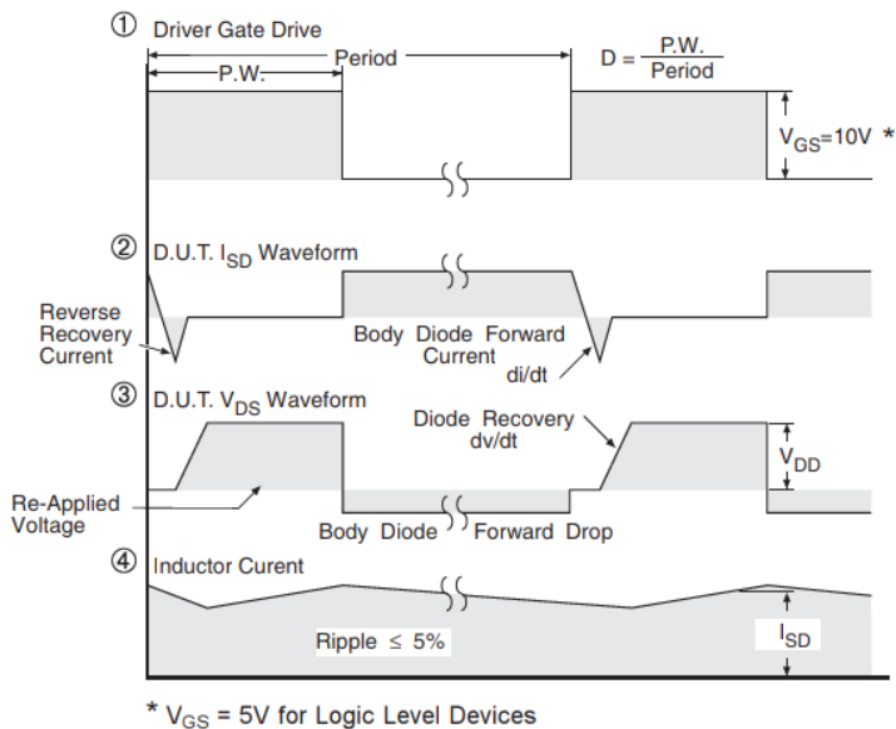
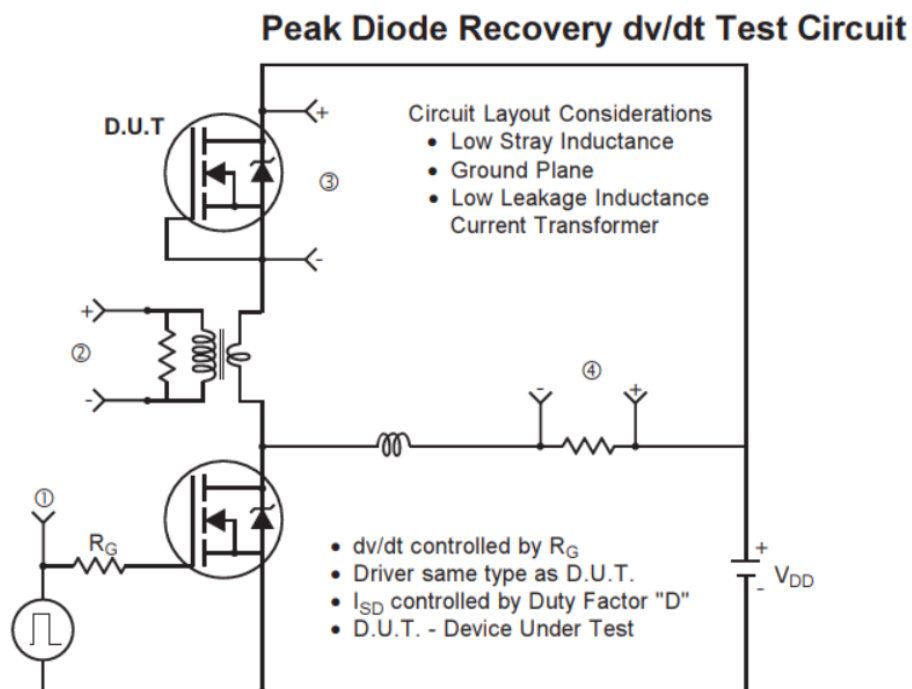
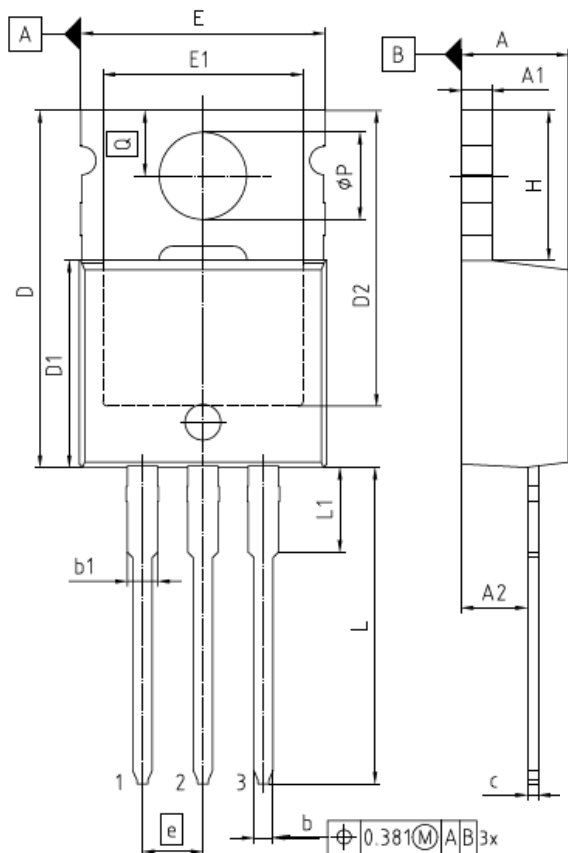


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs

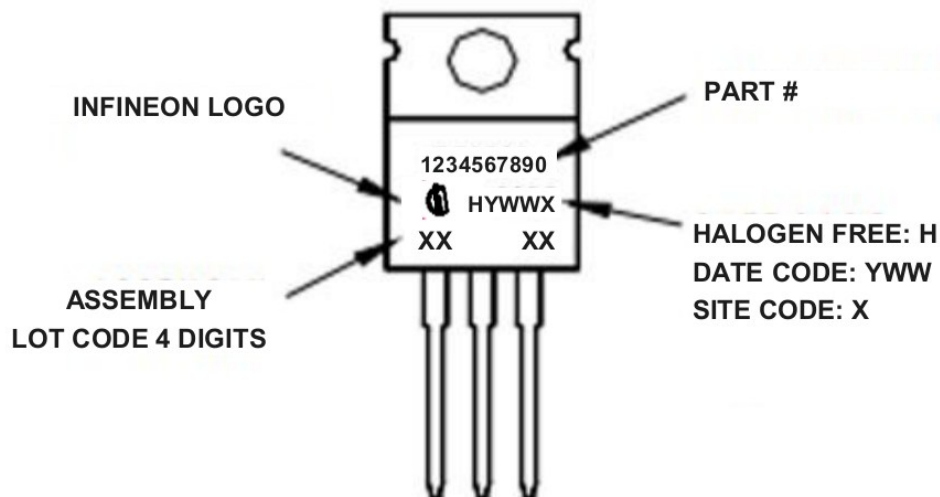
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER: PG-TO220-3-U05		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2026-07-28	2.1	- Update datasheet to Infineon format - Updated Package Outline and Part marking –page 8 - Added disclaimer on last page.

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