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International
IOR Rectifier

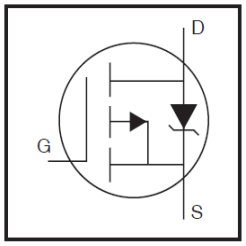
PD - 97034

IRF4905SPbF
IRF4905LPbF

英飞凌HEXFET®功率MOSFET

特性

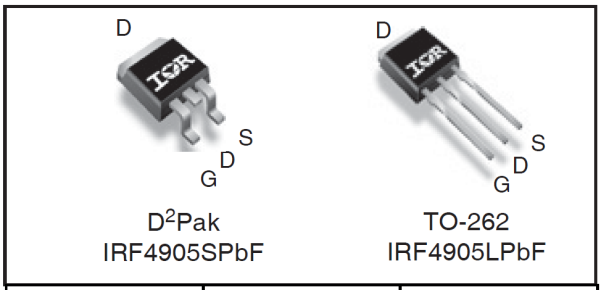
- 先进工艺技术
- 超低导通电阻
- 工作温度150°C
- 快速开关
- 允许达到 Tjmax 的重复雪崩
- 某些参数与 IRF4905S不同
- 无铅



V_{DSS} = -55V

$R_{DS(on)}$ = 20mΩ

I_D = -42A



D^2Pak
IRF4905SPbF

TO-262
IRF4905LPbF

G	D	S
Gate	Drain	Source

概述

英飞凌该设计的其他特点包括 150°C 工作结温、开关速度快和提高重复雪崩额定值。通过结合以上特点，使该设计成为一种极其高效和可靠的器件，可用于汽车应用和各种其他应用。

绝对最大额定值

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-70	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-44	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	-42	
I_{DM}	Pulsed Drain Current ①	-280	
P_D @T_C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy②	140	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	790	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf in (1.1N m)	

热阻抗

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	---	0.75	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑦⑧	---	40	

8/5/05

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。 为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

电气特性 @T_J = 25°C（除非另有说明）

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	---	---	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	---	-0.054	---	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	---	---	20	mΩ	V_{GS} = -10V, I_D = -42A ③
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	---	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
gfs	Forward Transconductance	19	---	---	S	V_{DS} = -25V, I_D = -42A
I_{DSS}	Drain-to-Source Leakage Current	---	---	-25	µA	V_{DS} = -55V, V_{GS} = 0V
		---	---	-200		V_{DS} = -44V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	---	---	100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	---	---	-100		V_{GS} = 20V
Q_g	Total Gate Charge	---	120	180	nC	I_D = -42A V_{DS}
Q_{gs}	Gate-to-Source Charge	---	32	---		= -44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	---	53	---		V_{GS} = -10V ③
$t_{d(on)}$	Turn-On Delay Time	---	20	---	ns	V_{DD} = -28V I_D
t_r	Rise Time	---	99	---		= -42A R_G =
$t_{d(off)}$	Turn-Off Delay Time	---	51	---		2.6 Ω
t_f	Fall Time	---	64	---		V_{GS} = -10V ③
L_S	Internal Source Inductance	---	7.5	---	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	---	3500	---	pF	V_{GS} = 0V V_{DS}
C_{oss}	Output Capacitance	---	1250	---		= -25V
C_{rss}	Reverse Transfer Capacitance	---	450	---		f = 1.0MHz
C_{oss}	Output Capacitance	---	4620	---		V_{GS} = 0V, V_{DS} = -1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	---	940	---		V_{GS} = 0V, V_{DS} = -44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	---	1530	---		V_{GS} = 0V, V_{DS} = 0V to -44V ④

源极-漏极额定值与特性

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	---	---	-42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) CD	---	---	-280		
V_{SD}	Diode Forward Voltage	---	---	-1.3	V	T_J = 25°C, I_S = -42A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	---	61	92	ns	T_J = 25°C, I_F = -42A, V_{DD} = -28V
Q_{rr}	Reverse Recovery Charge	---	150	220	nC	di/dt = -100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

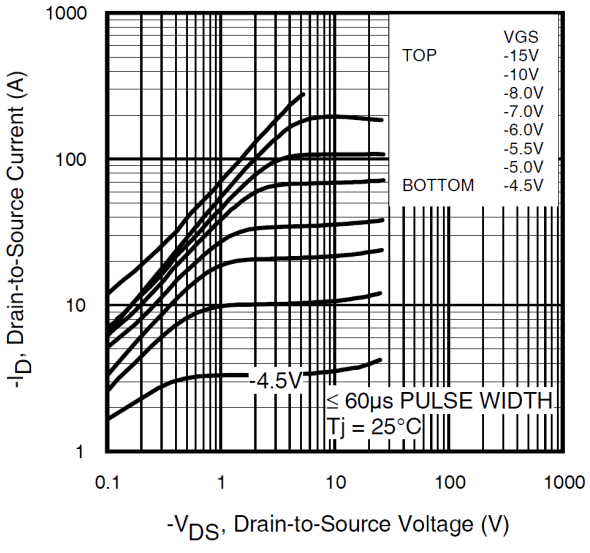


Fig 1. Typical Output Characteristics

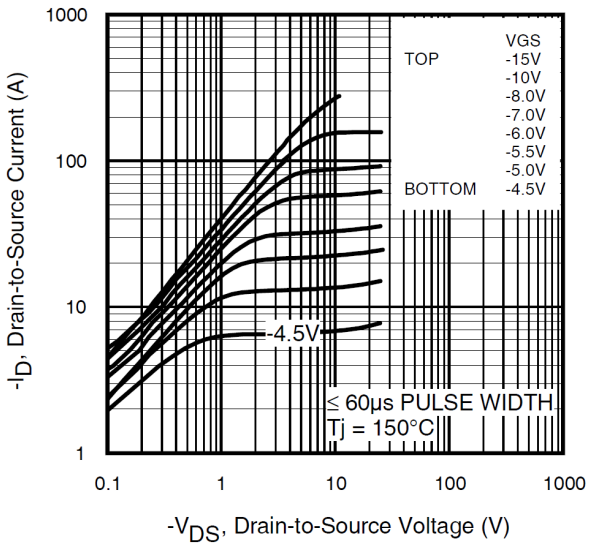


Fig 2. Typical Output Characteristics

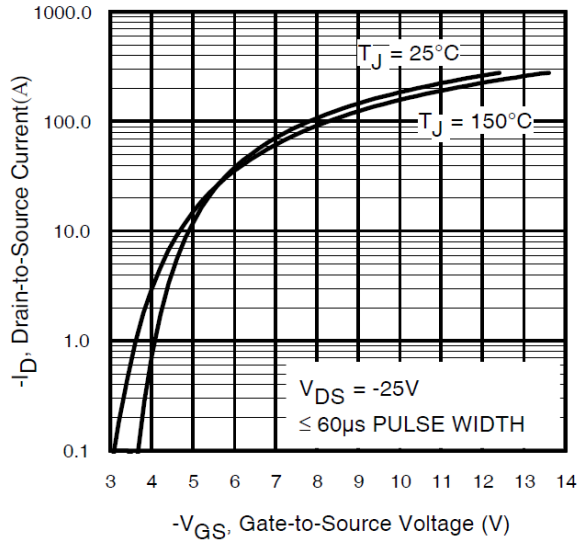


Fig 3. Typical Transfer Characteristics

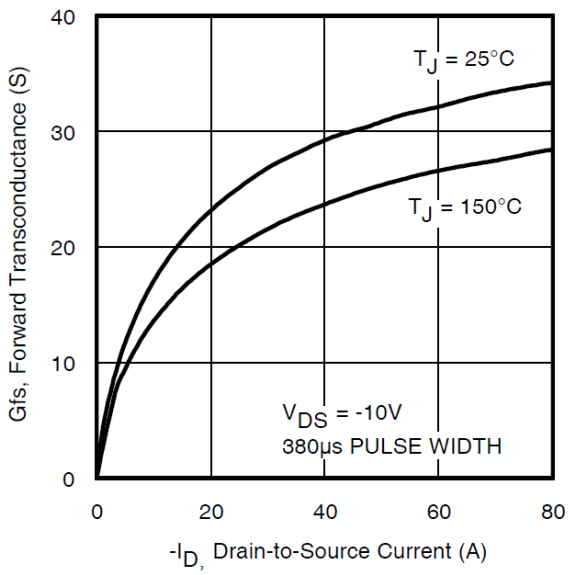


Fig 4. Typical Forward Transconductance Vs. Drain Current

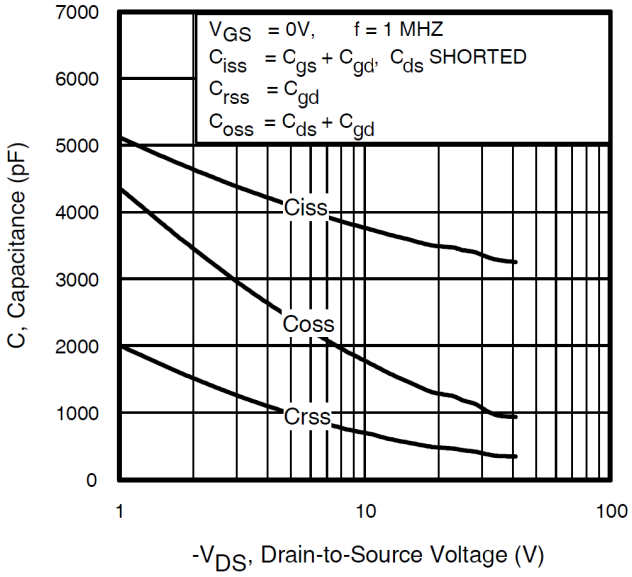


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

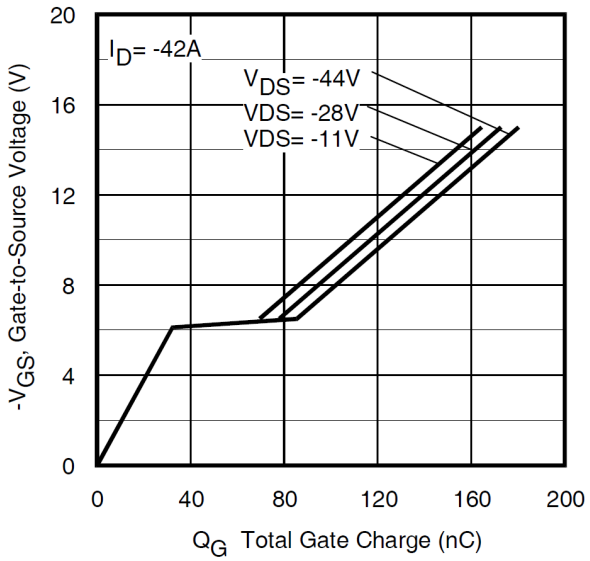


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

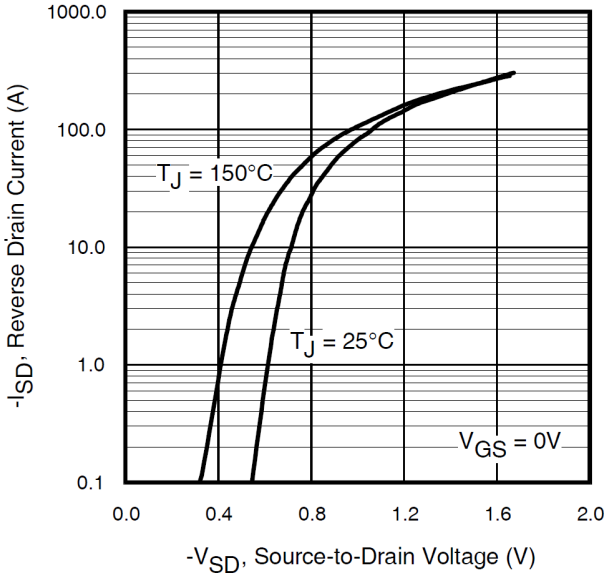


Fig 7. Typical Source-Drain Diode Forward Voltage

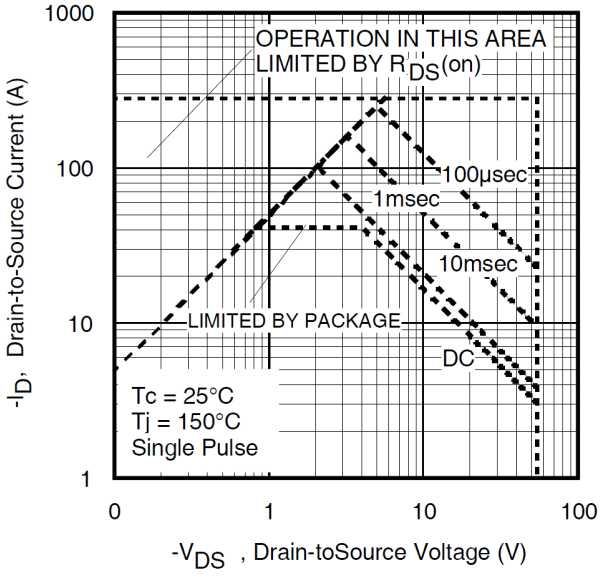


Fig 8. Maximum Safe Operating Area

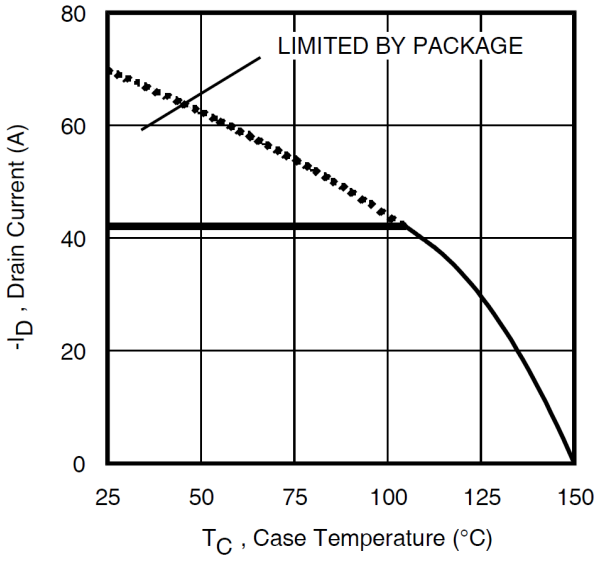


Fig 9. Maximum Drain Current Vs. Case Temperature

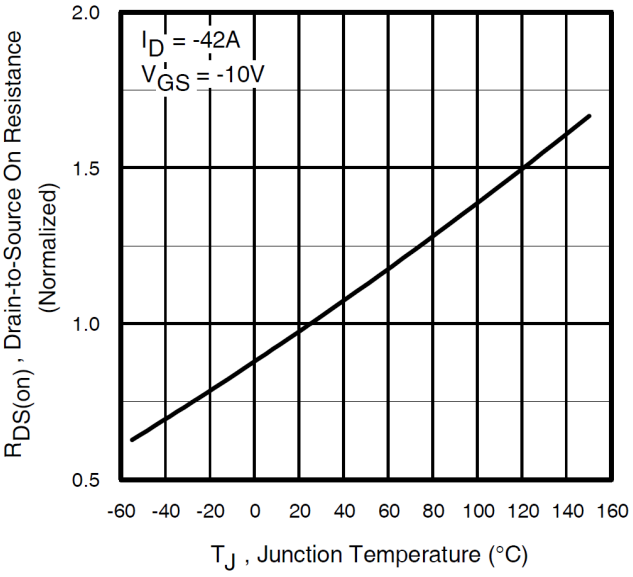


Fig 10. Normalized On-Resistance Vs. Temperature

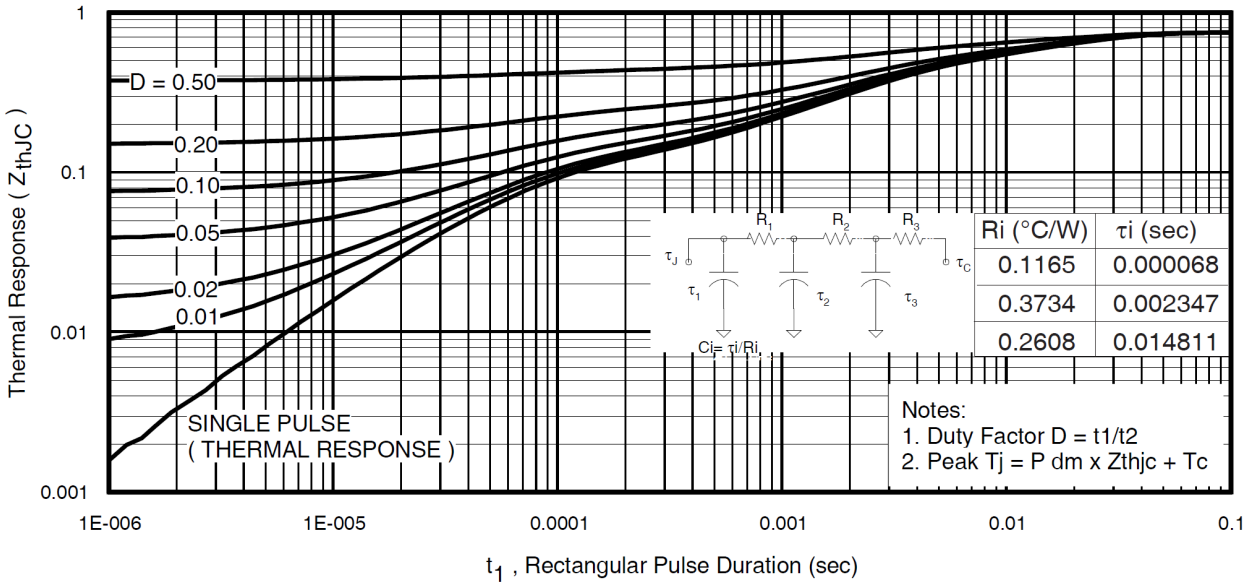


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

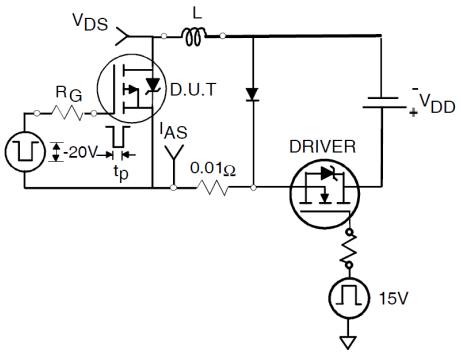


Fig 12a. Unclamped Inductive Test Circuit

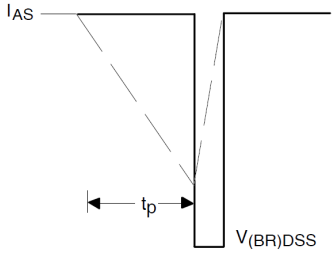


Fig 12b. Unclamped Inductive Waveforms

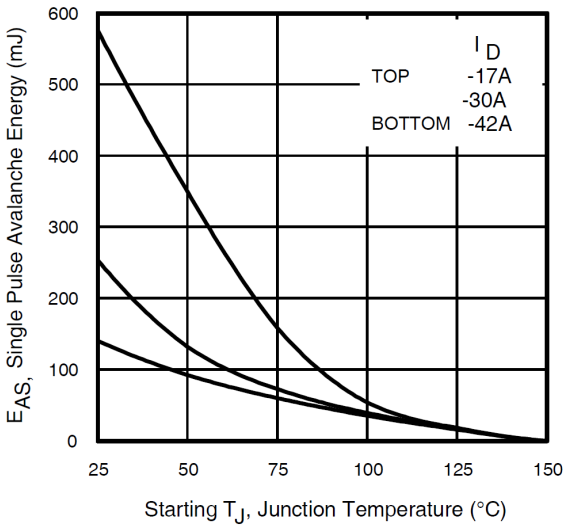


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

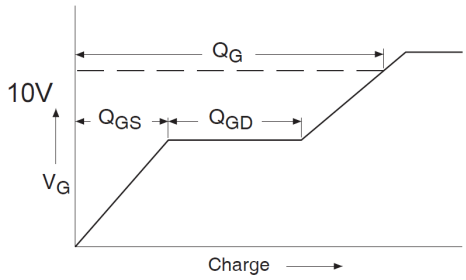


Fig 13a. Basic Gate Charge Waveform

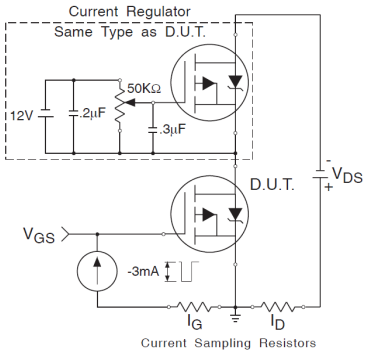


Fig 13b. Gate Charge Test Circuit

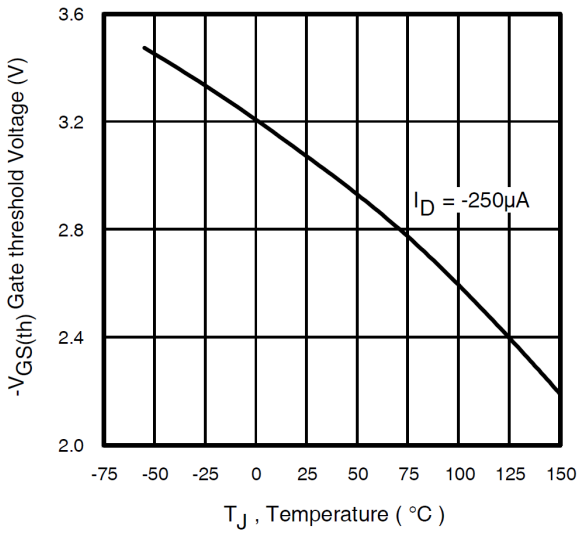


Fig 14. Threshold Voltage Vs. Temperature

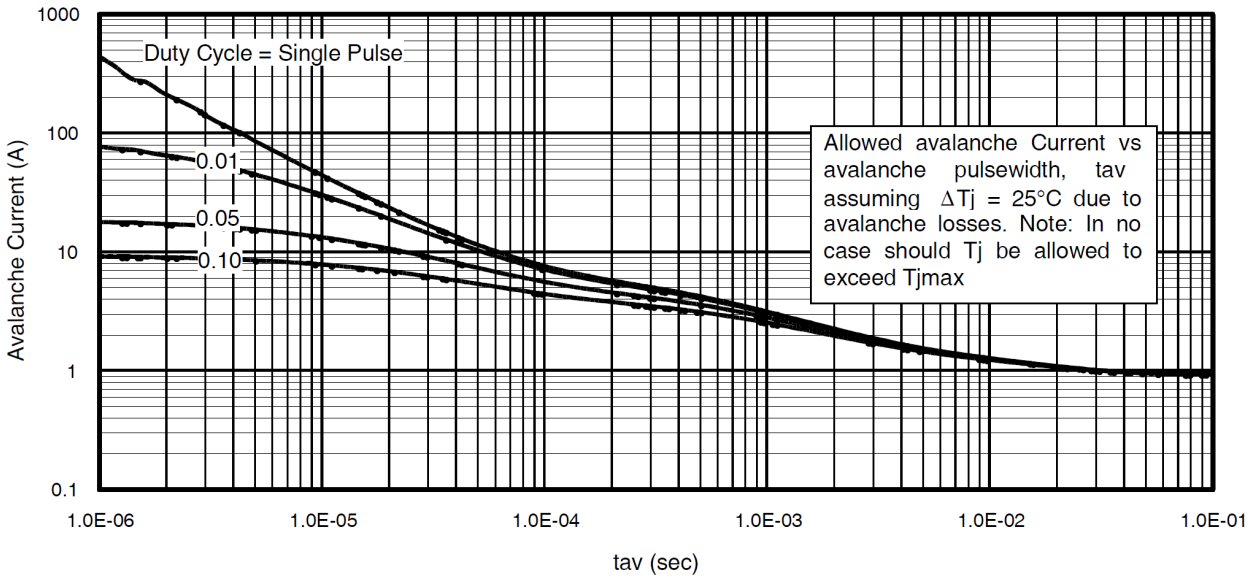


Fig 15. Typical Avalanche Current Vs.Pulsewidth

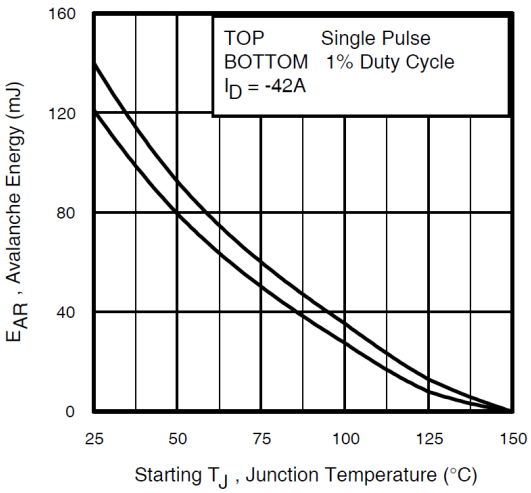


Fig 16. Maximum Avalanche Energy Vs. Temperature

关于重复的雪崩曲线的注释，图 15、16：（更多信息，请参见**www.infineon.com**上的 AN-1005）

1. 雪崩失效假设：
   纯粹的热现象和失效发生在结温远超 T_{jmax} 的情况下。这对每种零件类型都是有效的。
2. 只要不超过 T_{jmax}，就可以在雪崩中安全运行。
3. 如下公式基于图 12a、12b 所示的电路和波形。
4. $P_{D\,(ave)}$ = 每个雪崩脉冲的平均功率耗散。
5. BV = 额定击穿电压（1.3 倍系数，考虑雪崩期间的电压增加）。
6. I_{av} = 可允许的雪崩电流。
7. Δ T = 可允许的结温上升，不得超过 T_{jmax} （图 15、16 中假设为 25°C）。
   t_{av} = 雪崩的平均时间。
   D = 雪崩占空比 = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = 瞬态热阻抗，见图 11)

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

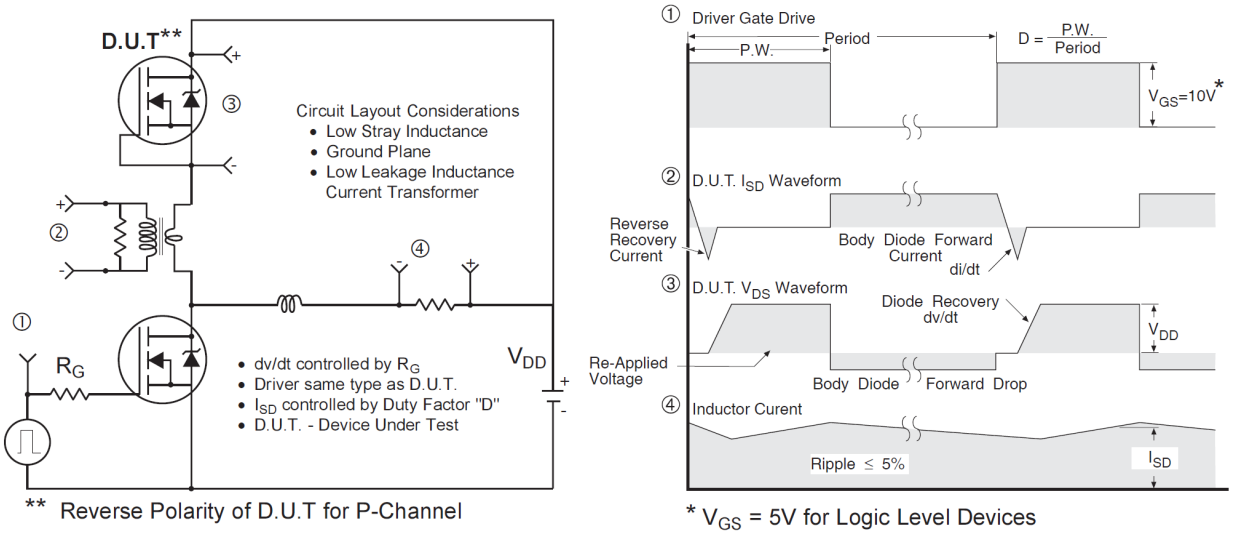


Fig 17. Peak Diode Recovery dv/dt Test Circuit for P-Channel

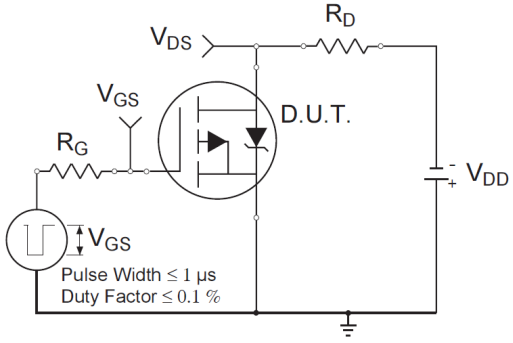


Fig 18a. Switching Time Test Circuit

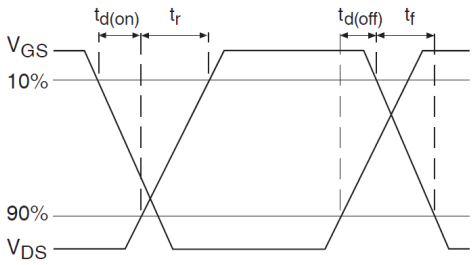
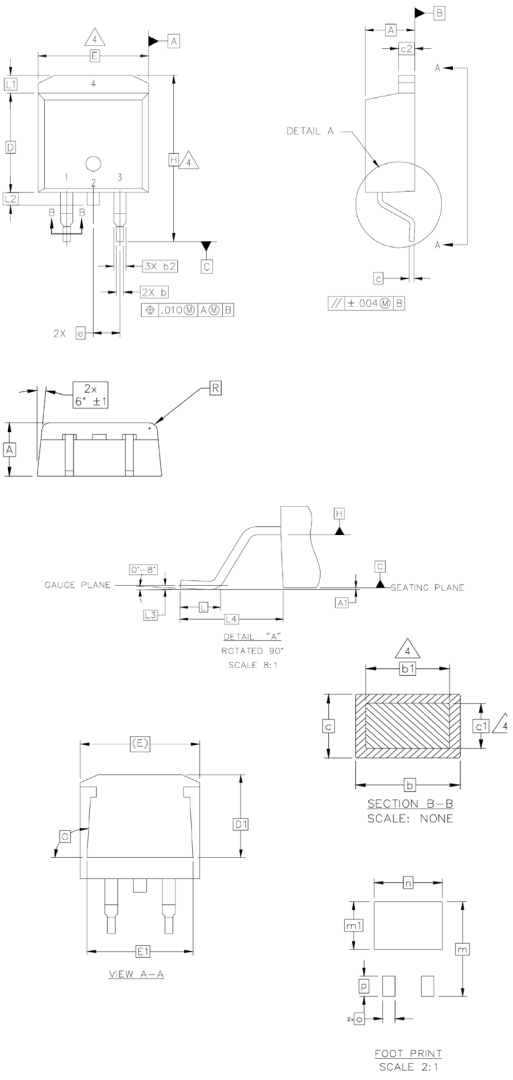


Fig 18b. Switching Time Waveforms

D 2 PAK-7TP 封装外形（尺寸以毫米（英寸）为单位）



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	4
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

DIODES

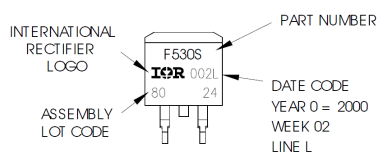
1.- ANODE *
2, 4.- CATHODE
3.- ANODE

* PART DEPENDENT.

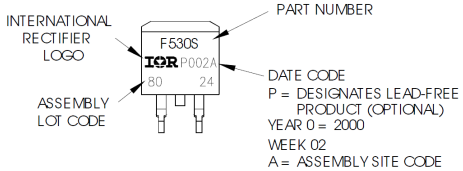
D 2 Pak 零件标识信息

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

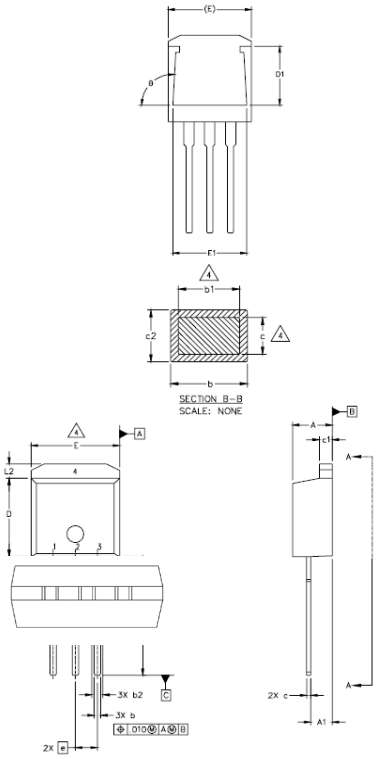
Note: "P" in assembly line position indicates "Lead-Free"



OR



TO-262 封装外形（尺寸以毫米（英寸）为单位）



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET	IGBT
1.– GATE	1- GATE
2.– DRAIN	2- COLLECTOR
3.– SOURCE	3- EMITTER
4.– DRAIN	4- COLLECTOR

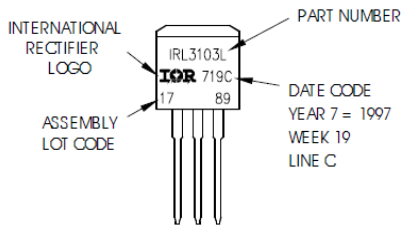
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4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

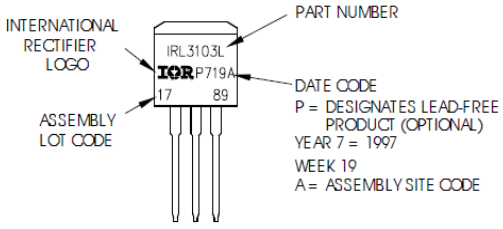
TO-262 零件标记信息

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

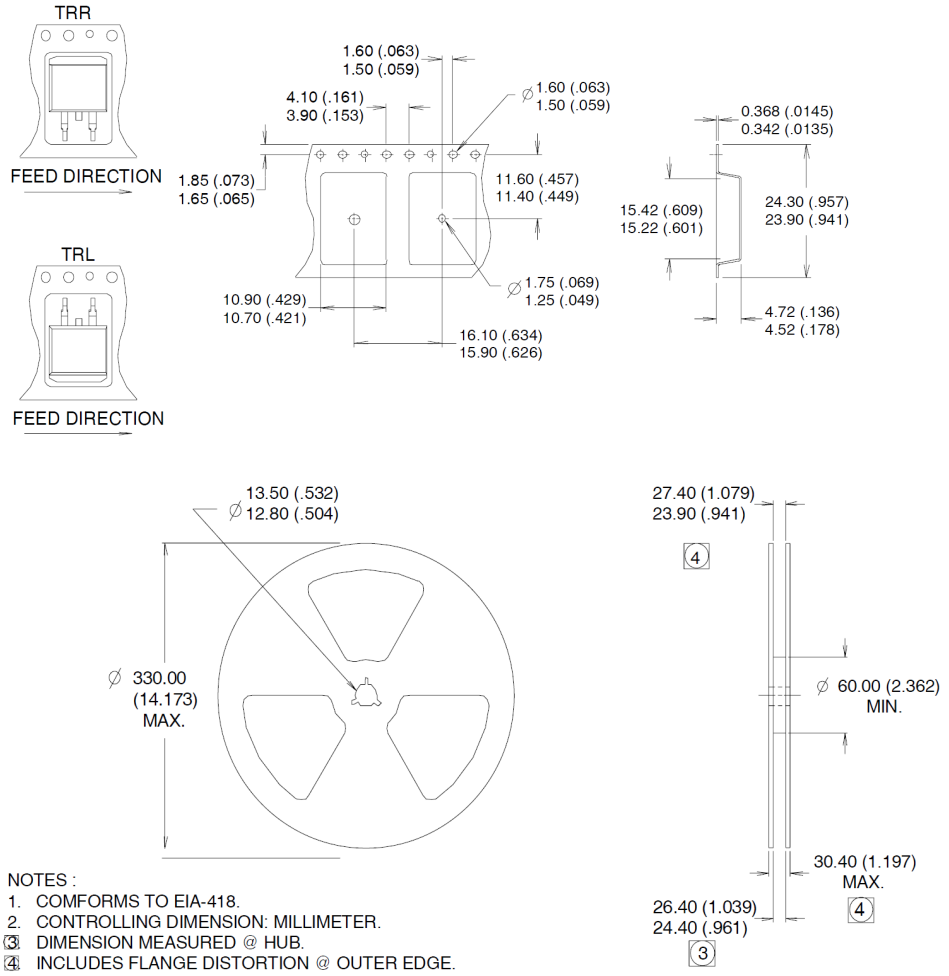
Note: "P" in assembly line position indicates "Lead-Free"



OR



D2Pak 胶带 & 卷筒信息



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

①重复的额定值；脉冲宽度受最高结温限制。（见图11）

②受TJmax限制，初始TJ = 25°C，L = 0.16mH

R_G = 25Ω, I_{AS} = -42A, V_{GS} =-10V.

不建议将部件用于高于此值。

③脉冲宽度≤ 1.0μσ；占空比≤ 2%。

④ C_{oss} eff. 是一个固定电容值， 当 V_{DS} 从 0 上升至 80% V_{DSS} 时，其充电时间与 C_{oss} 相同。

⑤受 T Jmax 限制 ，典型重复的雪崩性能见图 12a、12b、15、16。

⑥ 该值根据样片失效数据确定。100 % 已在生产环境中测试过该数值。

⑦这适用于安装在 1 英寸方形PCB （FR-4 或 G-10 材料）上的 D2Pak。有关建议的封装和焊接技术，请参考应用笔记 #AN-994。

⑧R_θ 在 TJ 约90°C 时测量

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