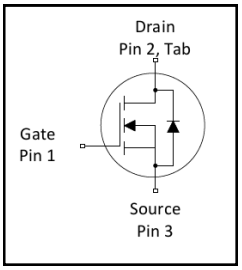
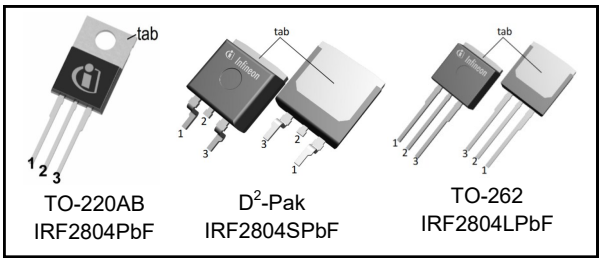
$V_{(BR)DSS}$	40V
$R_{DS(on)}$	2.0mΩ ⑨
I_D	75A





Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

G	D	S
Gate	Drain	Source

Description

This HEXFET Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF2804PbF	TO-220	Tube	50	IRF2804PbF
IRF2804SPbF	D^2-Pak	Tape and Reel	800	IRF2804SPbF
IRF2804LPbF	TO-262	Tube	50	IRF2804LPbF

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	270	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (See Fig. 9)	190	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	1080	
P_D @T_C = 25°C	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited)②	540	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑦	1160	
I_{AR}	Avalanche Current ①	See Fig. 12a,12b,15,16	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.50⑩	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑧	——	40	

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.031	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$ SMD	Static Drain-to-Source On-Resistance	—	1.5	2.0	mΩ	V_{GS} = 10V, I_D = 75A ④
$R_{DS(on)}$ TO-220	Static Drain-to-Source On-Resistance	—	1.8	2.3	mΩ	V_{GS} = 10V, I_D = 75A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 150µA
gfs	Forward Trans conductance	130	—	—	S	V_{DS} = 10V, I_D = 75A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 40V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	—	160	240	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge	—	41	62		V_{DS} = 32V
Q_{gd}	Gate-to-Drain Charge	—	66	99		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 20V
t_r	Rise Time	—	120	—		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	130	—		R_G= 2.5Ω
t_f	Fall Time	—	130	—		V_{GS} = 10V④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contac
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	6450	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1690	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	840	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	5350	—		V_{GS} = 0V,V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	1520	—		V_{GS} = 0V,V_{DS} = 32V, f = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance	—	2210	—		V_{GS} = 0V,V_{DS} = 0V to 32V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	270	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	1080		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 75A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	56	84	ns	T_J = 25°C ,I_F = 75A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	—	67	100	nC	di/dt = 100A/µs ④

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax} starting T_J = 25°C, L = 0.24mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} =10V. Part not recommended for use above this value.

③ I_{SD} ≤ 75A, di/dt ≤ 220A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑦ This value determined from sample failure population. 100% tested to this value in production.

⑧ This is applied to D^2 Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note# AN-994.

⑨ Max $R_{DS(on)}$ for D^2 Pak and TO-262 (SMD) devices.

⑩ TO-220 device will have an Rth value of 0.45°C/W.

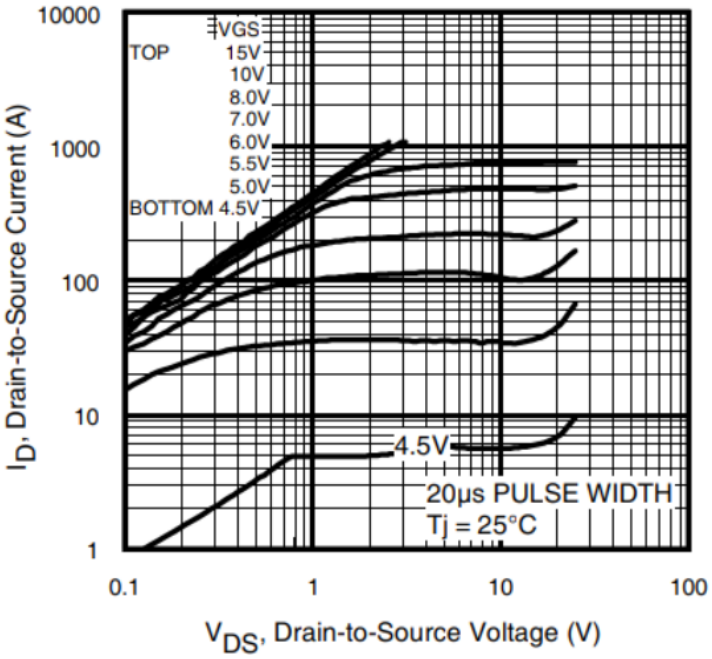


Fig. 1 Typical Output Characteristics

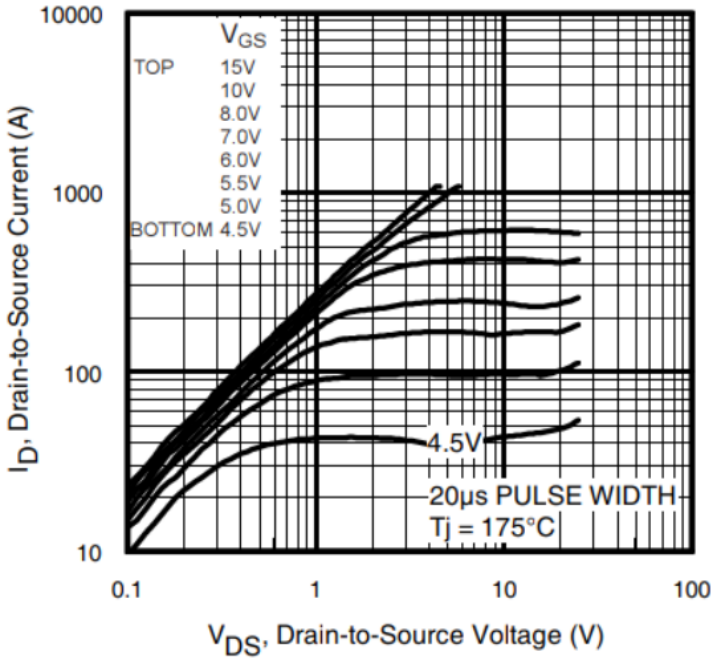


Fig. 2 Typical Output Characteristics

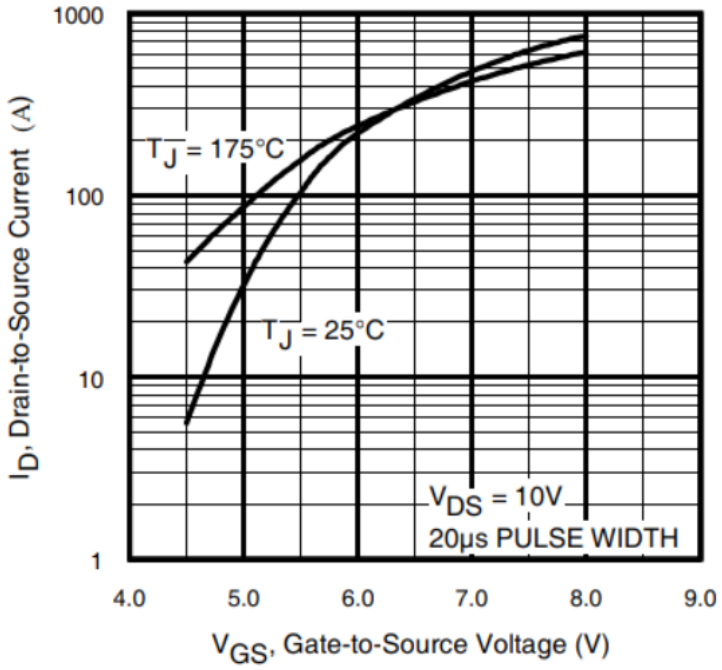


Fig. 3 Typical Transfer Characteristics

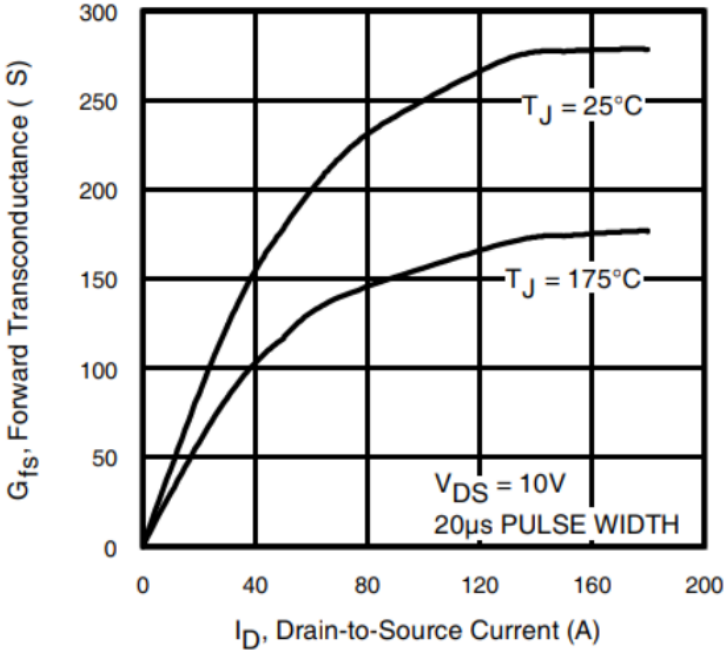


Fig. 4 Typical Forward Transconductance vs. Drain Current

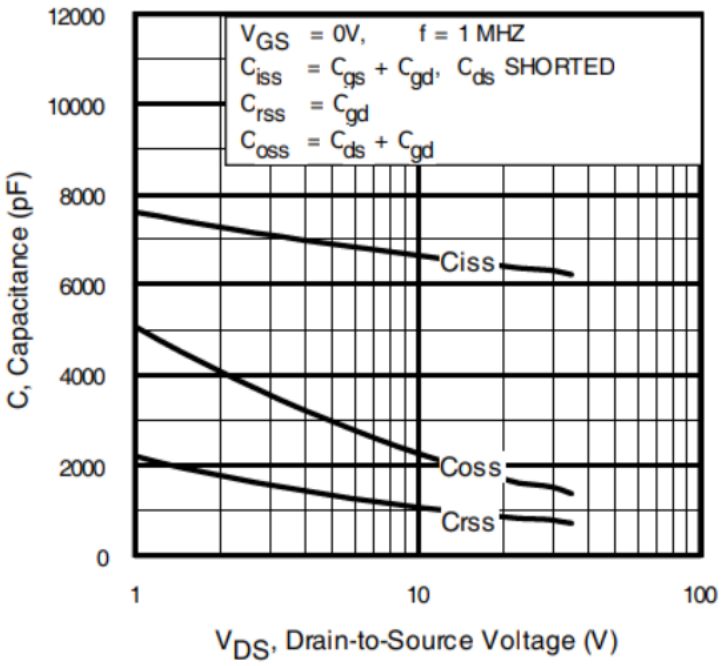


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

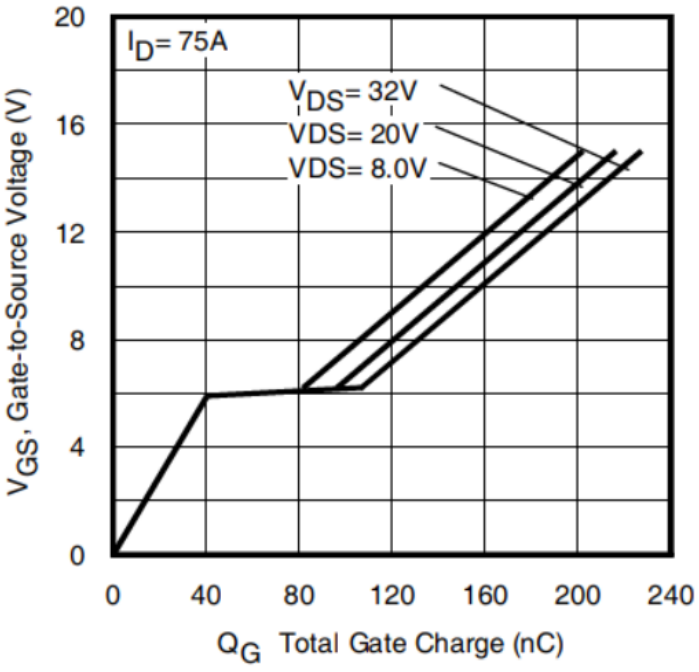


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

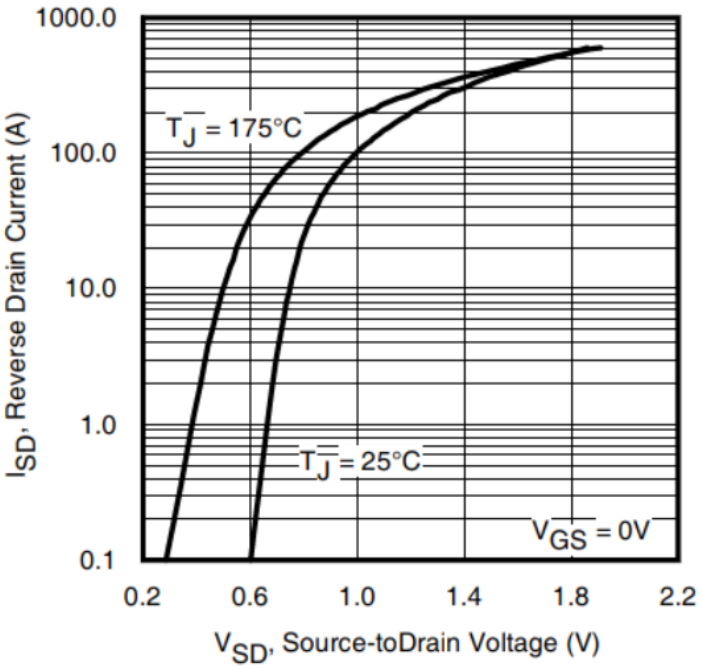


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

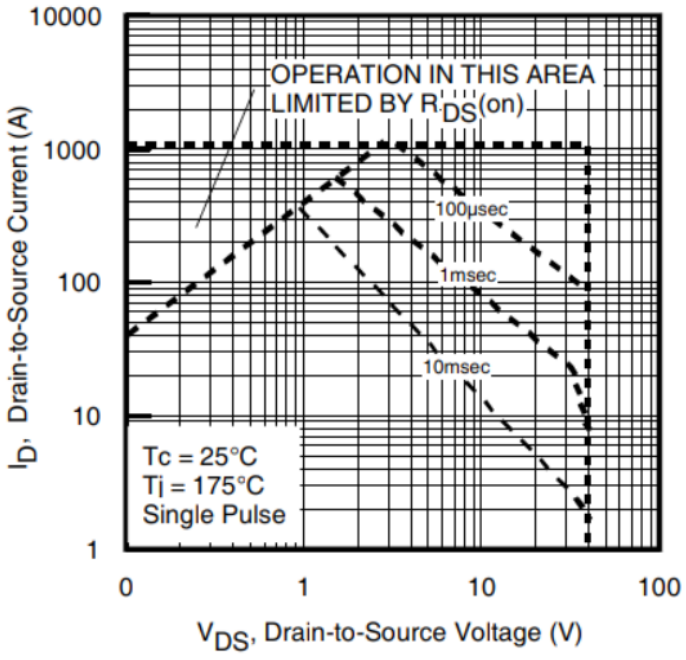


Fig 8. Maximum Safe Operating Area

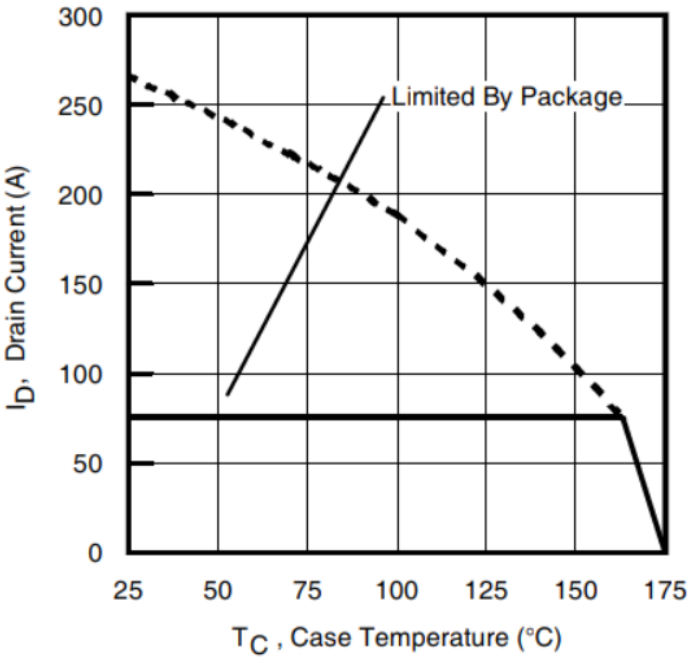


Fig 9. Maximum Drain Current vs. Case Temperature

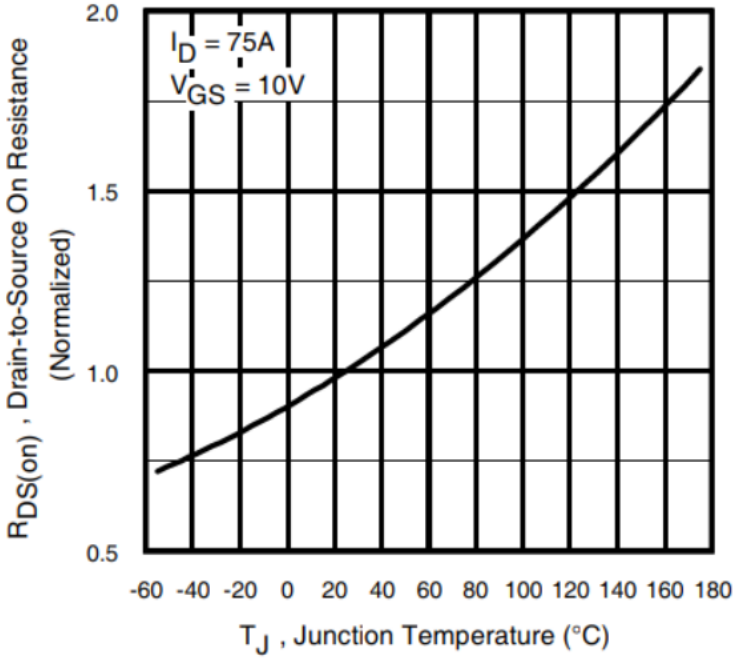


Fig 10. Normalized On-Resistance vs. Temperature

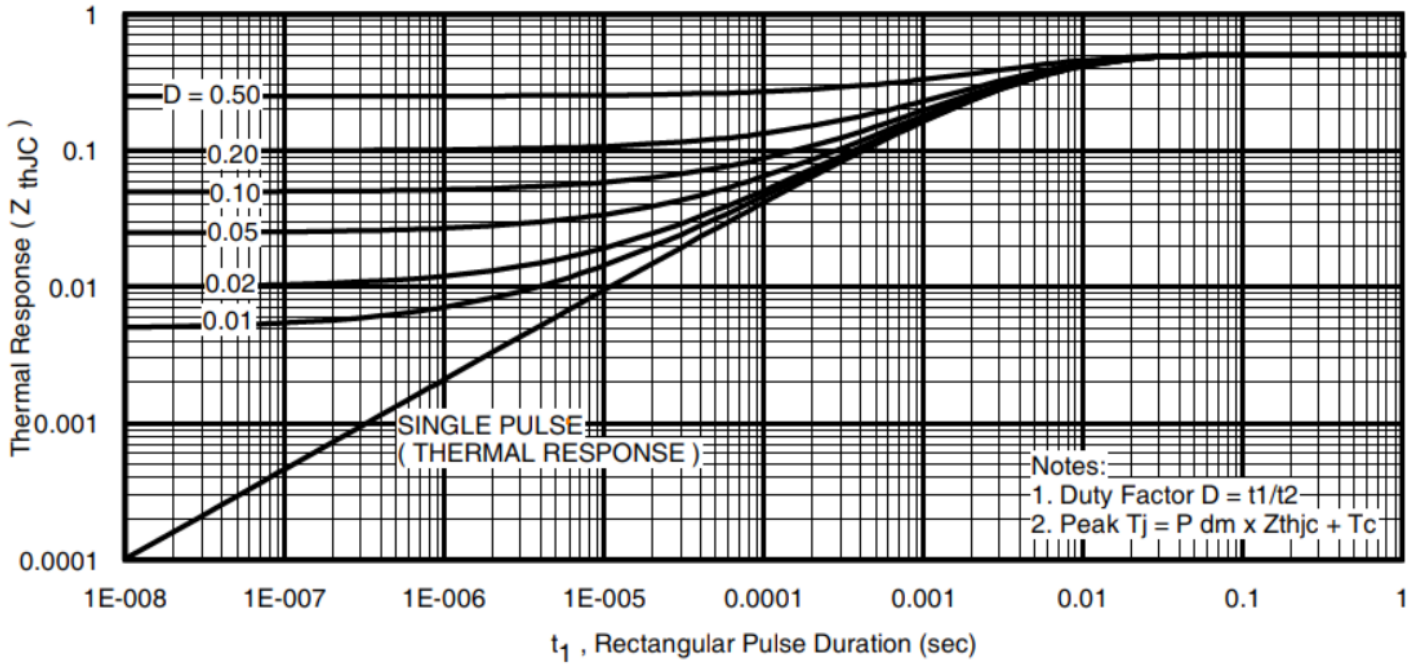


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

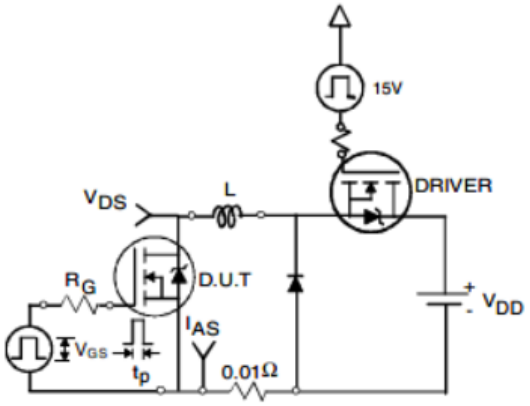


Fig. 12a. Unclamped Inductive Test Circuit

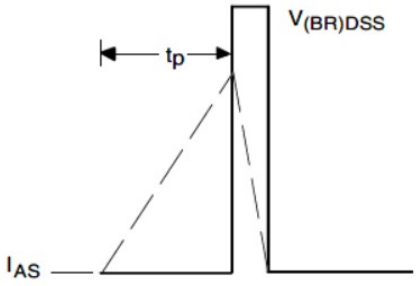


Fig. 12b. Unclamped Inductive Waveforms

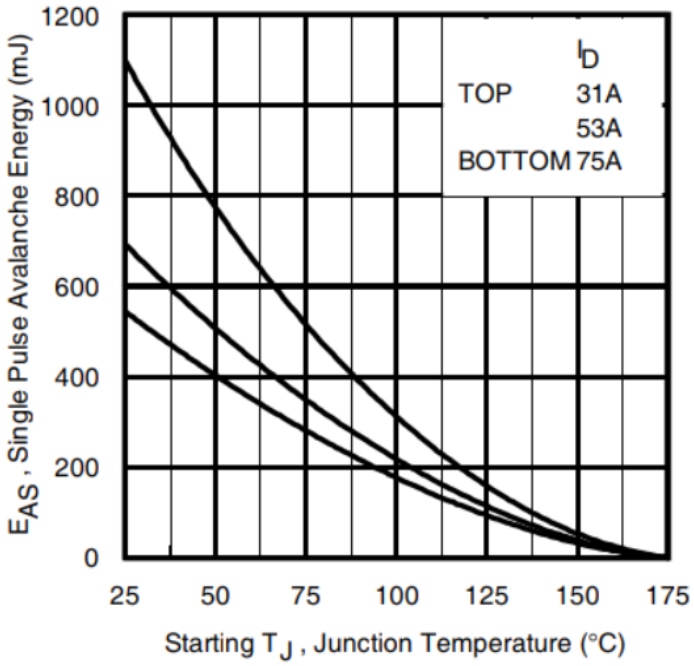


Fig 12c. Maximum Avalanche Energy vs. Drain Current

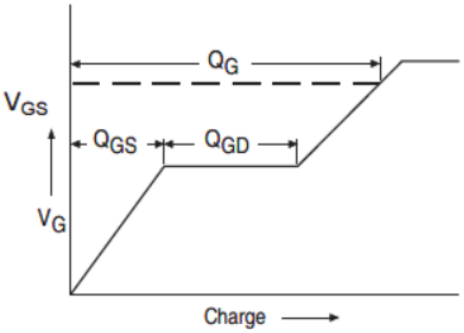


Fig 13a. Basic Gate Charge Waveform

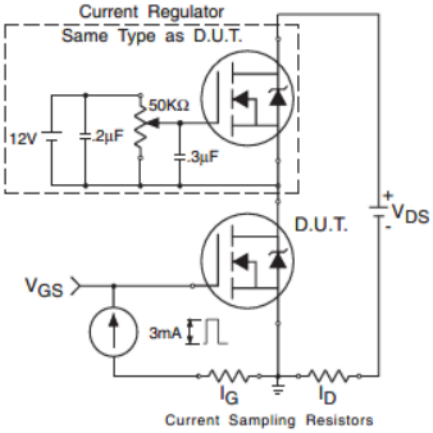


Fig 13b. Gate Charge Test Circuit

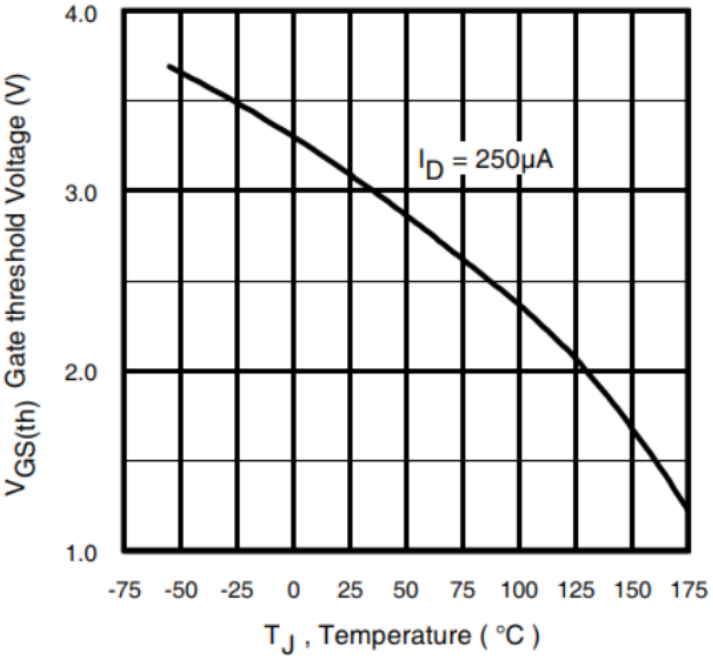


Fig. 14 Threshold Voltage vs. Temperature

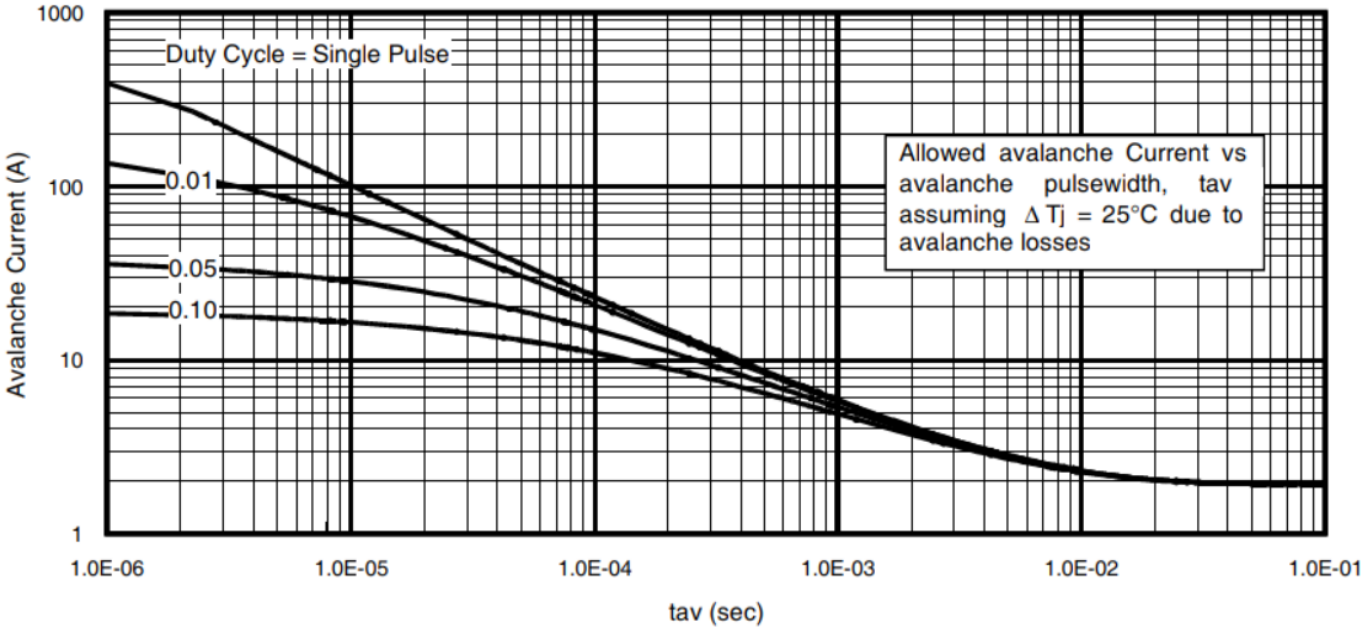


Fig 15. Typical Avalanche Current vs. Pulse Width

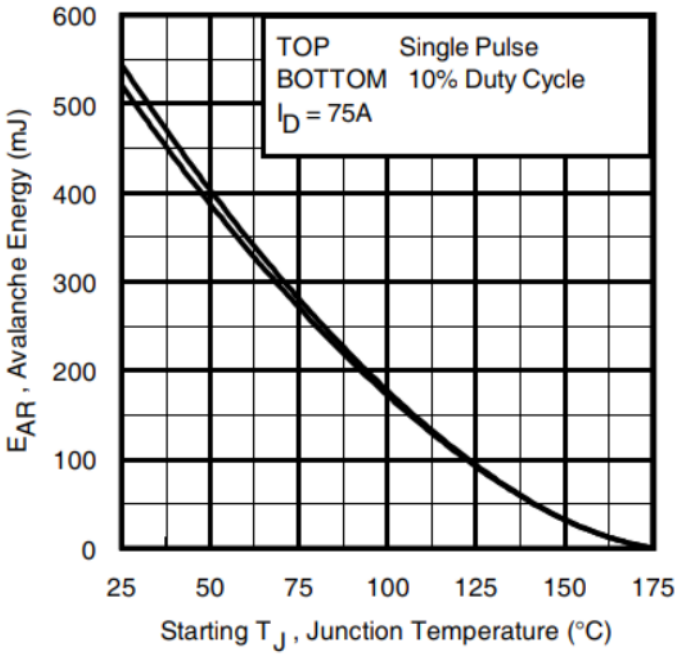


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$\mathbf{PD\ (ave) = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}}$$

$$\mathbf{I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]}$$

$$\mathbf{E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}}$$

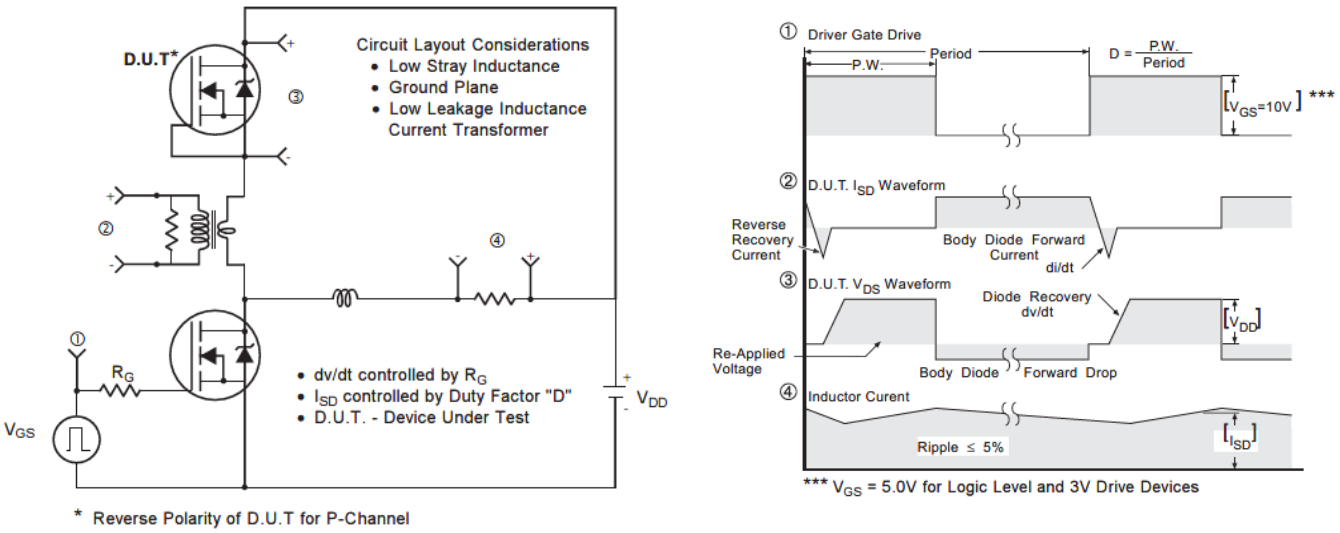


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

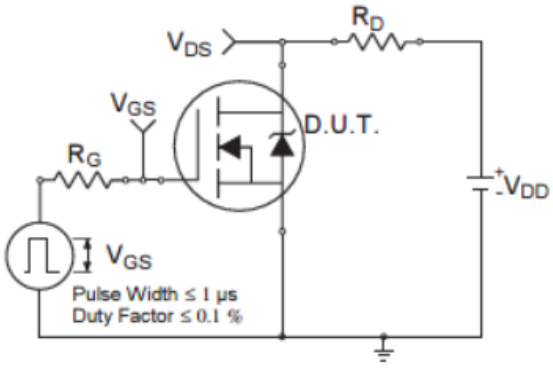


Fig 18a. Switching Time Test Circuit

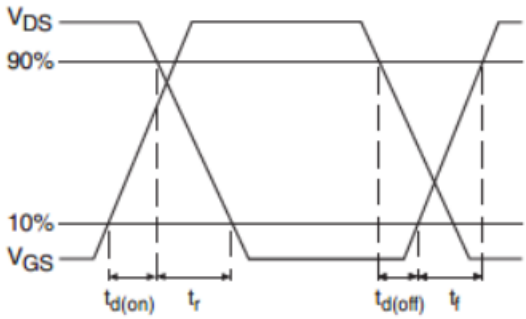
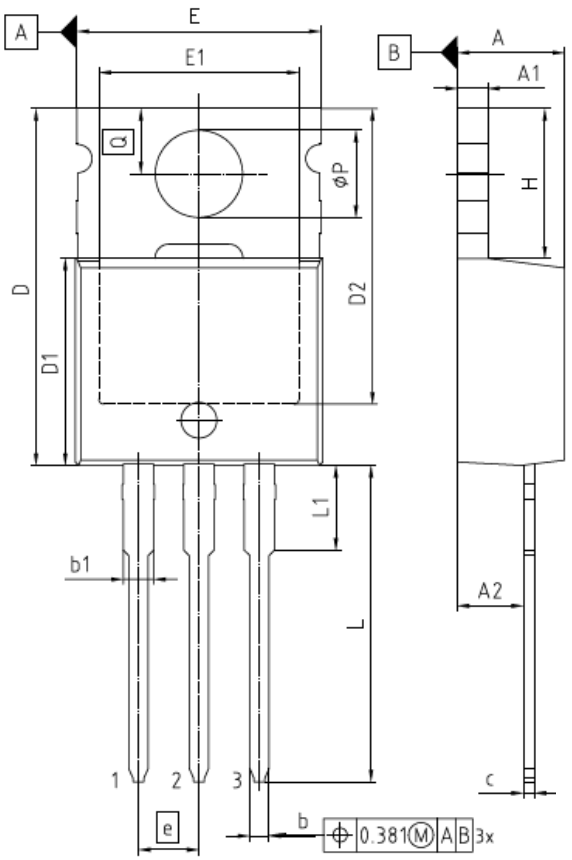


Fig 18b. Switching Time Waveforms

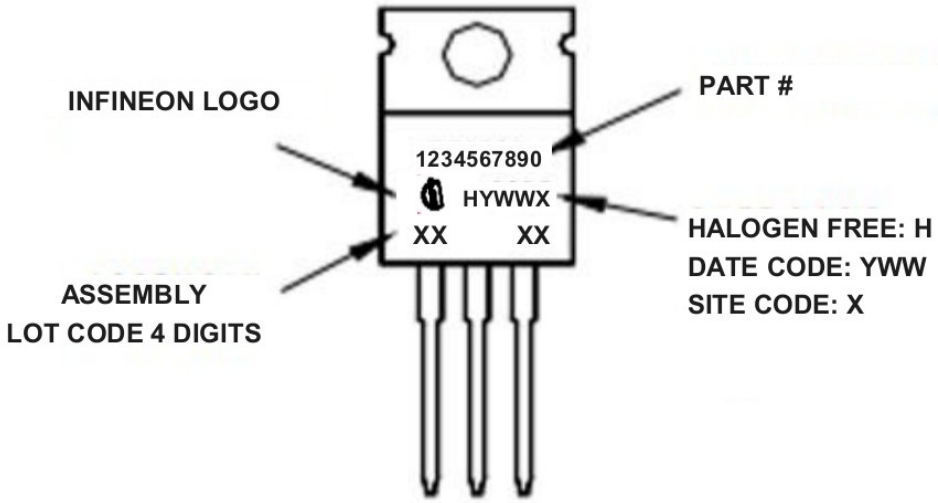
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

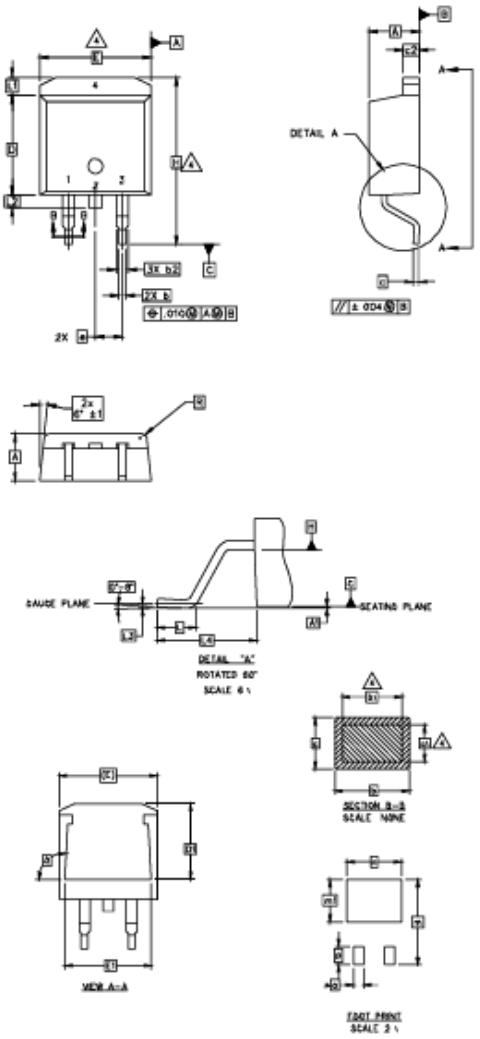
PACKAGE - GROUP NUMBER:	PG-TO220-3-U05	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

D² Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	4
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

DIODES

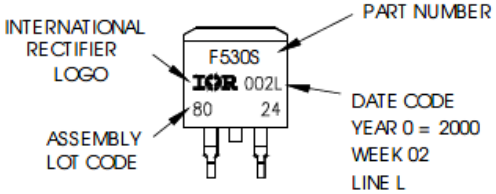
1.– ANODE *
2, 4.– CATHODE
3.– ANODE

* PART DEPENDENT.

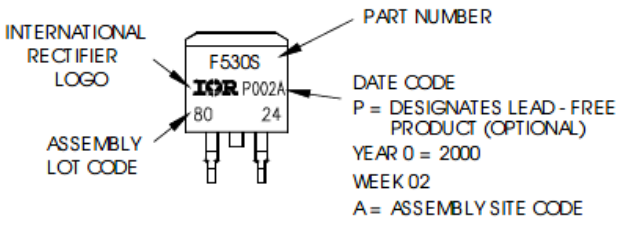
D² Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

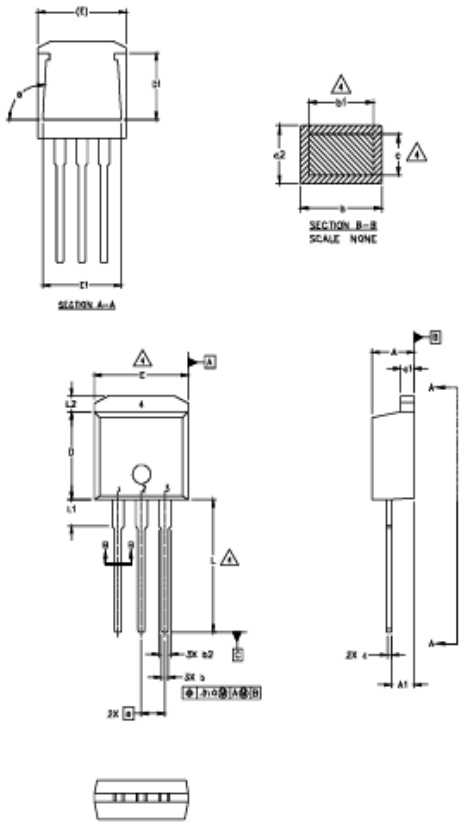
Note. "P" in assembly line position indicates "Lead – Free"



OR



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

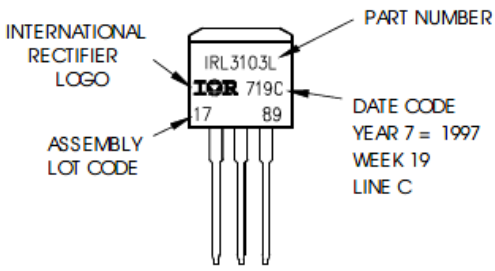
IGBT
1 – GATE
2 – COLLECTOR
3 – EMITTER

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

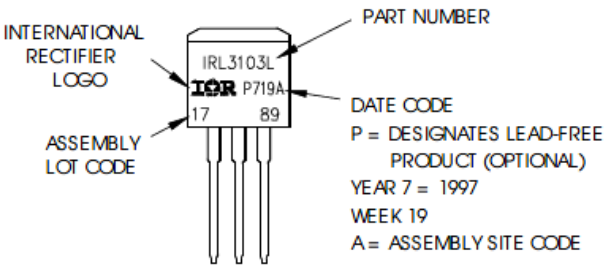
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

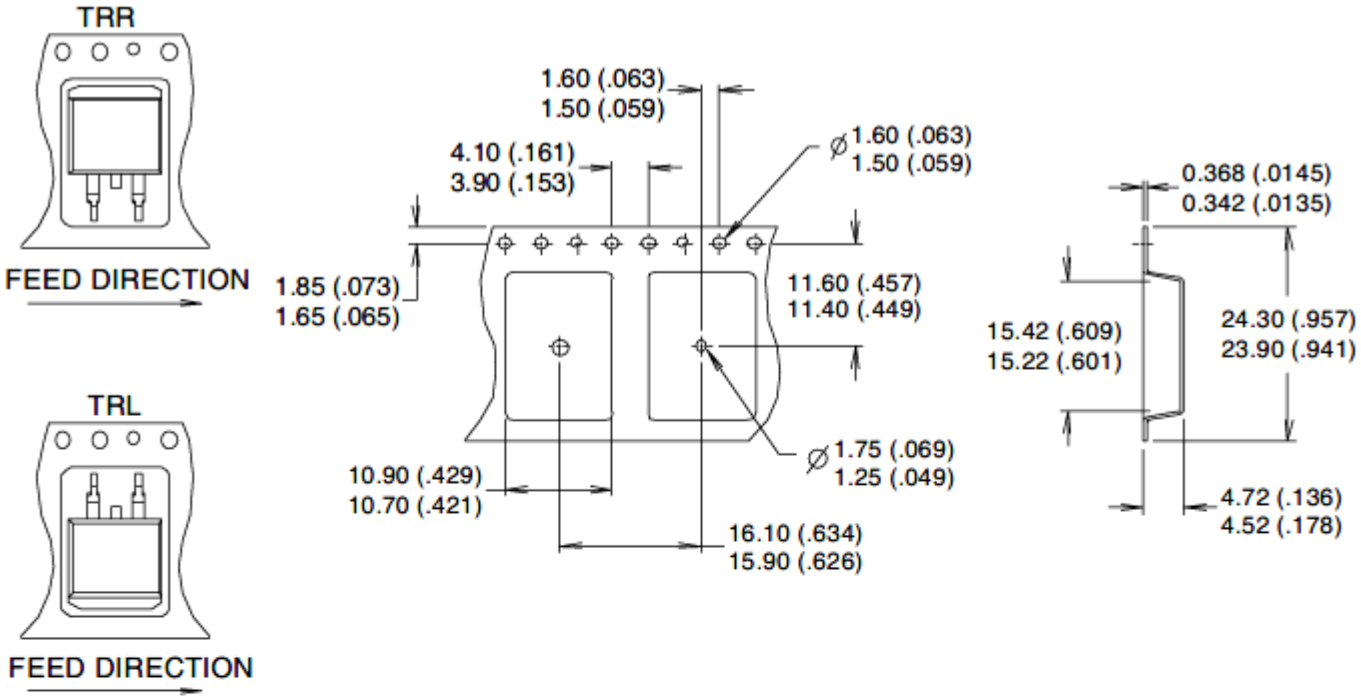
Note: "P" in assembly line position indicates "Lead – Free"

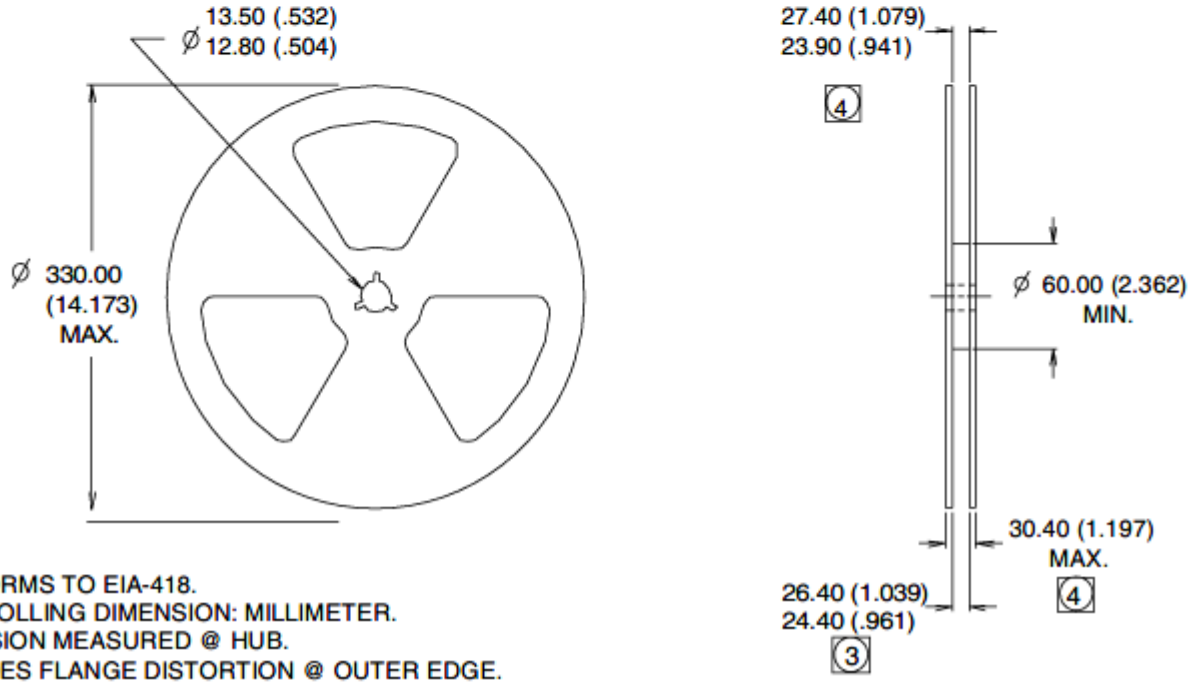


OR



D² Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Revision History

Date	Rev.	Comments
2026-09-01	2.1	• Update datasheet to Infineon format • Updated Package Outline and Part marking –page 9 • Added disclaimer on last page.

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