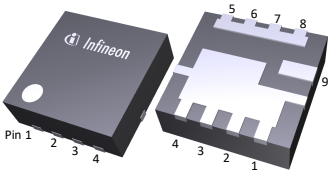
MOSFET

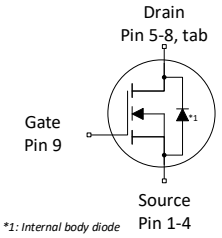
PG-TTFN-9 (3x3)

OptiMOS™ 5 Power-Transistor, 100 V



Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

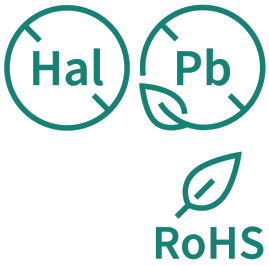


Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	6.5	mΩ
I_D	85	A
Q_{oss}	40	nC
Q_G(0V..10V)	34	nC



Part number	Package	Marking	Related links
IQE065N10NM5CG	PG-TTFN-9	06510C5	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	85	A	V_{GS}=10 V, T_C=25 °C
				60		V_{GS}=10 V, T_C=100 °C
				14		V_{GS}=10V, T_A=25°C, R_{thJA}=60°C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	341	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	147	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	100	W	T_C=25 °C
				2.5		T_A=25 °C, R_{thJA}=60 °C/W [3]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.8	1.5	°C/W	-
Device on PCB, 6 cm^2 cooling area [5]	R_{thJA}		-	60		

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=48 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1.0	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	5.7	6.5	mΩ	V_{GS}=10 V, I_D=20 A
			7.2	11		V_{GS}=6 V, I_D=10 A
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance	g_{fs}	-	55	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	2300	3000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [6]	C_{oss}		340	440		
Reverse transfer capacitance [6]	C_{rss}		18	32		
Turn-on delay time	$t_{d(on)}$	-	8.9	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=3 Ω
Rise time	t_r		3.8			
Turn-off delay time	$t_{d(off)}$		21.1			
Fall time	t_f		7.5			

[6] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10.1	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		6.8	-	nC	
Gate to drain charge [8)]	Q_{gd}		7.4	11	nC	
Switching charge	Q_{sw}		10.7	-	nC	
Gate charge total [8)]	Q_g		34	42	nC	
Gate plateau voltage	$V_{plateau}$		4.4	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	29	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [8)]	Q_{oss}	-	40	54	nC	V_{DS}=50 V, V_{GS}=0 V

7) See "Gate charge waveforms" for parameter definition

8) Defined by design. Not subject to production test.

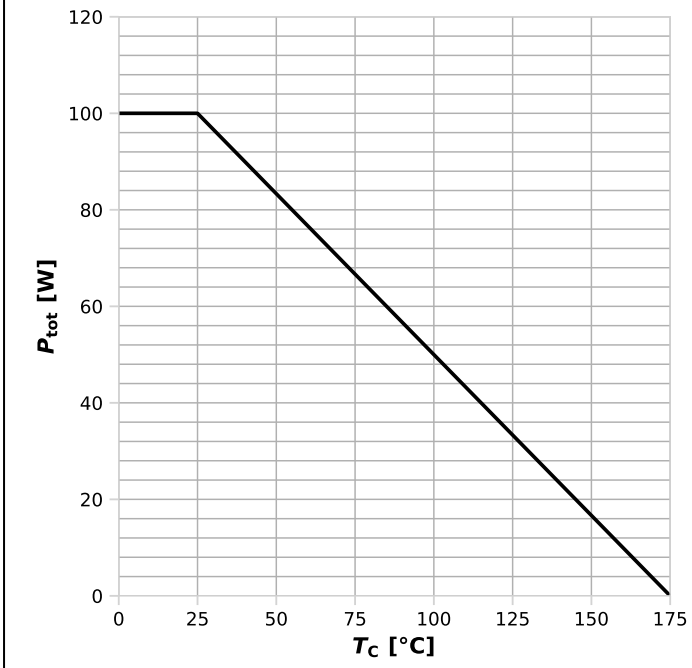
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	74	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			341		
Diode forward voltage	V_{SD}	-	0.83	1.1	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	36	72	ns	V_R=50 V, I_F=20 A, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}		40	80	nC	

9) Defined by design. Not subject to production test.

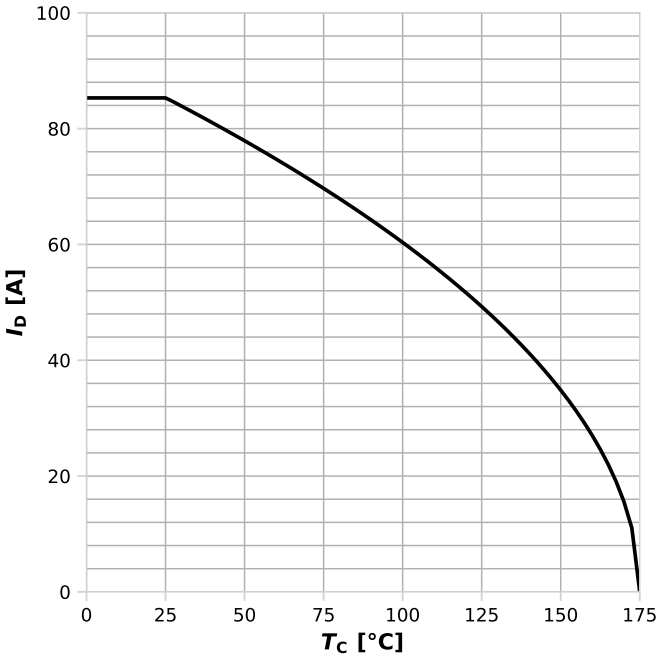
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



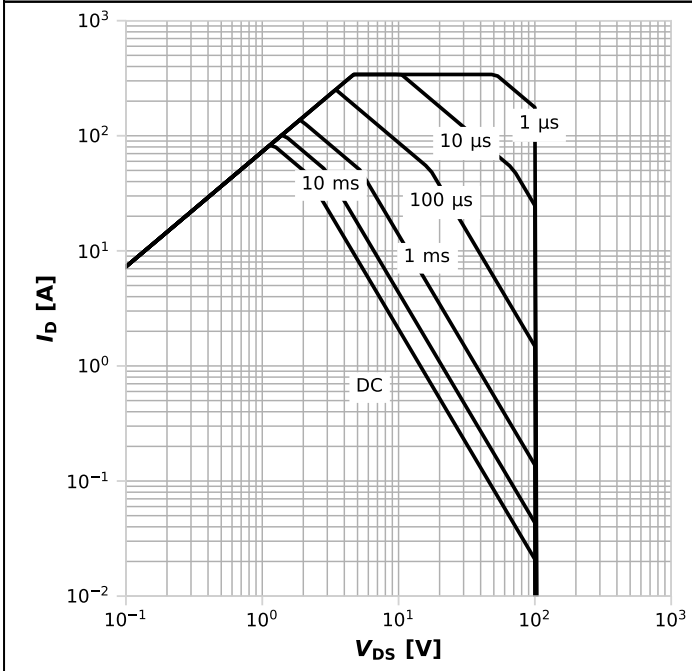
P_{tot}=f(T_C)

Diagram 2: Drain current



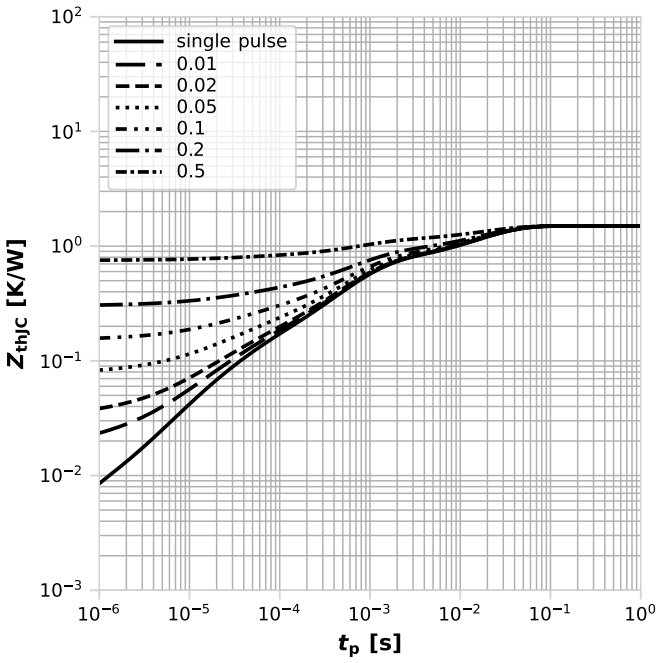
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



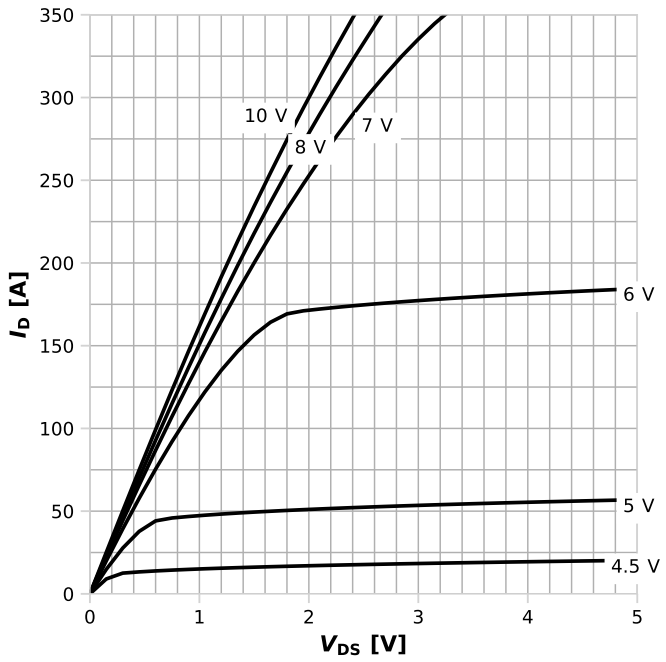
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



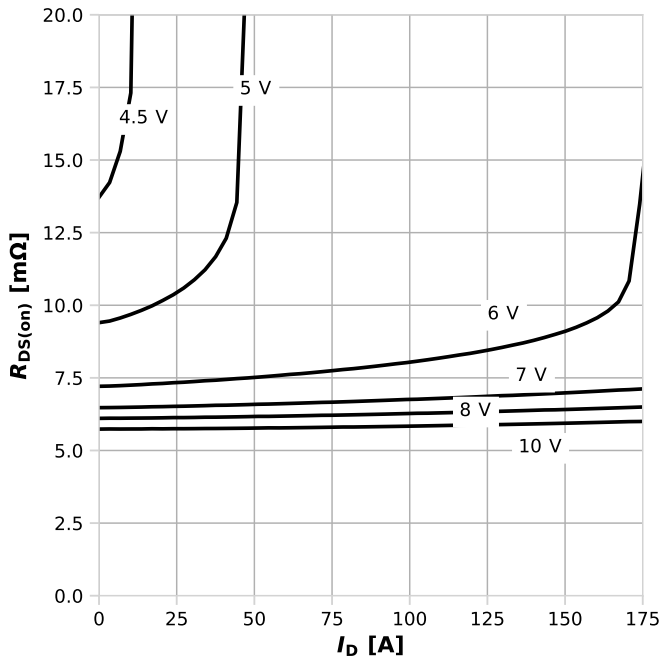
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



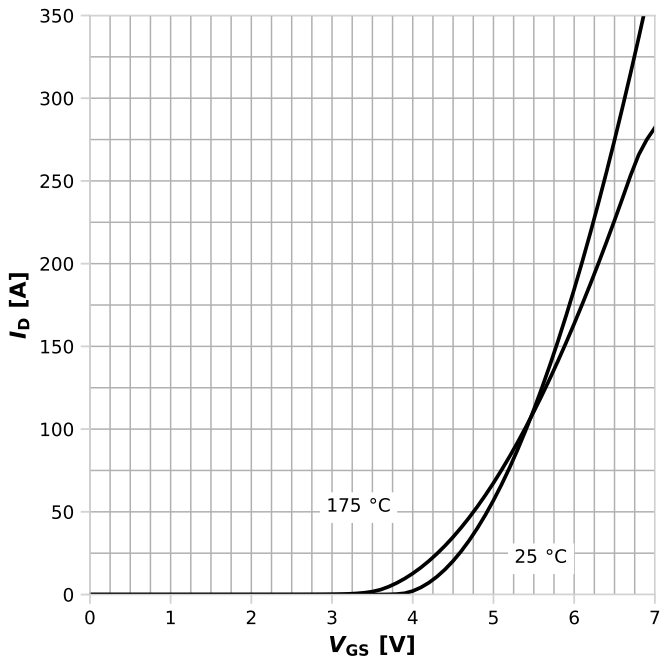
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



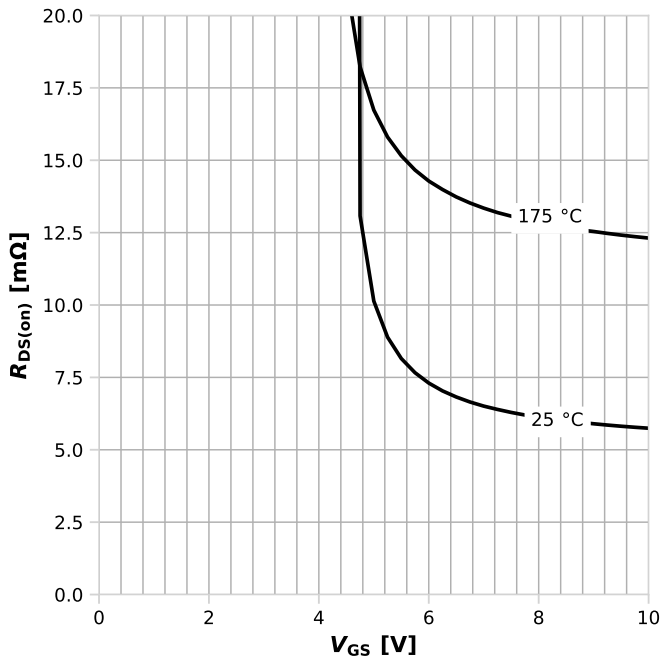
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=20 A; parameter: T_j

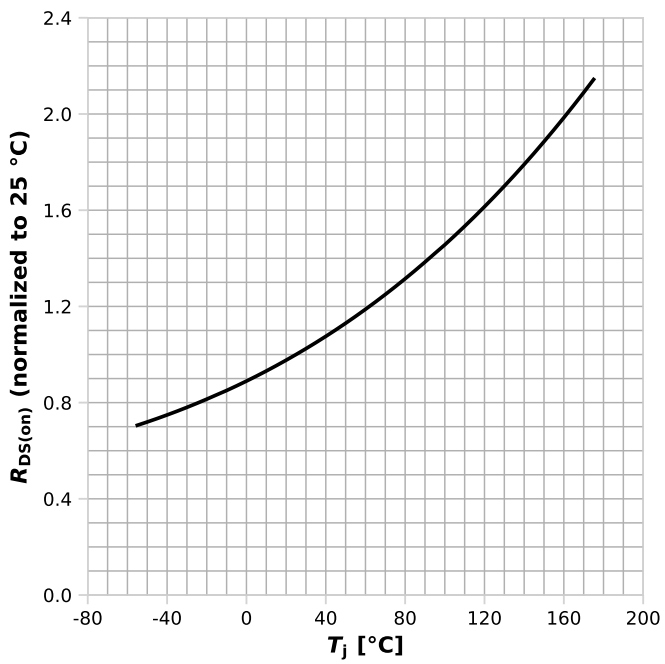
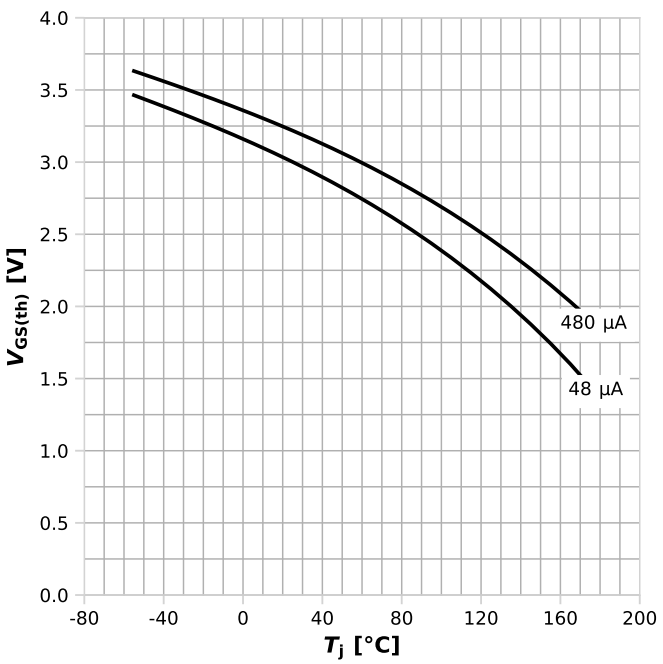
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=20 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

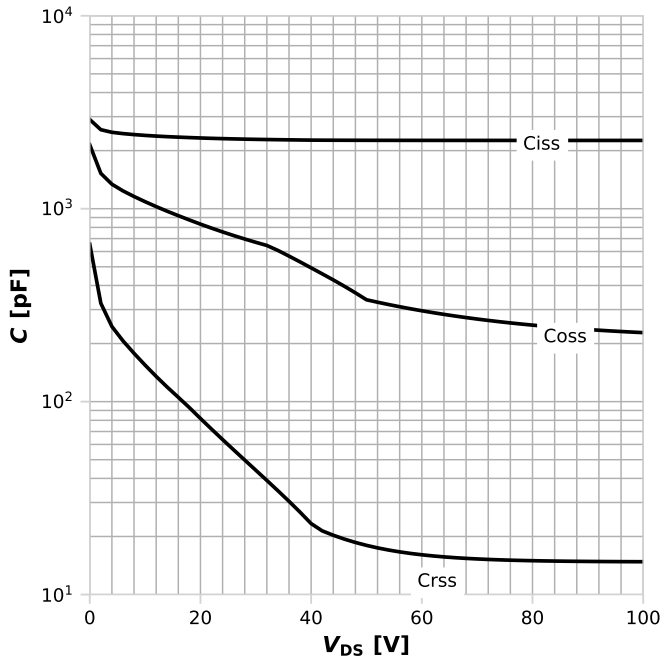
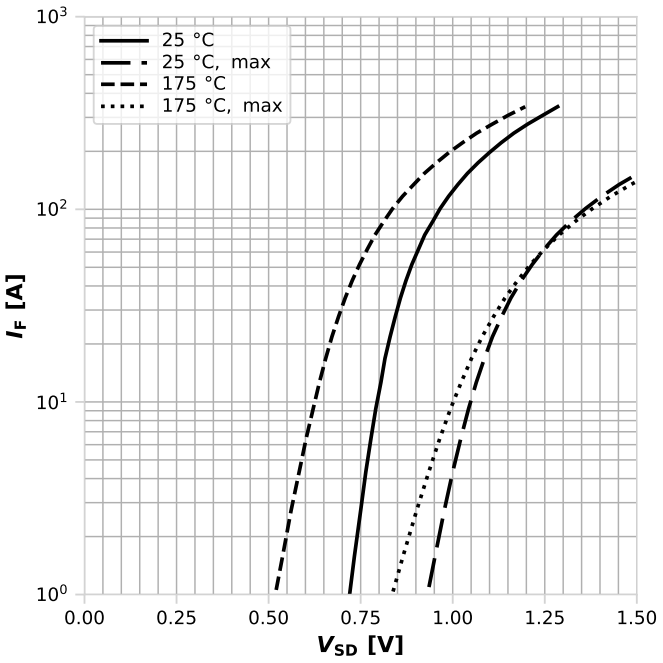
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

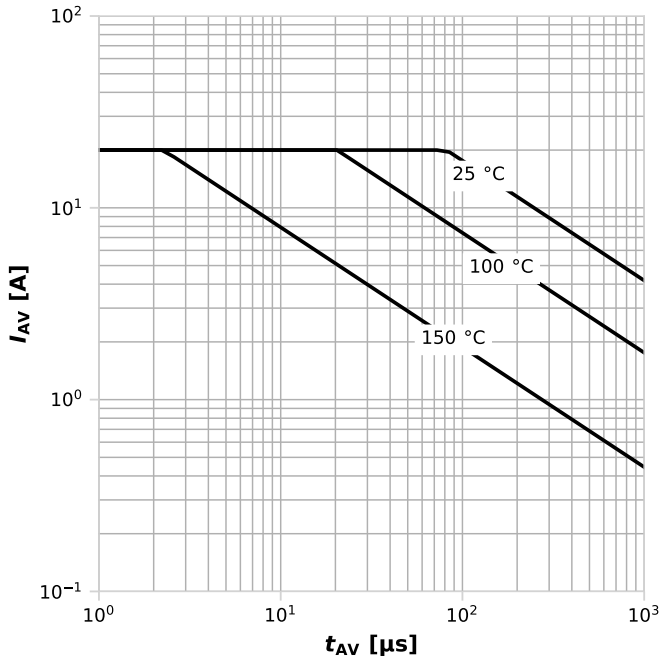
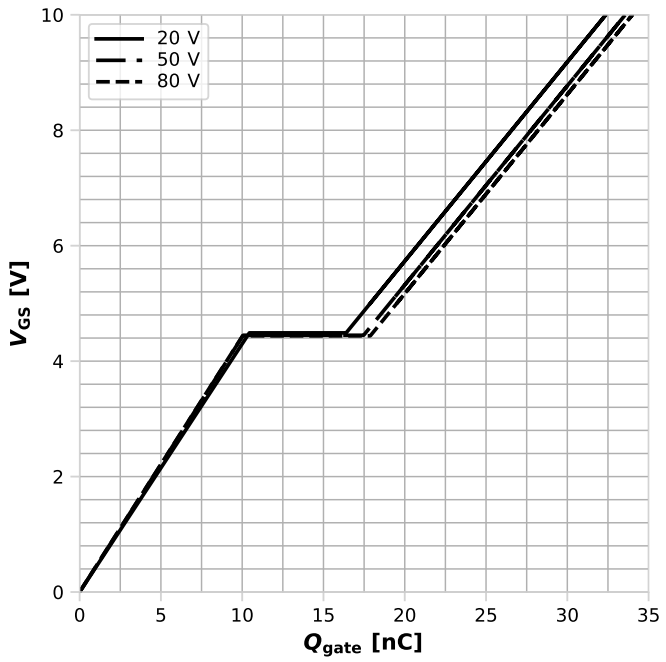
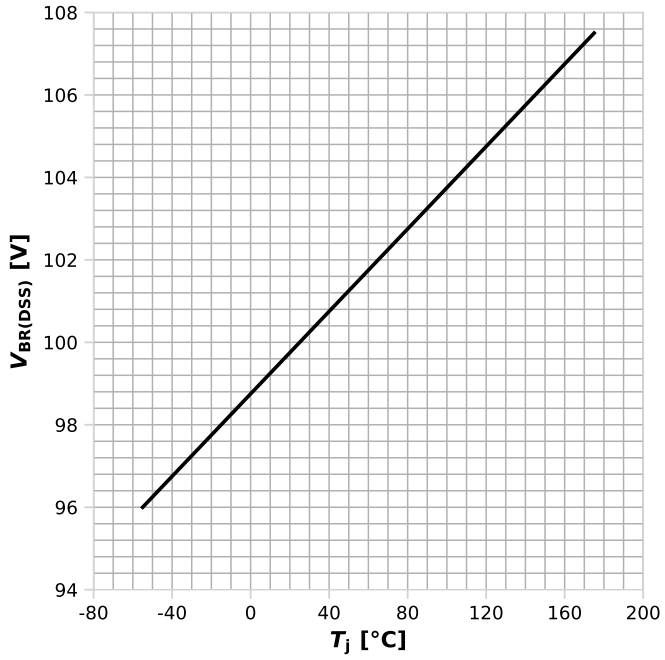
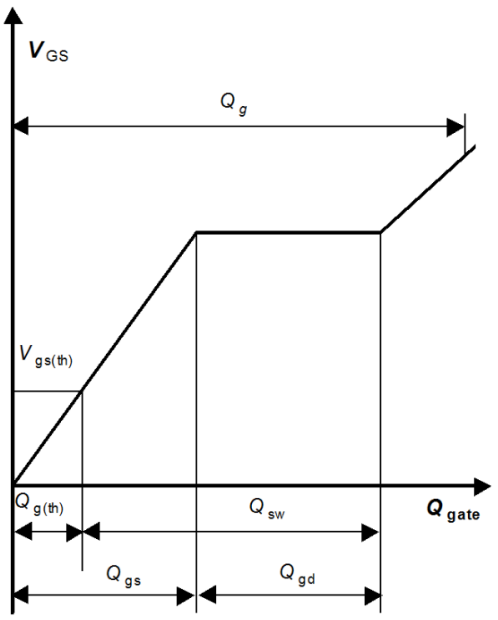
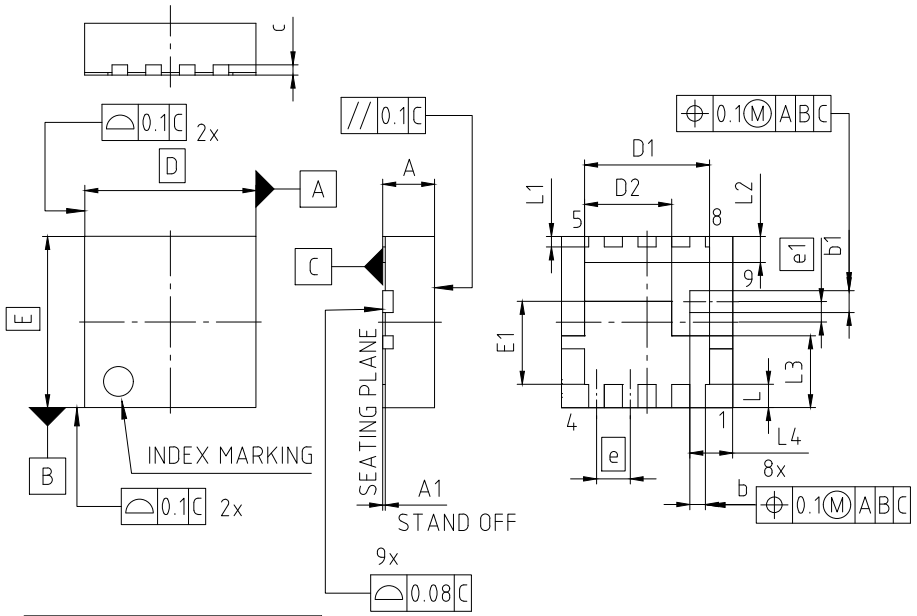
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=20 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TTFN-9-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	-	1.10
A1	-	0.05
b	0.20	0.40
b1	0.32	0.52
c	0.20	
D	3.30	
D1	2.31	2.51
D2	1.58	1.78
E	3.30	
E1	1.50	1.70
e	0.65	
e1	0.395	
L	0.35	0.55
L1	0.10	0.30
L2	0.40	0.60
L3	1.285	1.485
L4	0.725	0.925

Figure 1 Outline PG-TTFN-9, dimensions in mm

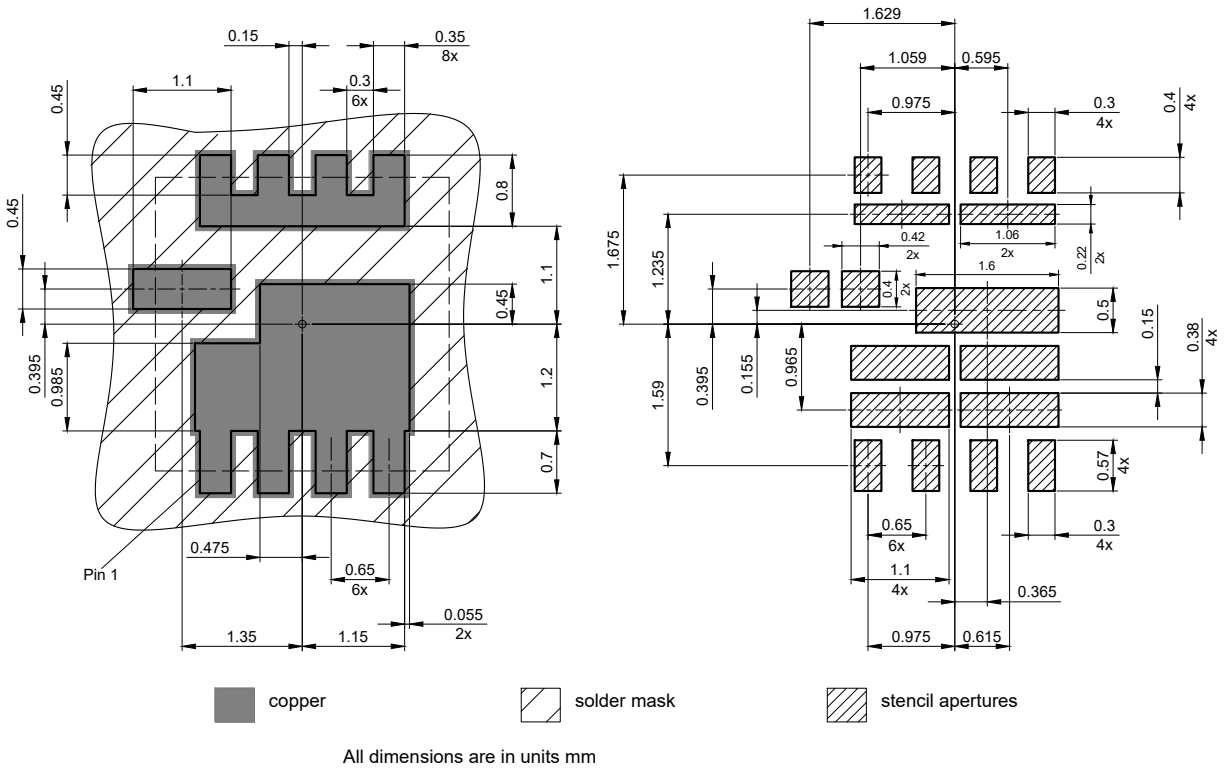


Figure 2 Boardpad drawing PG-TTFN-9, dimensions in mm

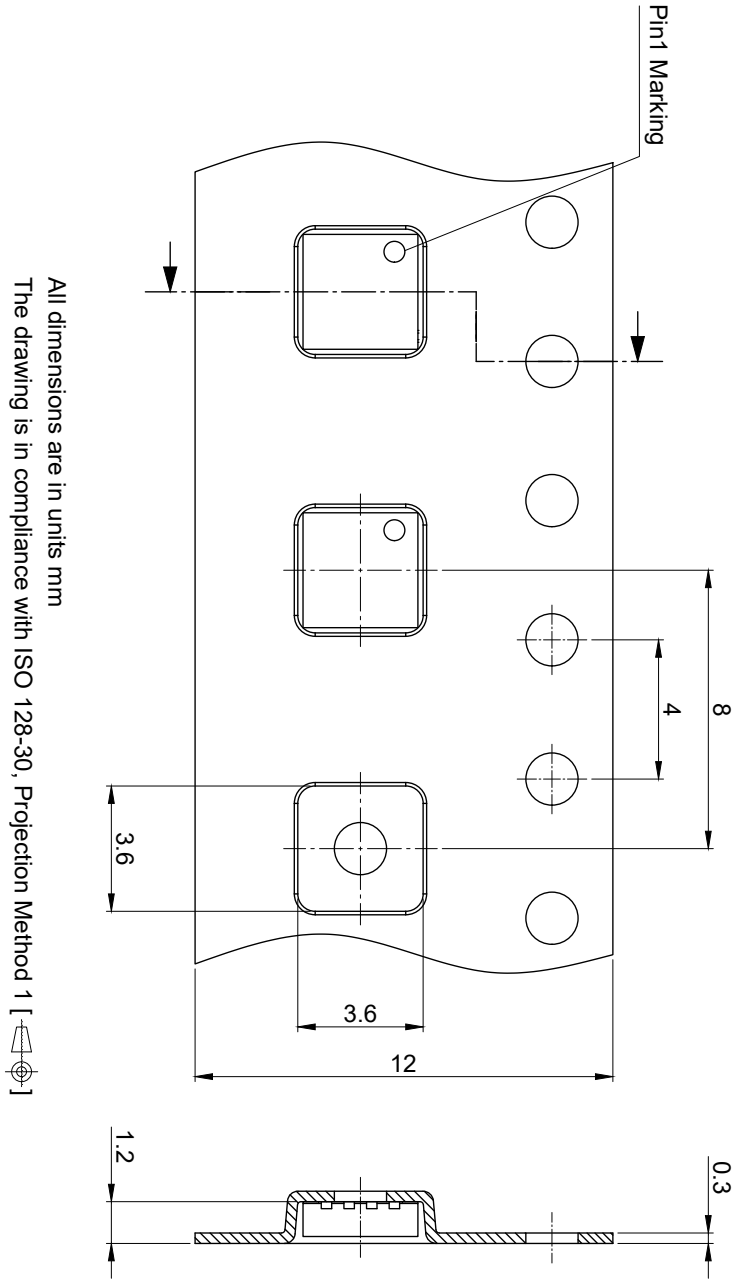


Figure 3 Packaging variant PG-TTFN-9, dimensions in mm

Revision history

IQE065N10NM5CG

Revision 2025-06-02, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2021-04-26	Release of final version
2.1	2021-12-01	Update "Marking" and Gate resistance
2.2	2025-06-02	Update gate resistance

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