

MOSFET
OptiMOS™ 6 Power-Transistor, 80 V

Features

- Optimized for high performance SMPS
- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

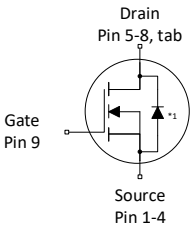
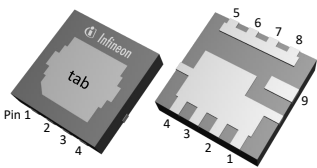
Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max} V_{GS}=10\text{ V}$	3.15	mΩ
$R_{DS(on),max} V_{GS}=4.5\text{ V}$	4.0	mΩ
I_D	127	A
Q_{oss}	57	nC
$Q_G(0V...4.5V)$	33	nC
$Q_{rr}(100A/\mu s)$	20	nC

Part number	Package	Marking	Related links
IQE031N08LM6CGSC	PG-WHTFN-9	N	-

PG-WHTFN-9 (3x3)



*1: Internal body diode

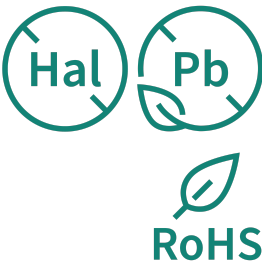




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	127	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				90		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				80		$V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$
				18		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=60\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	508	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	203	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	125	W	$T_C=25\text{ °C}$
				2.5		$T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.2	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.7	1.4		
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	60		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	$V_{DS}=V_{GS}$, $I_D=50.8\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.80	3.15	m Ω	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
			3.36	4.0		$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$
Gate resistance	R_G	0.3	0.55	0.8	Ω	-
Transconductance ⁶⁾	g_{fs}	55	110	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=20\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	3500	4600	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		660	860		
Reverse transfer capacitance ⁷⁾	C_{rss}		35	61		
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		17			
Turn-off delay time	$t_{d(off)}$		21			
Fall time	t_f		9.3			

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	9.1	-	nC	$V_{DD}=40\text{ V}$, $I_D=10\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		5.9	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}		7.9	12	nC	
Switching charge	Q_{sw}		11	-	nC	
Gate charge total ⁹⁾	Q_g		26	33	nC	
Gate plateau voltage	$V_{plateau}$		2.6	-	V	
Gate charge total ⁹⁾	Q_g	-	54	68	nC	$V_{DD}=40\text{ V}$, $I_D=10\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	22	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge ⁹⁾	Q_{oss}	-	57	74	nC	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See "Gate charge waveforms" for parameter definition

⁹⁾ Defined by design. Not subject to production test.

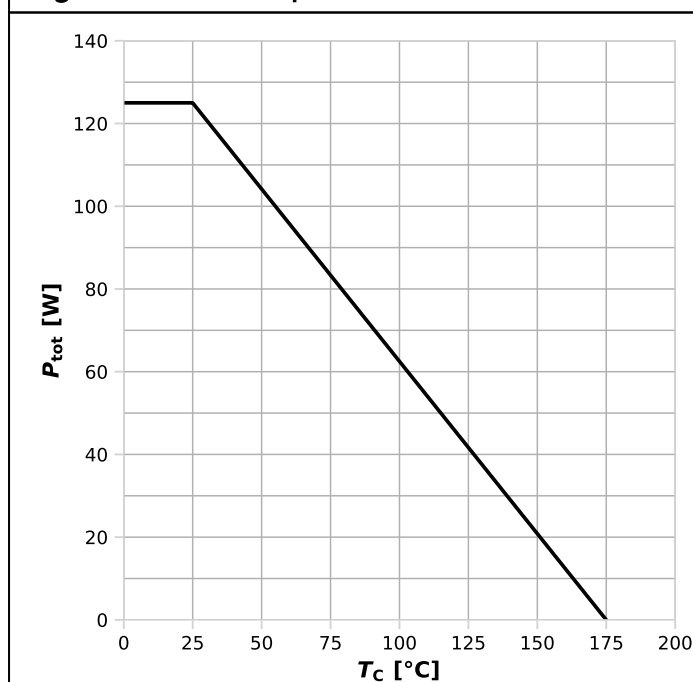
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	116	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			508		
Diode forward voltage	V_{SD}	-	0.79	1.0	V	$V_{GS}=0\text{ V}$, $I_F=20\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁰⁾	t_{rr}	-	27	54	ns	$V_R=40\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		20	40	nC	
Reverse recovery time ¹⁰⁾	t_{rr}	-	18	36	ns	$V_R=40\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		115	230	nC	

¹⁰⁾ Defined by design. Not subject to production test.

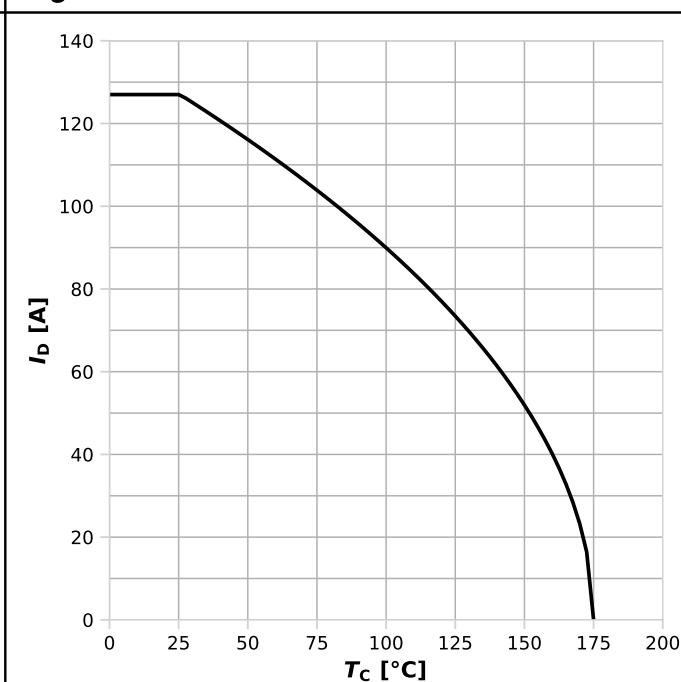
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



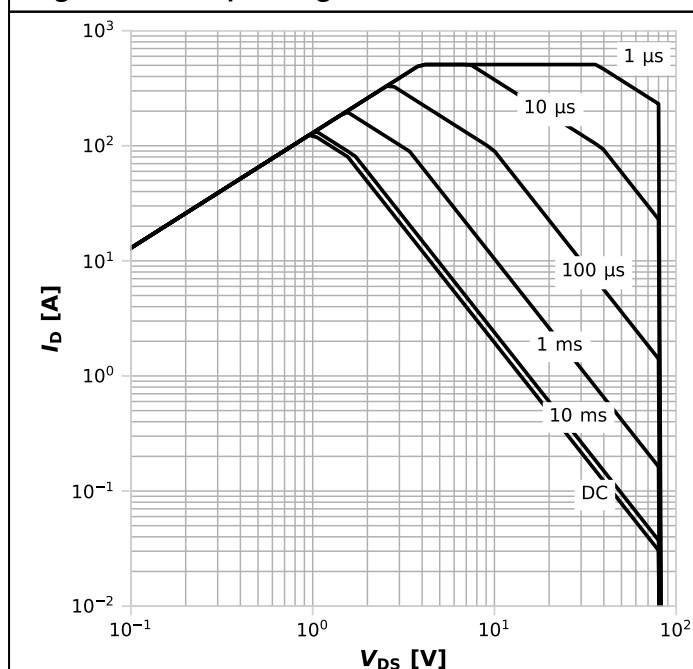
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Drain current



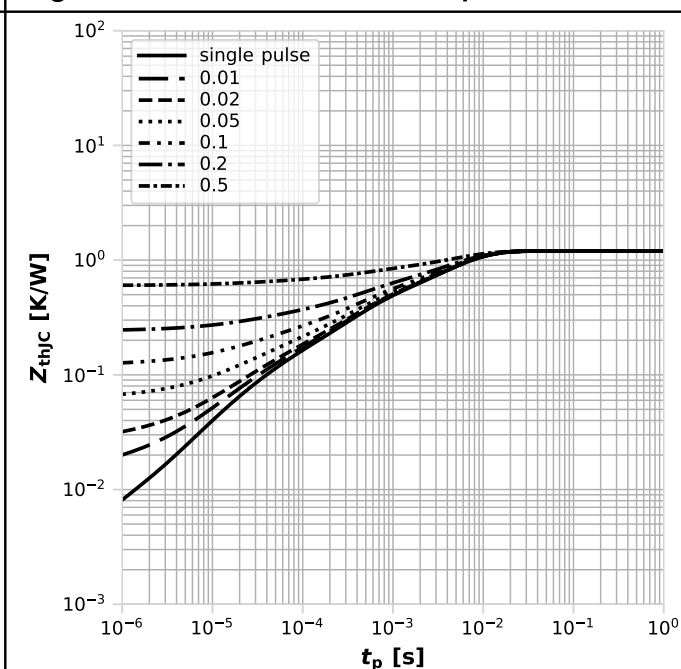
$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$

Diagram 3: Safe operating area



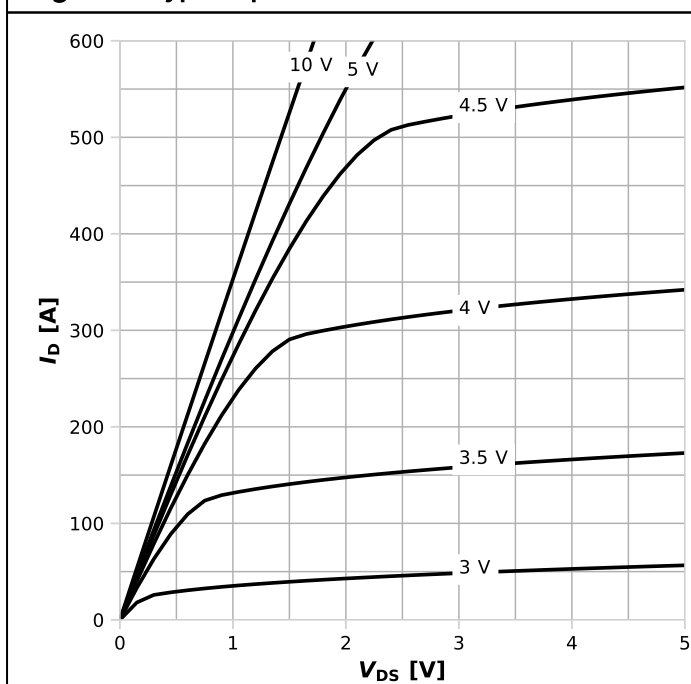
$$I_D = f(V_{DS}); T_c = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



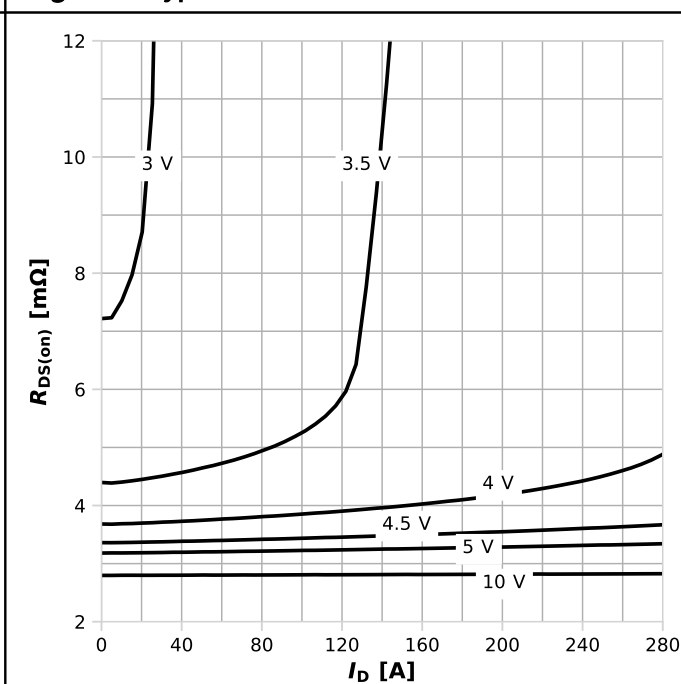
$$Z_{thJC} = f(t_p); \text{parameter: } D = t_p / T$$

Diagram 5: Typ. output characteristics



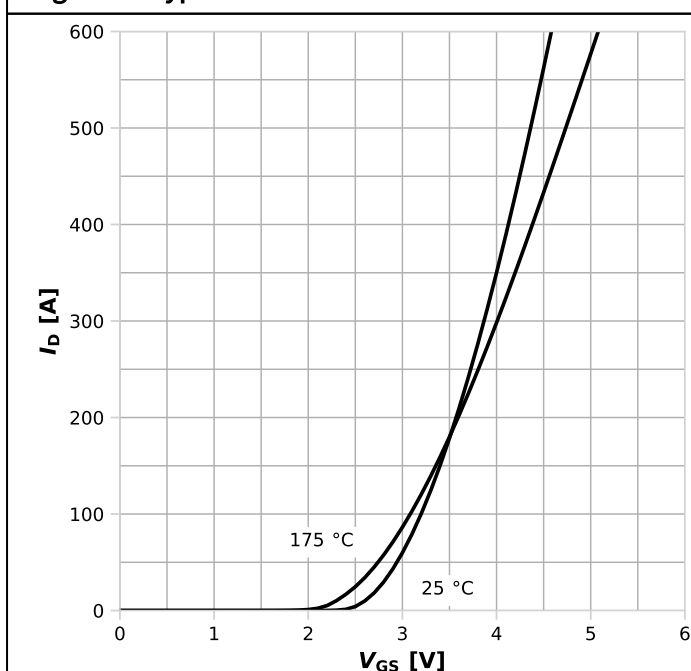
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



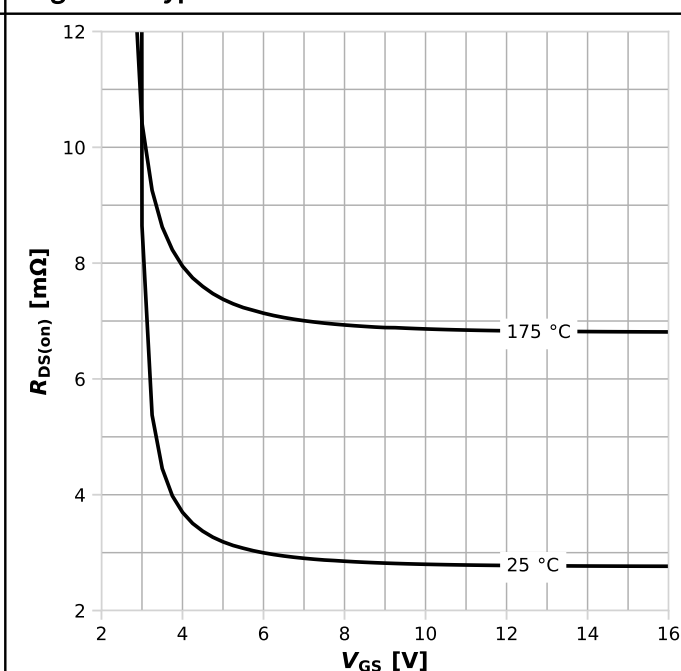
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



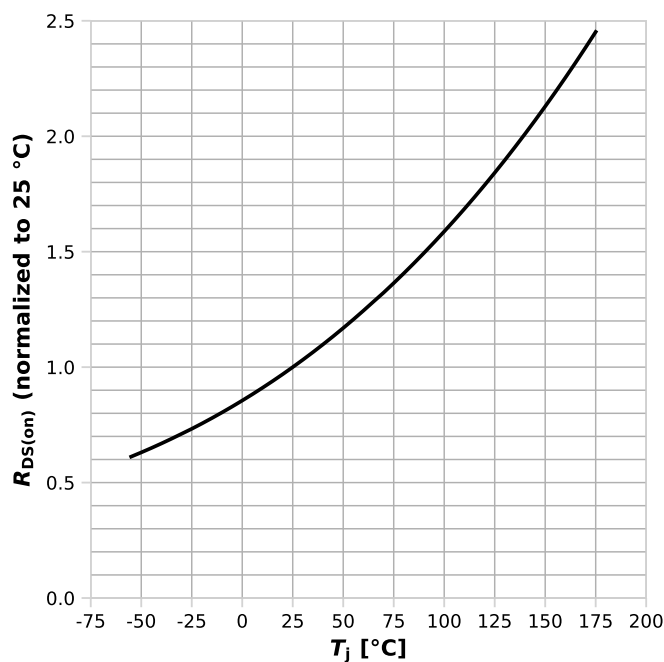
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



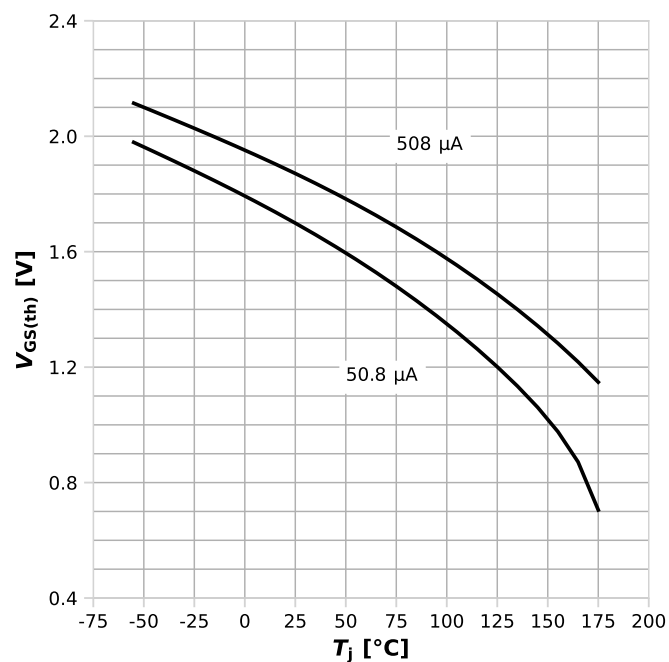
$R_{DS(on)} = f(V_{GS})$, $I_D = 20\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



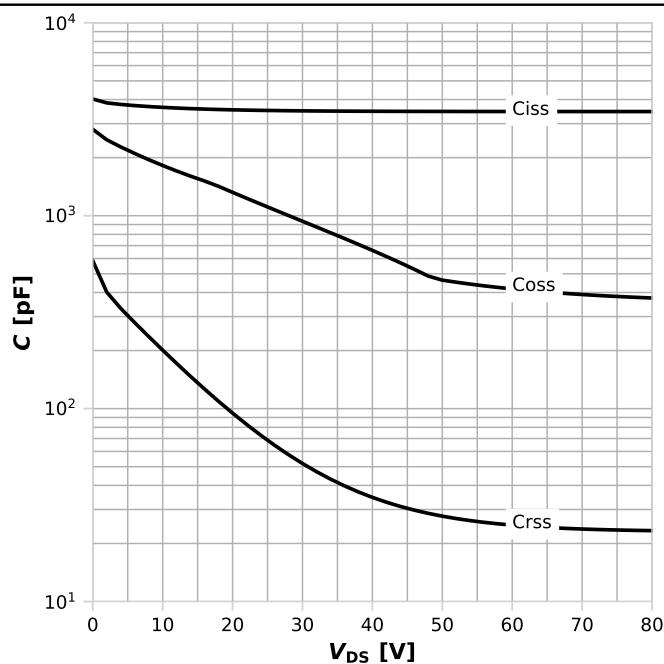
$$R_{DS(on)} = f(T_j), I_D = 20 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



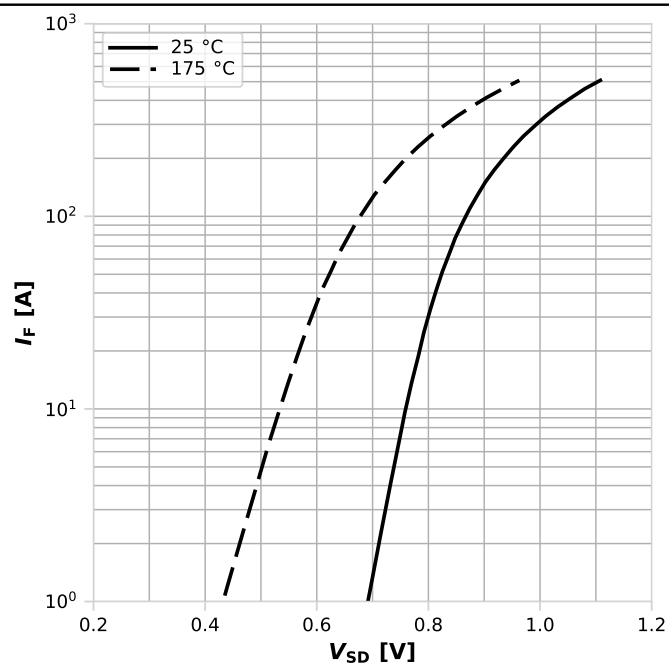
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{parameter: } I_D$$

Diagram 11: Typ. capacitances



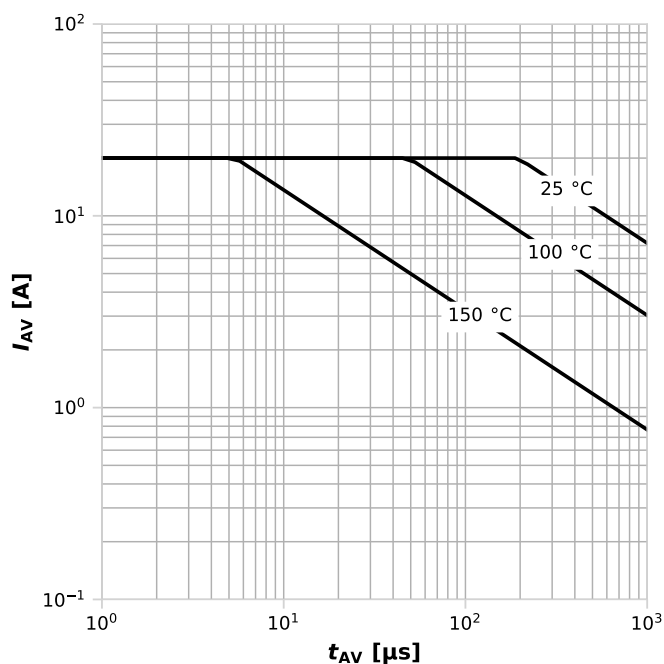
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



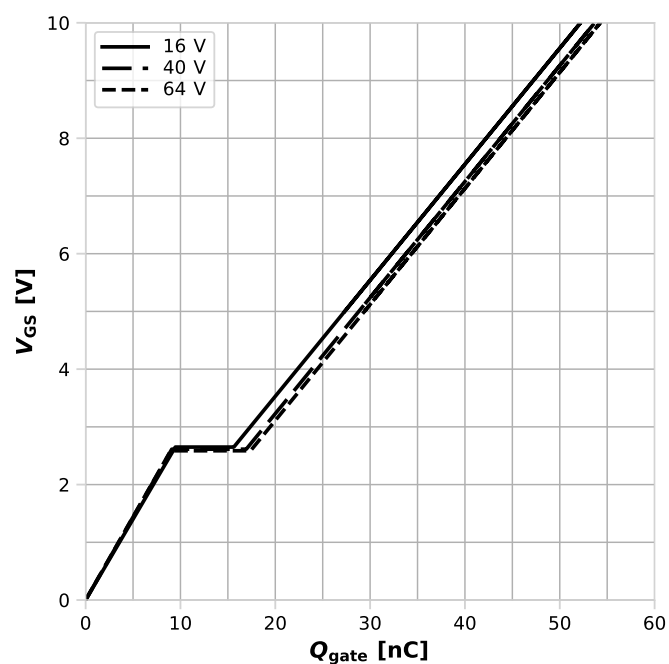
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Diagram 13: Avalanche characteristics



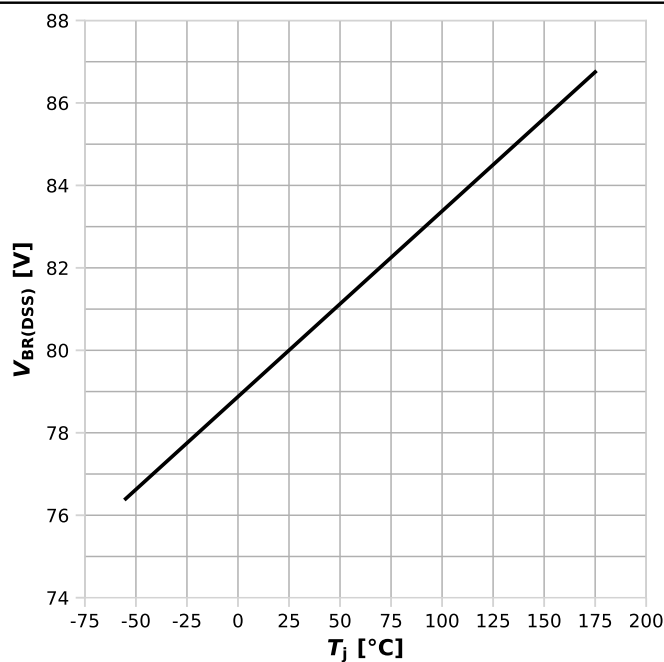
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



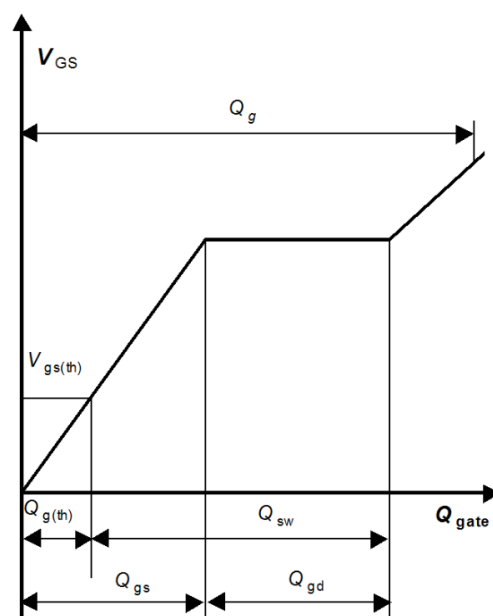
$V_{GS}=f(Q_{gate})$, $I_D=10\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



-

5 Package outlines

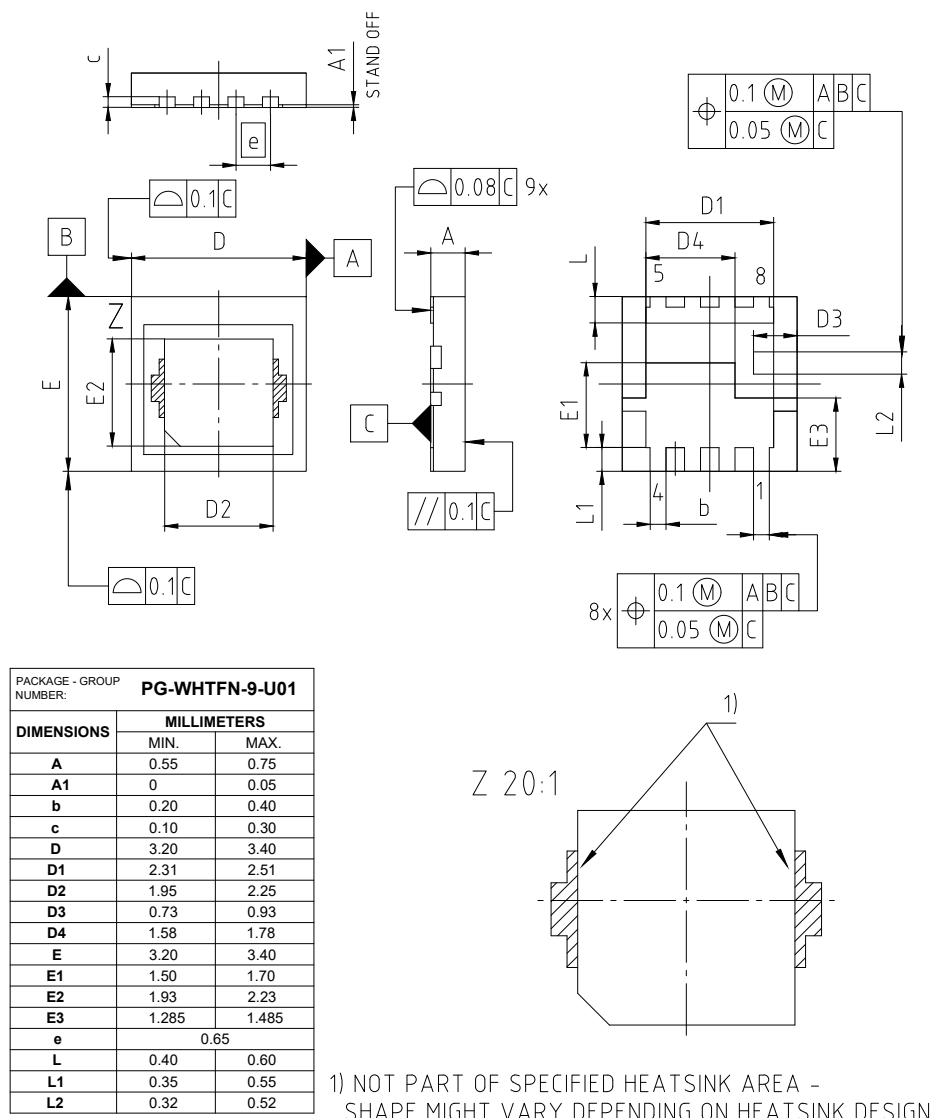


Figure 1 Outline PG-WHTFN-9, dimensions in mm

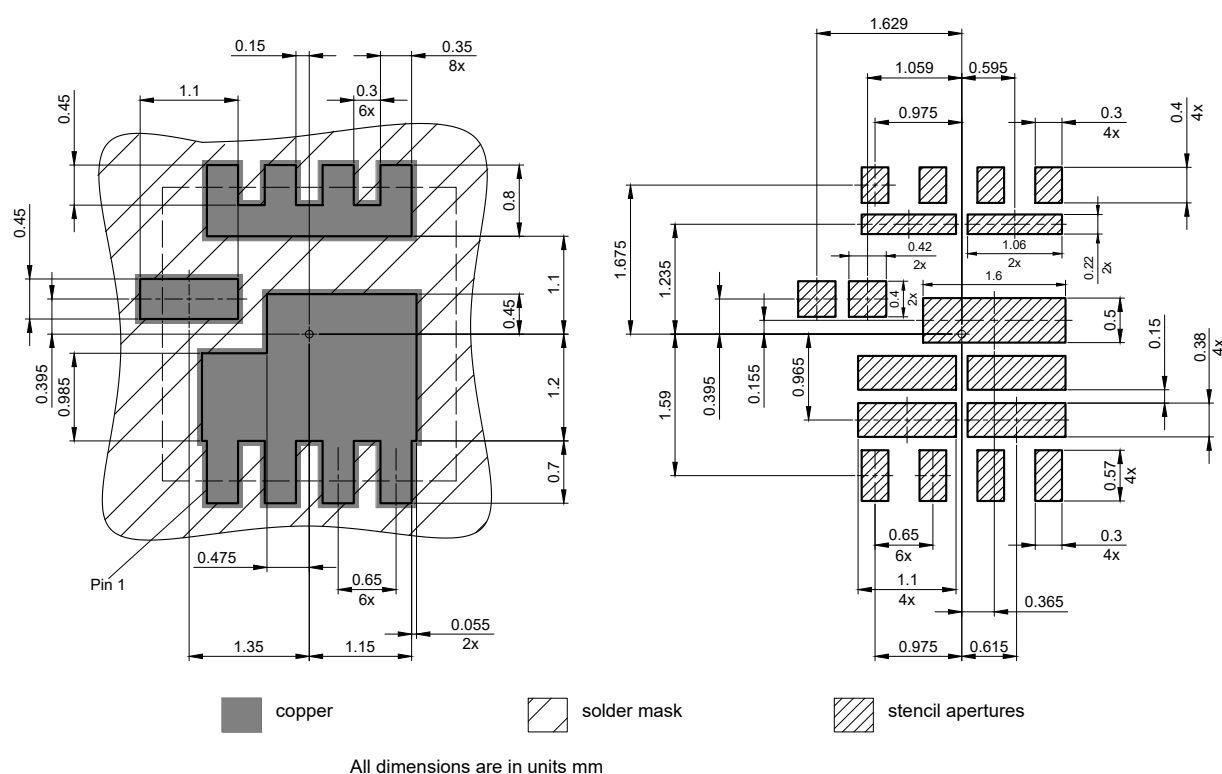


Figure 2 Footprint drawing PG-WHTFN-9, dimensions in mm

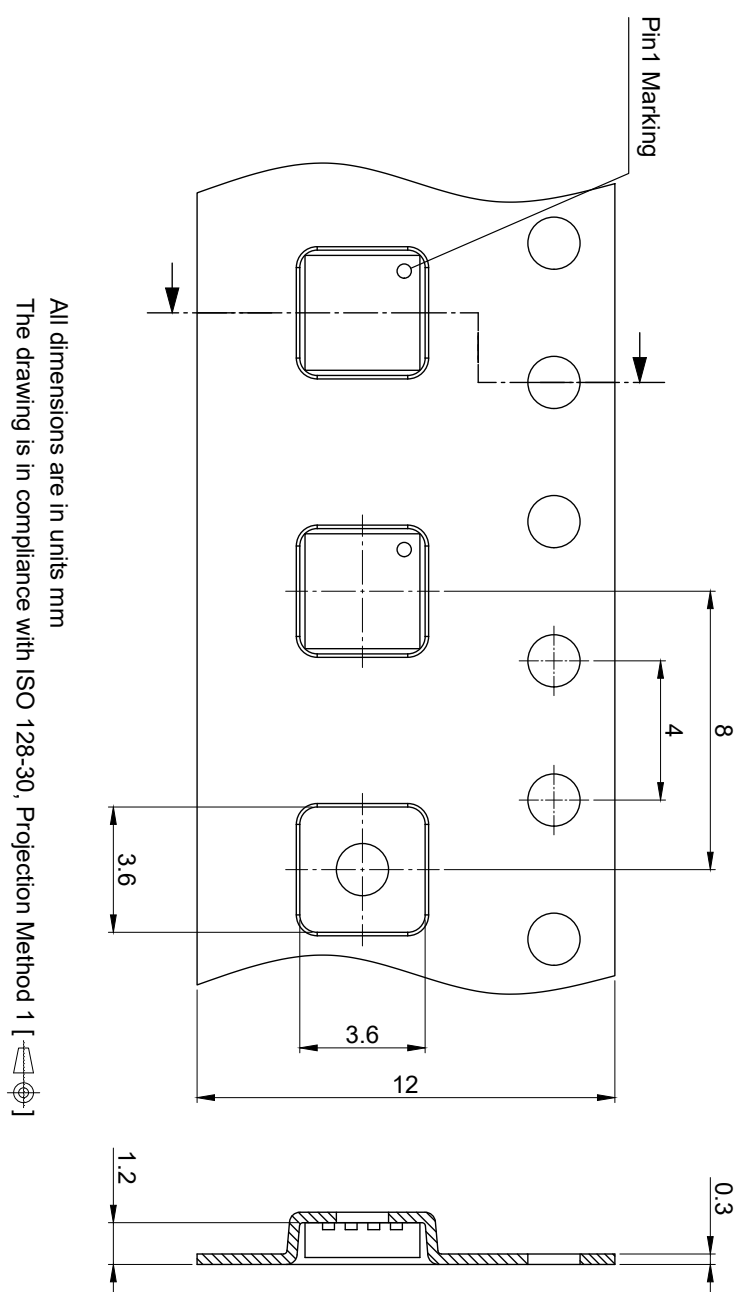


Figure 3 Packaging variant PG-WHTFN-9, dimensions in mm

Revision history

IQE031N08LM6CGSC

Revision 2025-05-21, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-05-21	Release of final version

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Published by

Infineon Technologies AG

81726 München, Germany

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