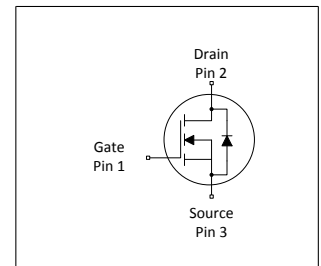


MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.



Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)} \cdot Q_g$ and $R_{DS(on)} \cdot E_{oss}$
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product Validation: Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	145	mΩ
$Q_{g,typ}$	31	nC
$I_{D,pulse}$	58	A
$E_{oss} @ 400V$	3.6	μJ
Body diode di_F/dt	1300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPW60R145CFD7	PG-TO 247-3	60R145F7	see Appendix A

Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Test Circuits 11

Package Outlines 12

Appendix A 13

Revision History 14

Trademarks 14

Disclaimer 14

1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	16 10.0	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	58	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	68	mJ	$I_D=4.1\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.34	mJ	$I_D=4.1\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	4.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	83	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	16	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	58	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 16\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	diF/dt	-	-	1300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 16\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_θ .

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.51	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	lead
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}$, $I_D=0.34mA$
Zero gate voltage drain current ¹⁾	I_{DSS}	-	-	1	μA	$V_{DS}=600V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=600V$, $V_{GS}=0V$, $T_j=125^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.127 0.289	0.145 -	Ω	$V_{GS}=10V$, $I_D=6.8A$, $T_j=25^\circ C$ $V_{GS}=10V$, $I_D=6.8A$, $T_j=150^\circ C$
Gate resistance	R_G	-	10	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1330	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	24	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ²⁾	$C_{o(er)}$	-	44	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ³⁾	$C_{o(tr)}$	-	453	-	pF	$I_D=constant$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	27	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.3A$, $R_G=5.3\Omega$; see table 9
Rise time	t_r	-	18	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.3A$, $R_G=5.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	71	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.3A$, $R_G=5.3\Omega$; see table 9
Fall time	t_f	-	7.2	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.3A$, $R_G=5.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	$V_{DD}=400V$, $I_D=7.3A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	10	-	nC	$V_{DD}=400V$, $I_D=7.3A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	31	-	nC	$V_{DD}=400V$, $I_D=7.3A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V$, $I_D=7.3A$, $V_{GS}=0$ to $10V$

¹⁾ Maximum specification is defined by calculated six sigma upper confidence bound

²⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V$, $I_F=6.8A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	102	153	ns	$V_R=400V$, $I_F=7.3A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.45	0.9	μC	$V_R=400V$, $I_F=7.3A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	8	-	A	$V_R=400V$, $I_F=7.3A$, $di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

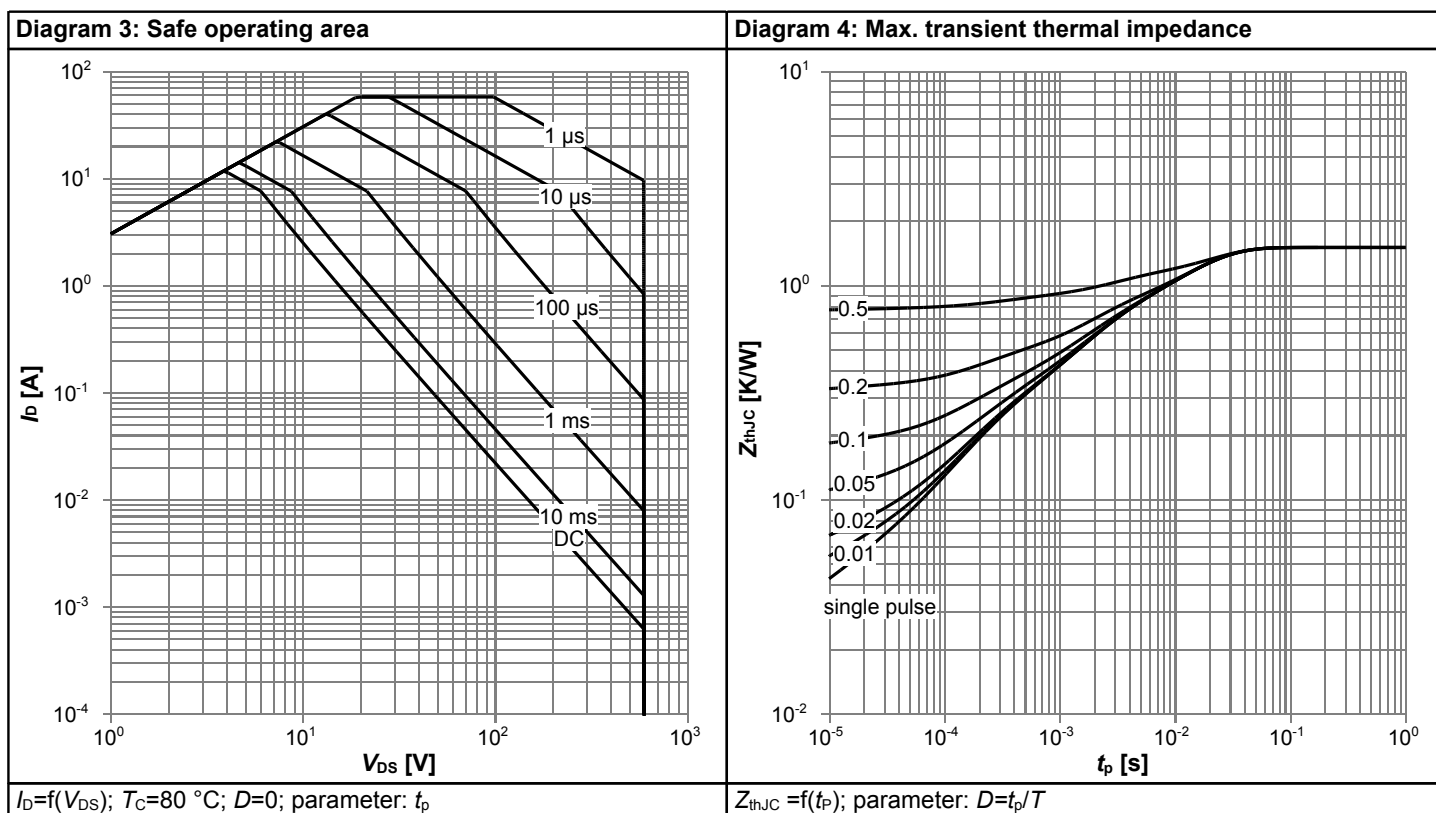
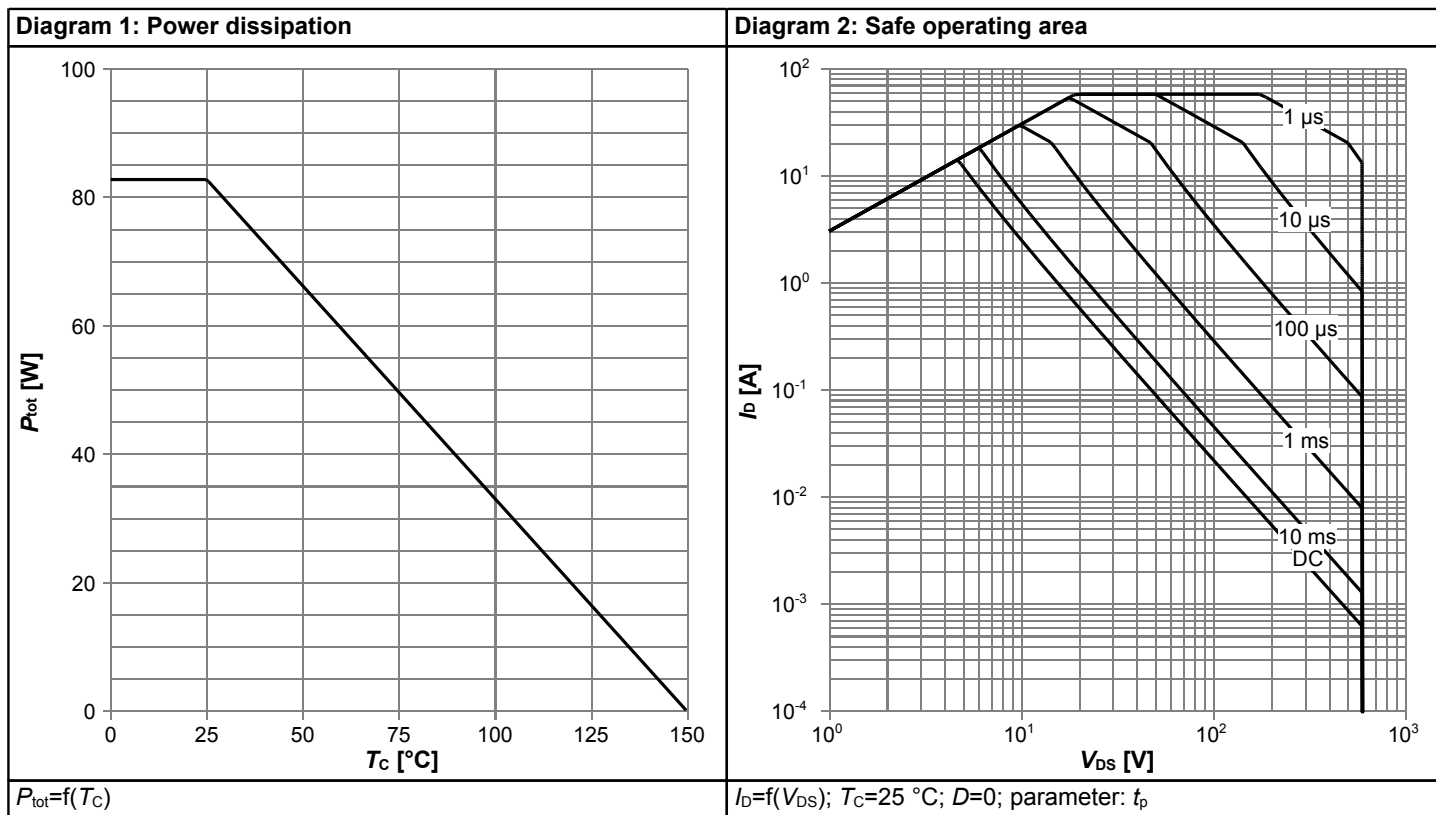
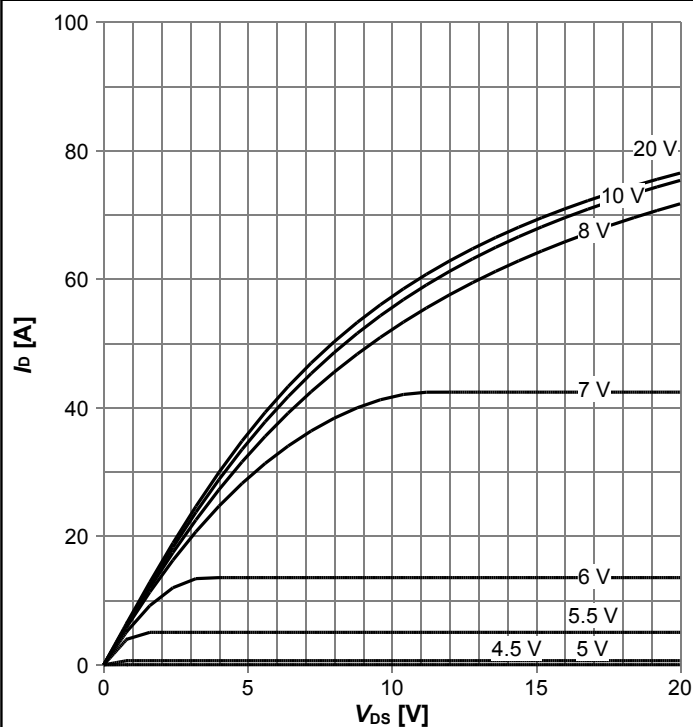
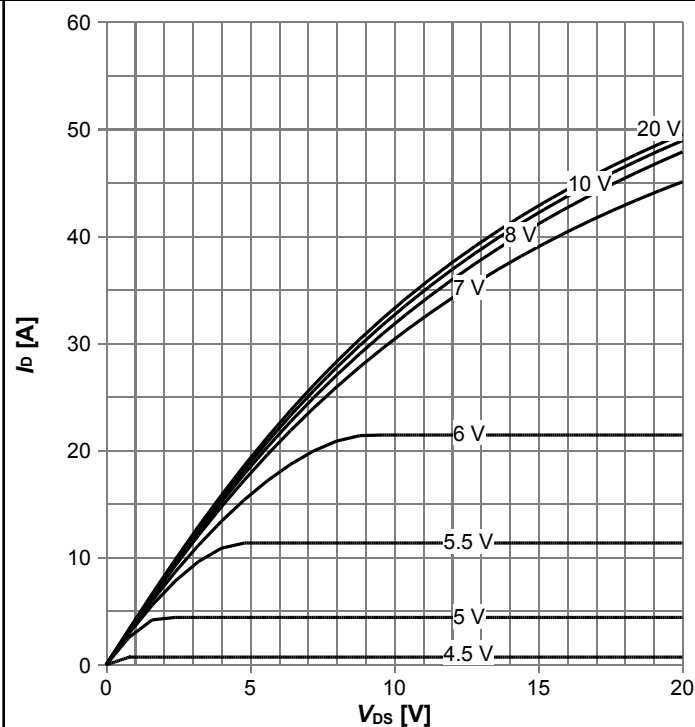


Diagram 5: Typ. output characteristics



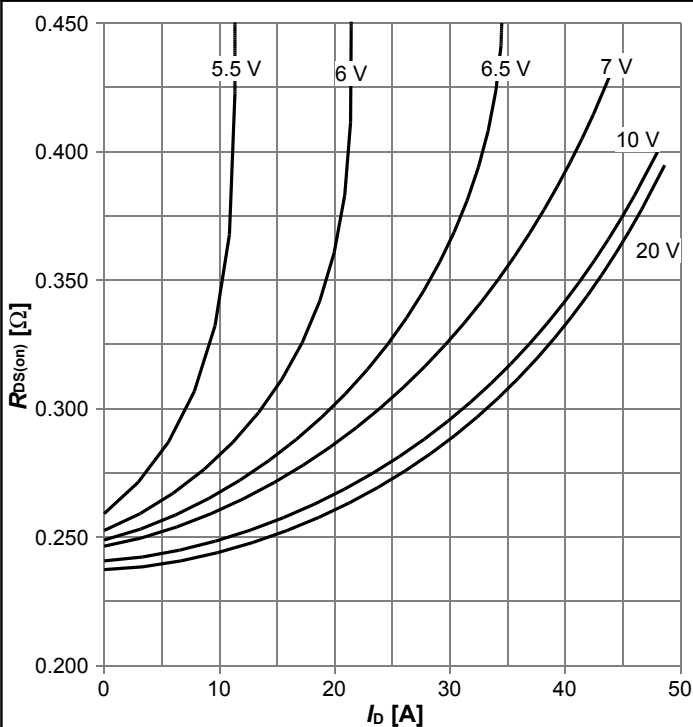
$I_D = f(V_{DS})$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



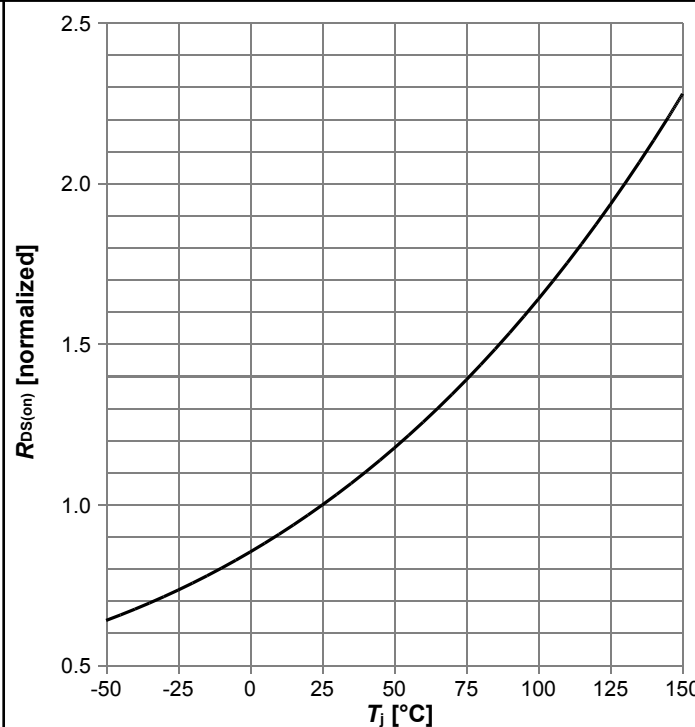
$I_D = f(V_{DS})$; $T_J = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



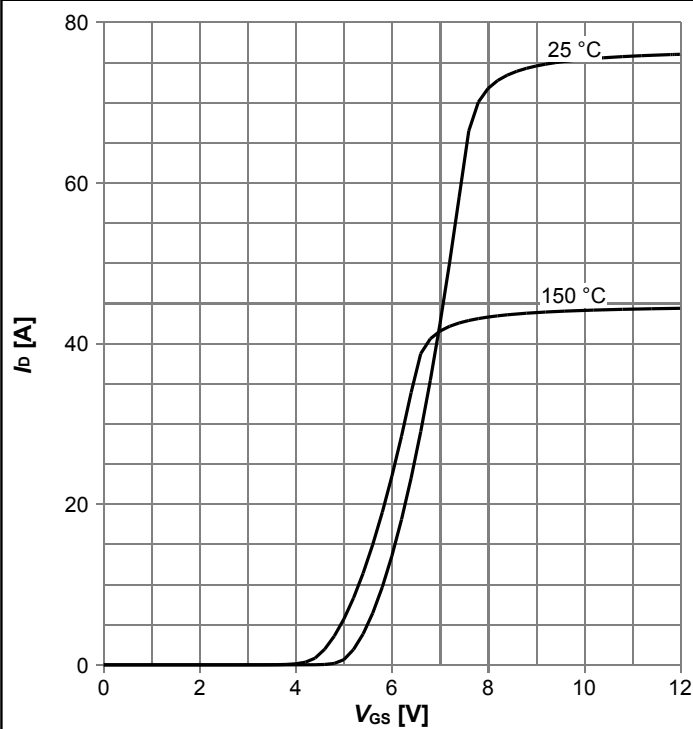
$R_{DS(on)} = f(I_D)$; $T_J = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



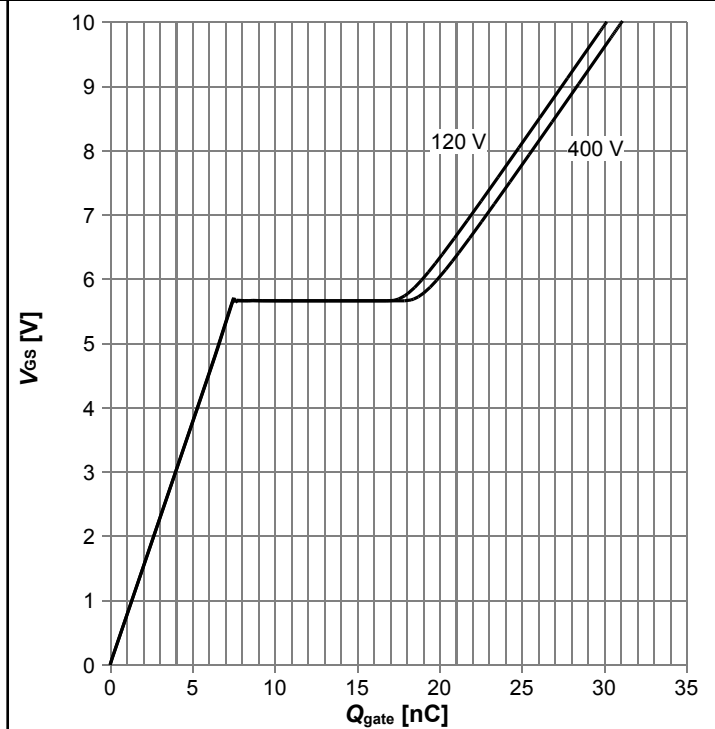
$R_{DS(on)} = f(T_J)$; $I_D = 6.8\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



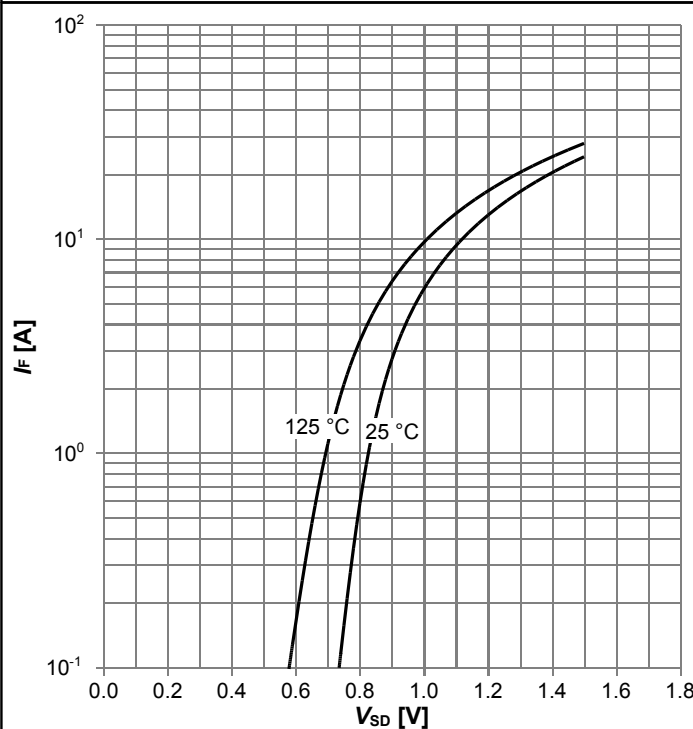
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



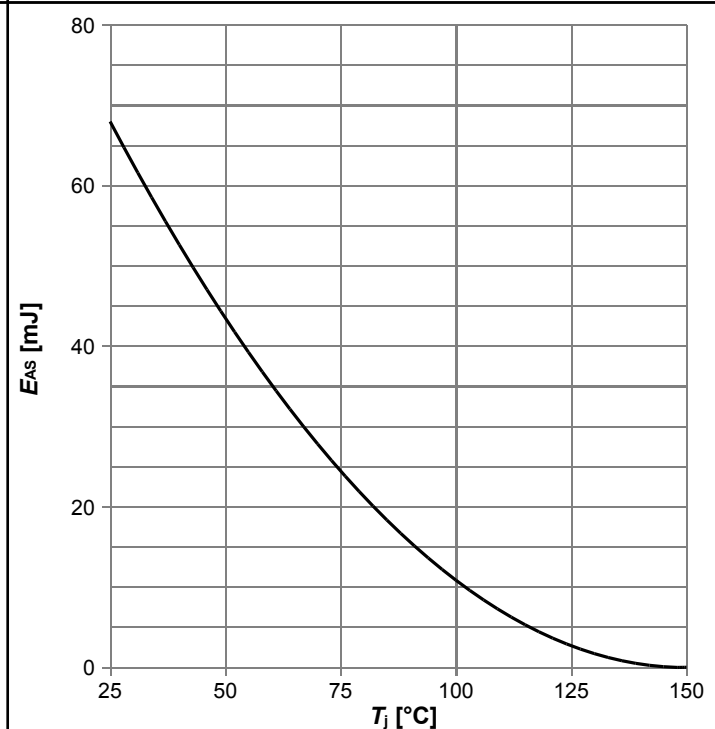
$V_{GS} = f(Q_{gate})$; $I_D = 7.3$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



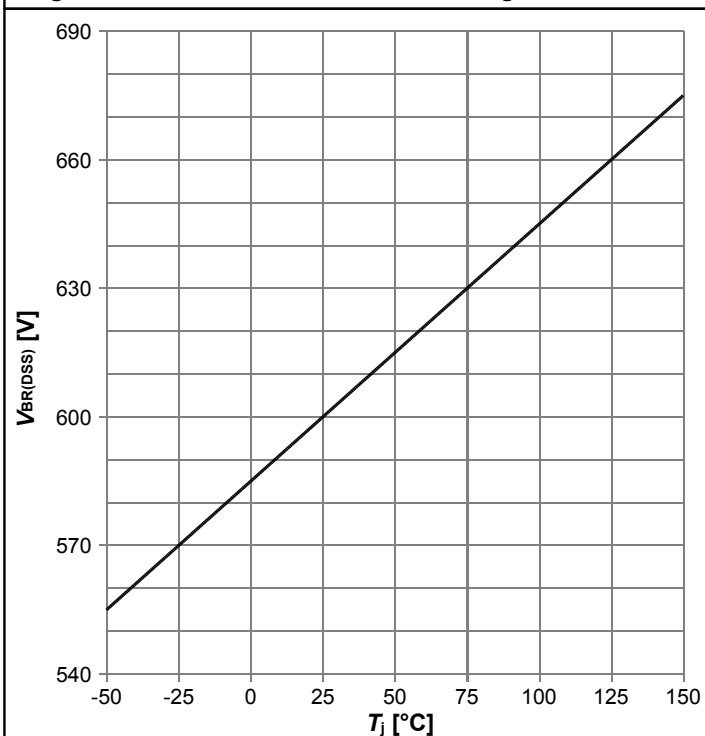
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



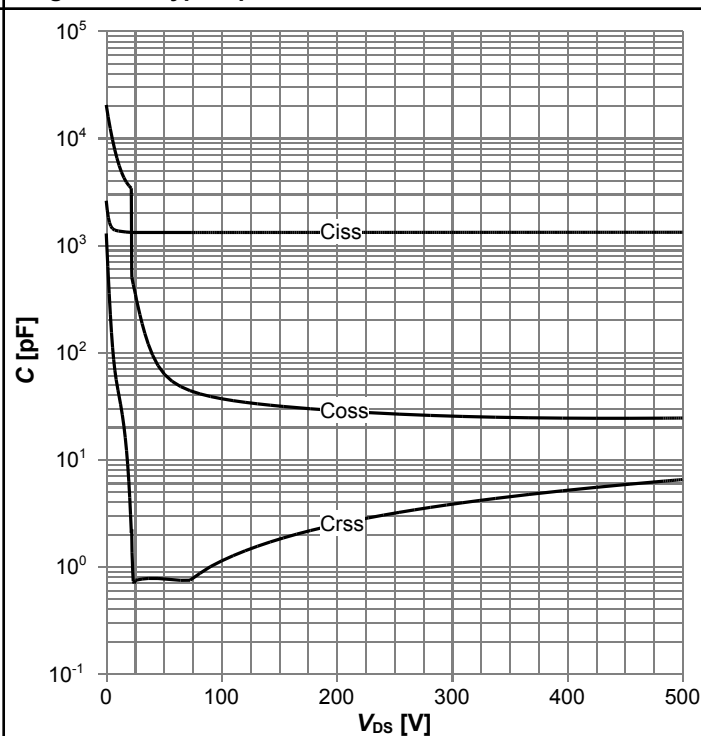
$E_{AS} = f(T_j)$; $I_D = 4.0$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



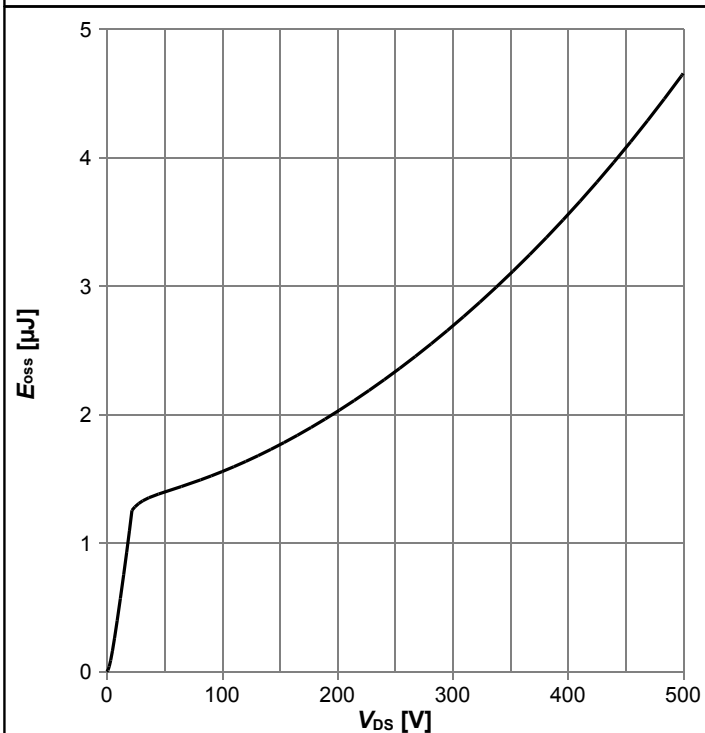
$$V_{BR(DSS)} = f(T_J); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $V_{DS(peak)}$ V_{DS} $90\% V_{DS}$ $10\% V_{DS}$ dV/dt I_F dI_F/dt t_{tr} $10\% I_{Fm}$ I_{Fm} dI_{Fm}/dt Q_{rr}
---	--

Table 9 Switching times

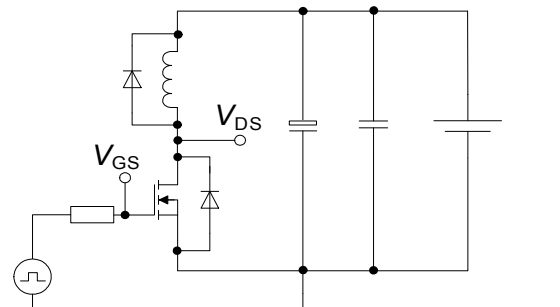
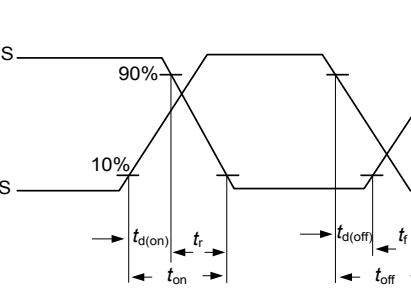
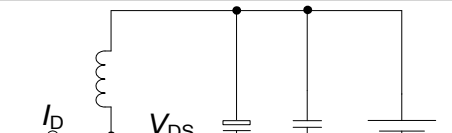
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a MOSFET switching an inductive load. A pulse source drives the gate of the MOSFET through a resistor, with the gate voltage labeled V_{GS}. The MOSFET's drain is connected to an inductor, which is in series with a load. A freewheeling diode is connected in parallel with the inductor. The drain-source voltage is labeled V_{DS}. A capacitor is connected in parallel with the inductor and diode. The MOSFET is shown with its internal structure, including the gate, drain, and source regions, and the body diode.	 The timing diagram shows the switching waveforms for V_{DS} and V_{GS}. The V_{GS} waveform is a square wave that transitions between a low level and a high level. The V_{DS} waveform shows the voltage across the MOSFET during these transitions. Key time intervals are defined: $t_{d(on)}$: Delay time from the start of the V_{GS} rise to the 10% point of the V_{DS} fall. t_r: Rise time of V_{GS} from 10% to 90%. t_{on}: Total on-time from the start of V_{GS} rise to the start of V_{GS} fall. $t_{d(off)}$: Delay time from the start of the V_{GS} fall to the 90% point of the V_{DS} rise. t_f: Fall time of V_{GS} from 90% to 10%. t_{off}: Total off-time from the start of V_{GS} fall to the start of V_{GS} rise.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines

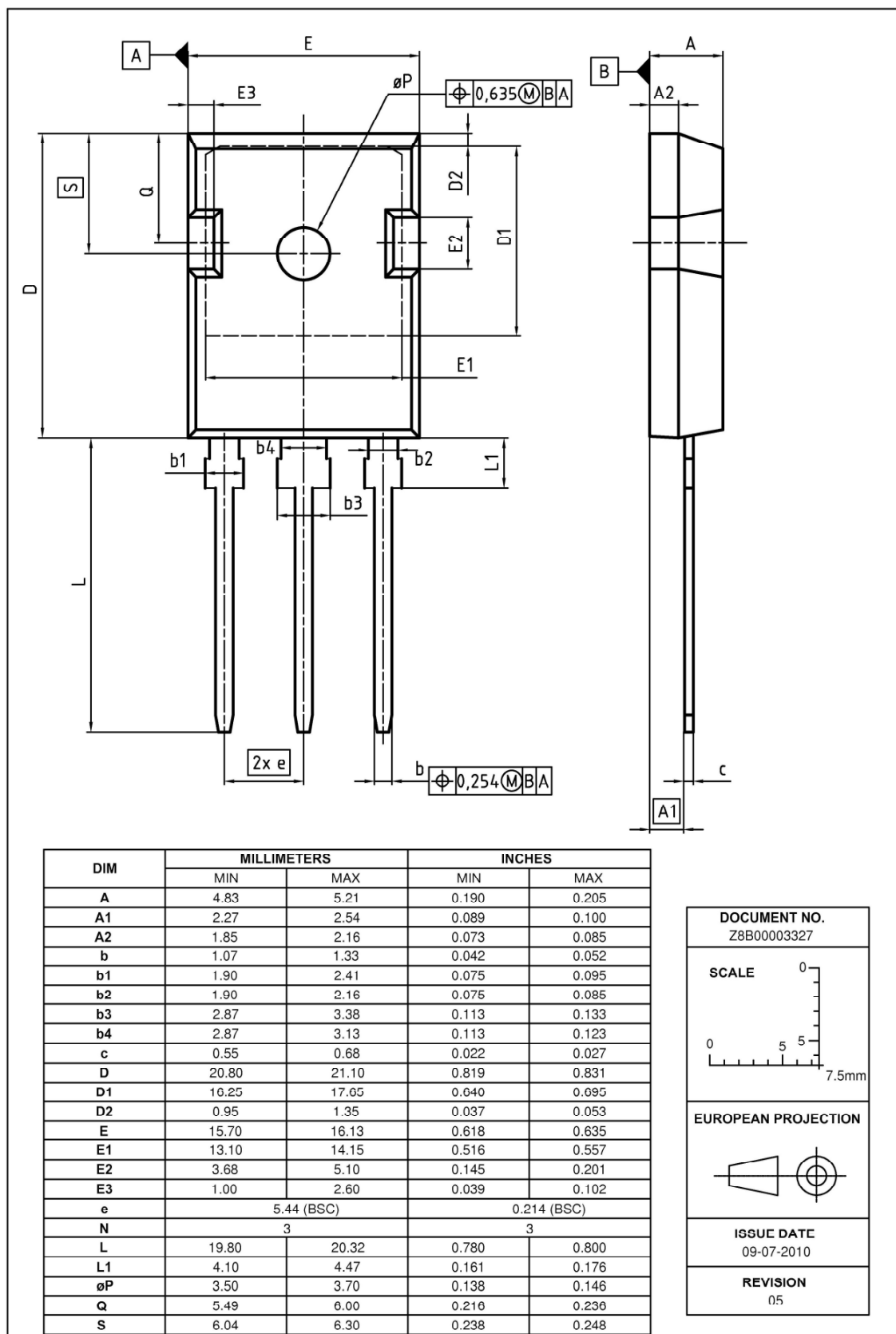


Figure 1 Outline PG-TO 247-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 application note:** www.infineon.com
- **IFX CoolMOS CFD7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPW60R145CFD7

Revision: 2018-11-05, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-04-20	Release of final version
2.1	2018-11-05	Table 7: Reduced trr,max value; Change of qualification grade nomenclature

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

Published by

Infineon Technologies AG

81726 München, Germany

© 2018 Infineon Technologies AG

All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.