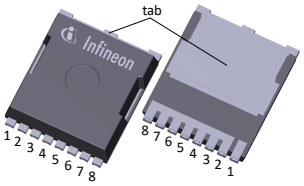
MOSFET

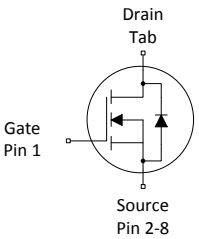
TOLL

OptiMOS™ 6 Power-Transistor, 200 V



Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020
- 100% avalanche tested

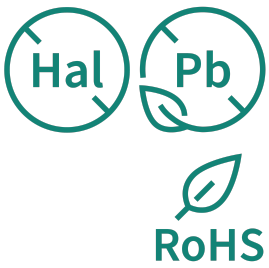


Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	12.9	mΩ
I_D	87	A
Q_{oss}	116	nC
Q_G	37	nC
Q_{rr} (1000A/µs)	271	nC



Part number	Package	Marking	Related links
IPT129N20NM6	PG-HSOF-8	129N20N6	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	87	A	V_{GS}=10 V, T_C=25 °C
				61		V_{GS}=10 V, T_C=100 °C
				64		V_{GS}=15 V, T_C=100 °C
				11		V_{GS}=10 V, T_A=25°C, R_{thJA}=40°C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	348	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	258	mJ	I_D=39 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	234	W	T_C=25 °C
				3.8		T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.32	0.64	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}		-	40		
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}		-	62		

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.7	4.5	V	V_{DS}=V_{GS}, I_D=129 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=160 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=160 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	10.9	12.9	mΩ	V_{GS}=10 V, I_D=65 A
			9.4	12		V_{GS}=15 V, I_D=65 A
Gate resistance	R_G	-	3.8	-	Ω	-
Transconductance [6)]	g_{fs}	18	36	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=65 A

6) Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2900	3800	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance [7)]	C_{oss}		460	600		
Reverse transfer capacitance [7)]	C_{rss}		19	33		
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=32.5 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		13			
Turn-off delay time	$t_{d(off)}$		20			
Fall time	t_f		7			

7) Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	V_{DD}=100 V, I_D=32.5 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		10.7	-	nC	
Gate to drain charge [9]	Q_{gd}		7.5	11.3	nC	
Switching charge	Q_{sw}		16.8	-	nC	
Gate charge total [9]	Q_g		37	56	nC	
Gate plateau voltage	$V_{plateau}$		6.9	-	V	
Output charge [9]	Q_{oss}	-	116	151	nC	V_{DS}=100 V, V_{GS}=0 V

[8] See "Gate charge waveforms" for parameter definition

[9] Defined by design. Not subject to production test.

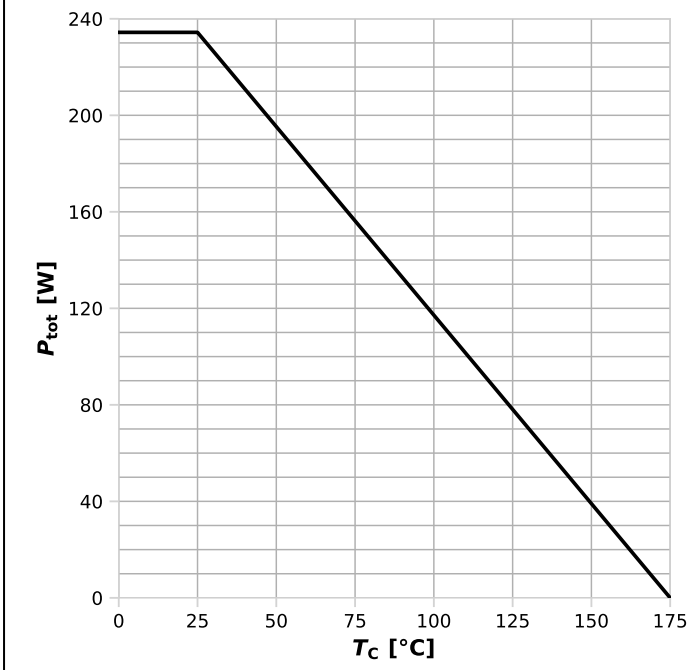
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	87	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			348		
Diode forward voltage	V_{SD}	-	0.90	1.0	V	V_{GS}=0 V, I_F=65 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	46	-	ns	V_R=100 V, I_F=32.5 A, di_F/dt=100 A/µs
Reverse recovery charge [10]	Q_{rr}		43	86	nC	
Reverse recovery time	t_{rr}	-	39	-	ns	V_R=100 V, I_F=32.5 A, di_F/dt=1000 A/µs
Reverse recovery charge [10]	Q_{rr}		271	542	nC	

[10] Defined by design. Not subject to production test.

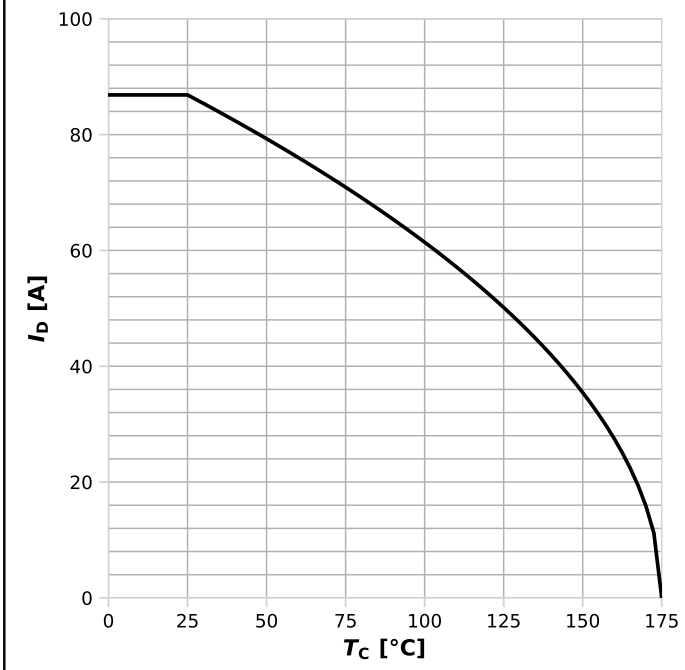
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



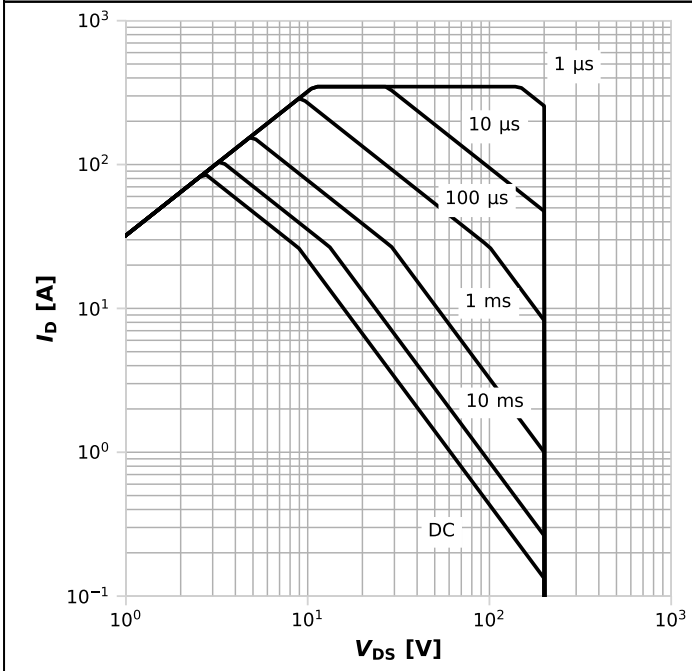
P_{tot}=f(T_C)

Diagram 2: Drain current



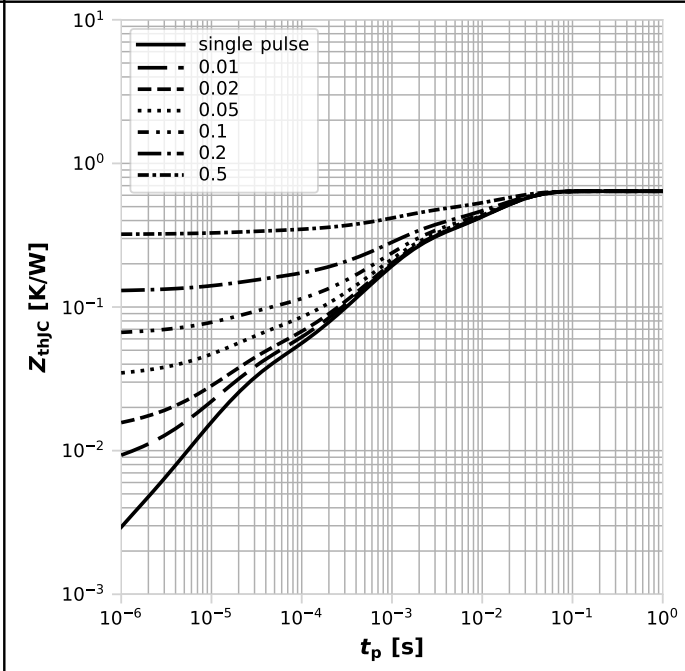
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



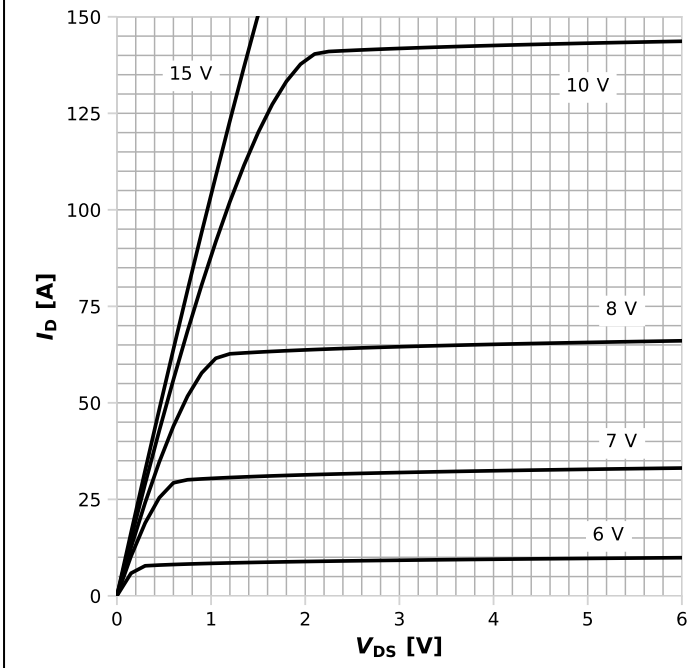
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



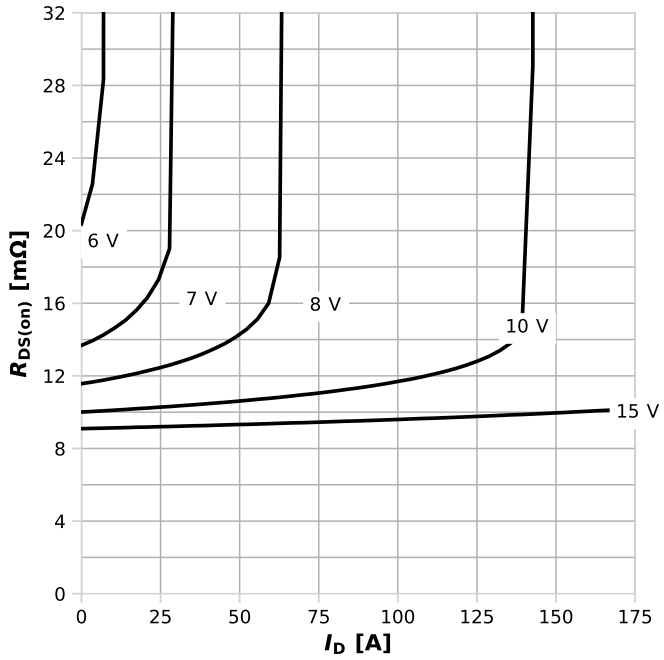
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



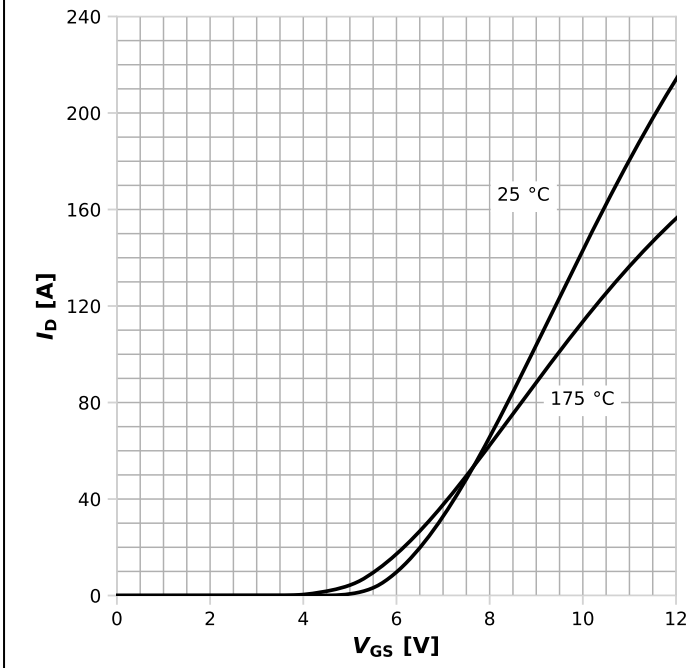
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



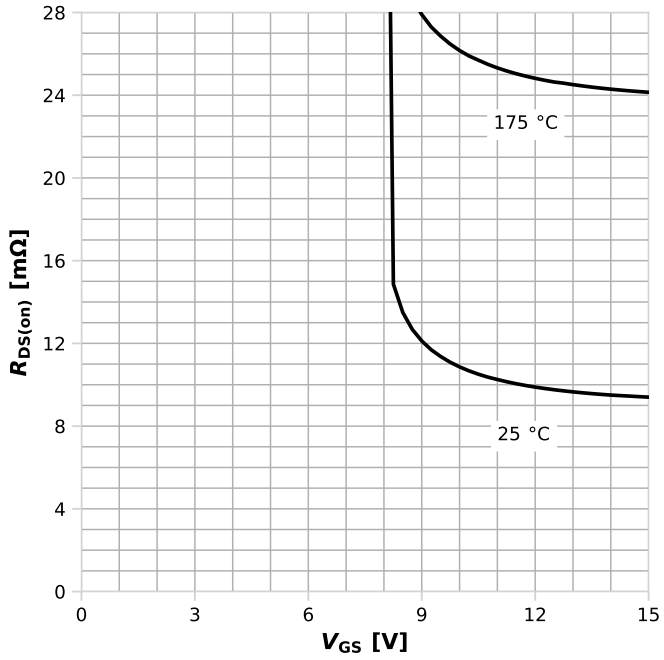
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=65 A; parameter: T_j

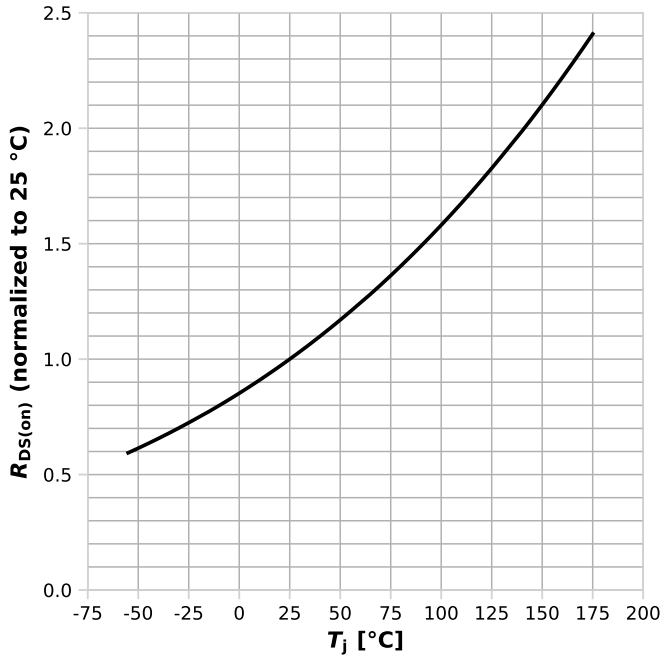
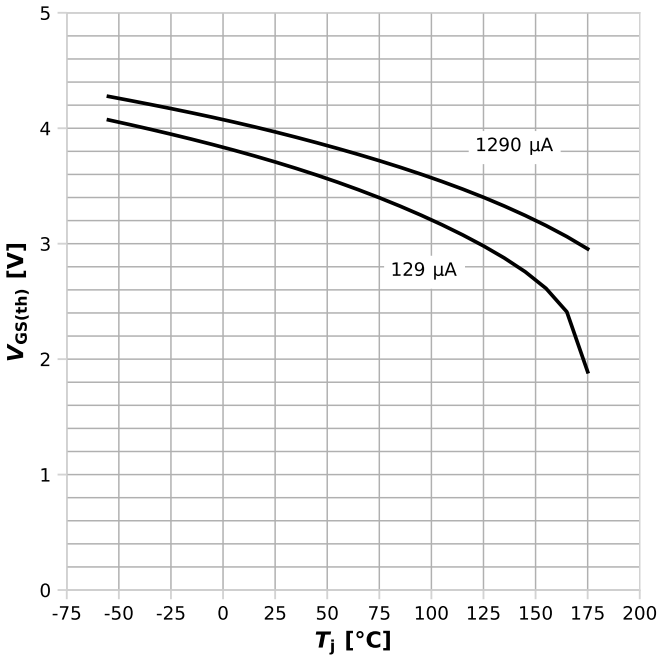
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=65 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

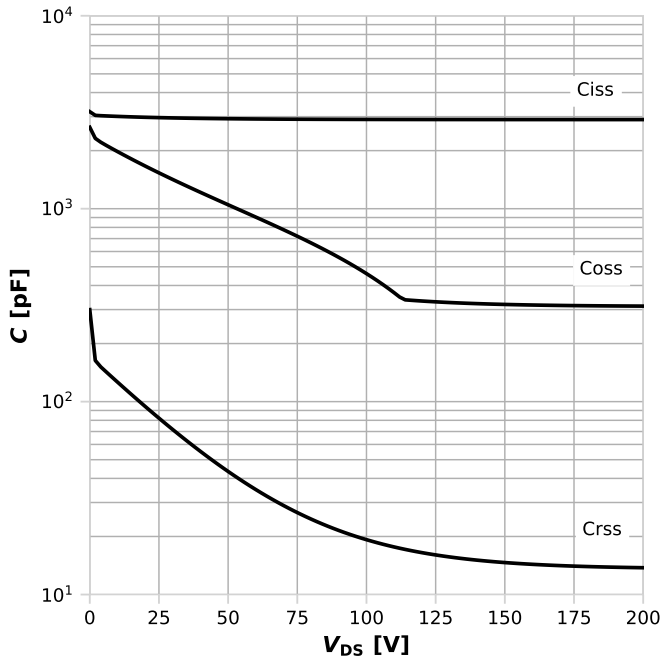
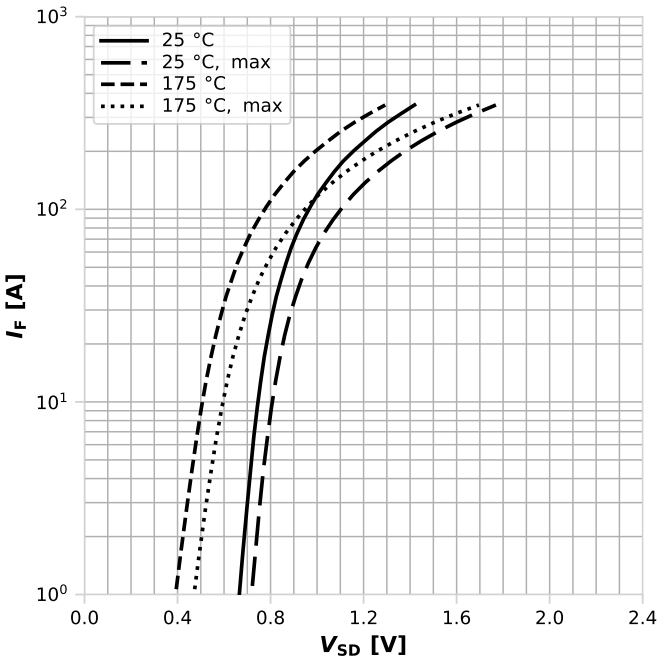
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

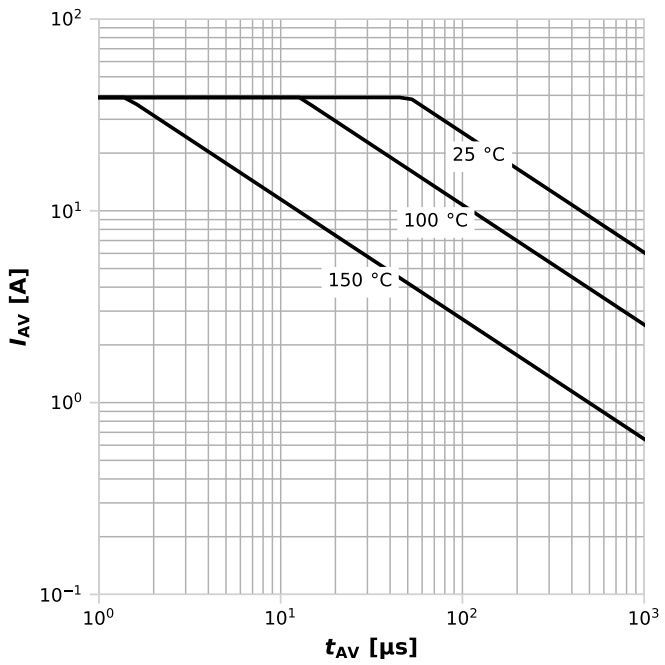
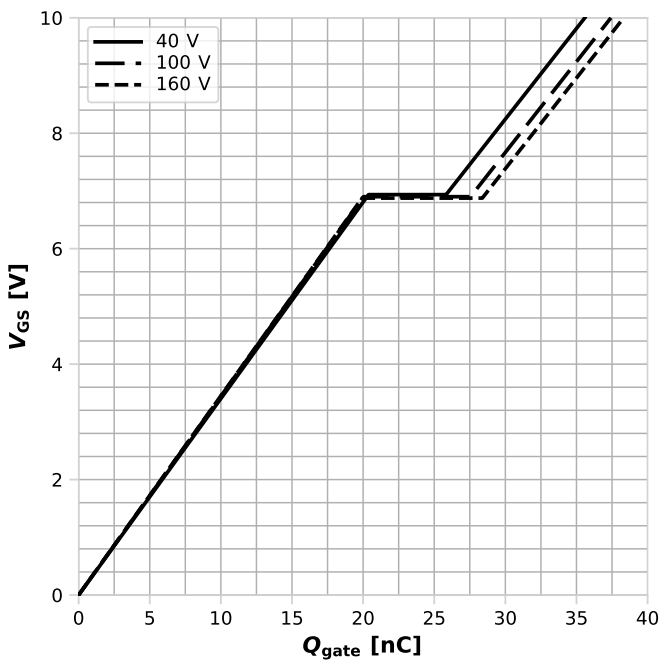
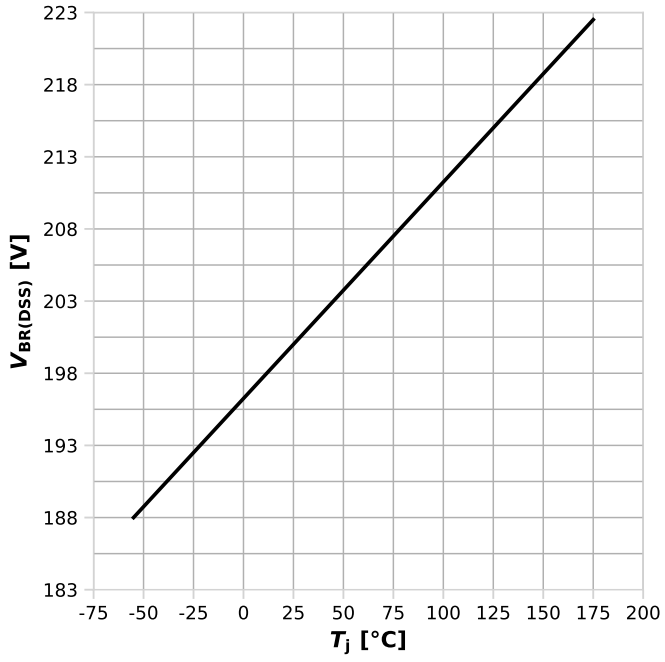
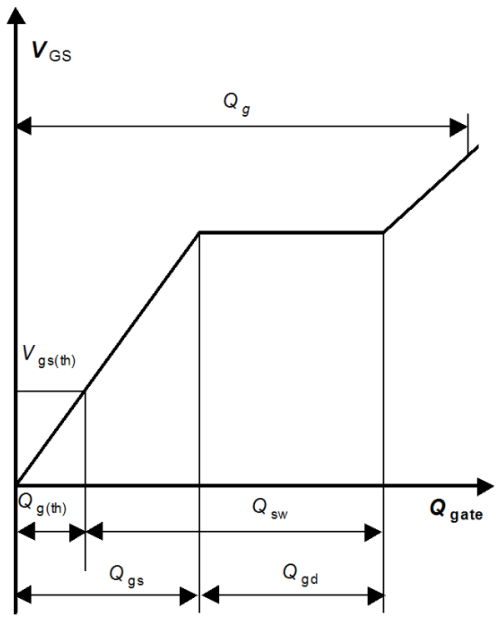
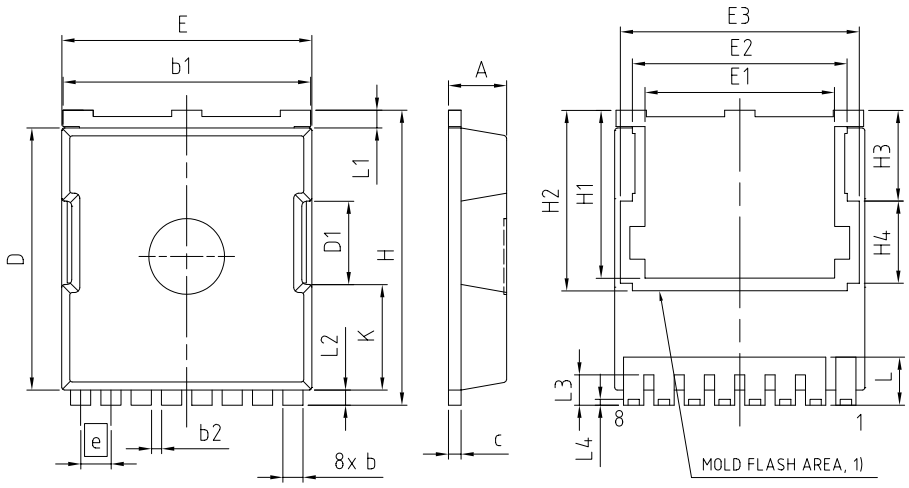
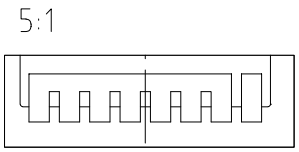
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=32.5 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.30	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	7.50
H3	3.59	
H4	3.26	
N	8	
K	4.03	4.33
L	1.60	2.10
L1	0.50	0.90
L2	0.45	0.75
L3	1.00	1.30
L4	0.13	0.33



OPTIONAL LEAD FORM:
WITHOUT LTI OPTION

1) PATIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

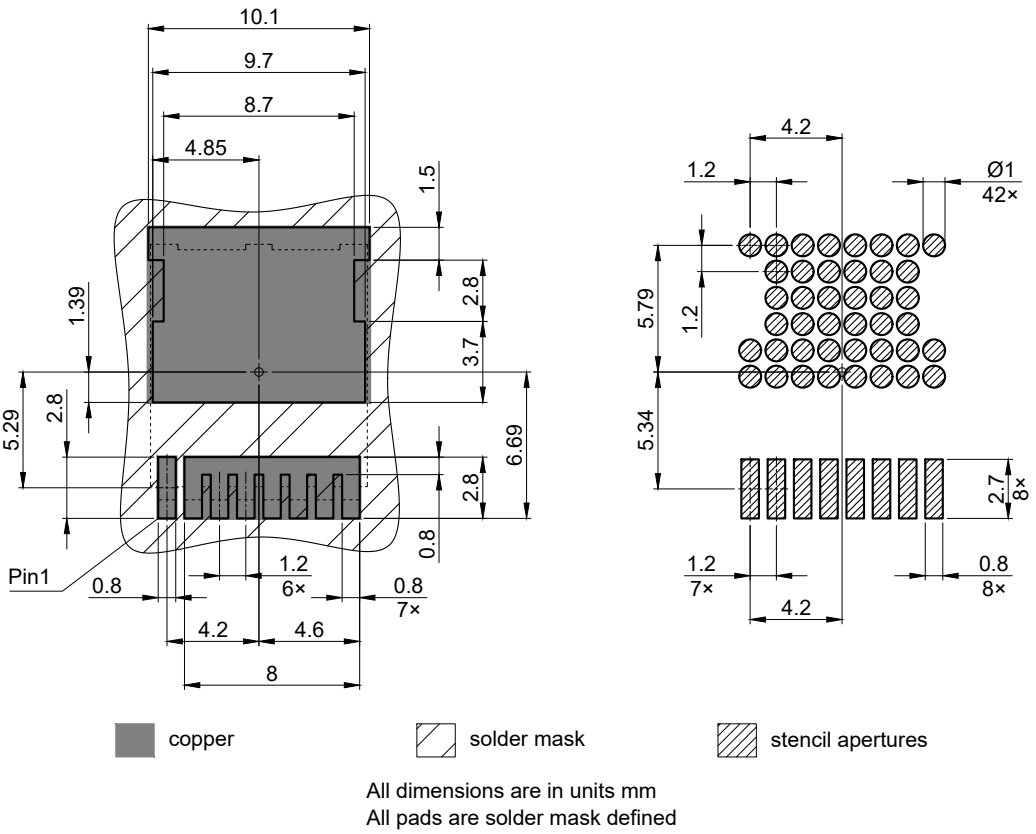


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm

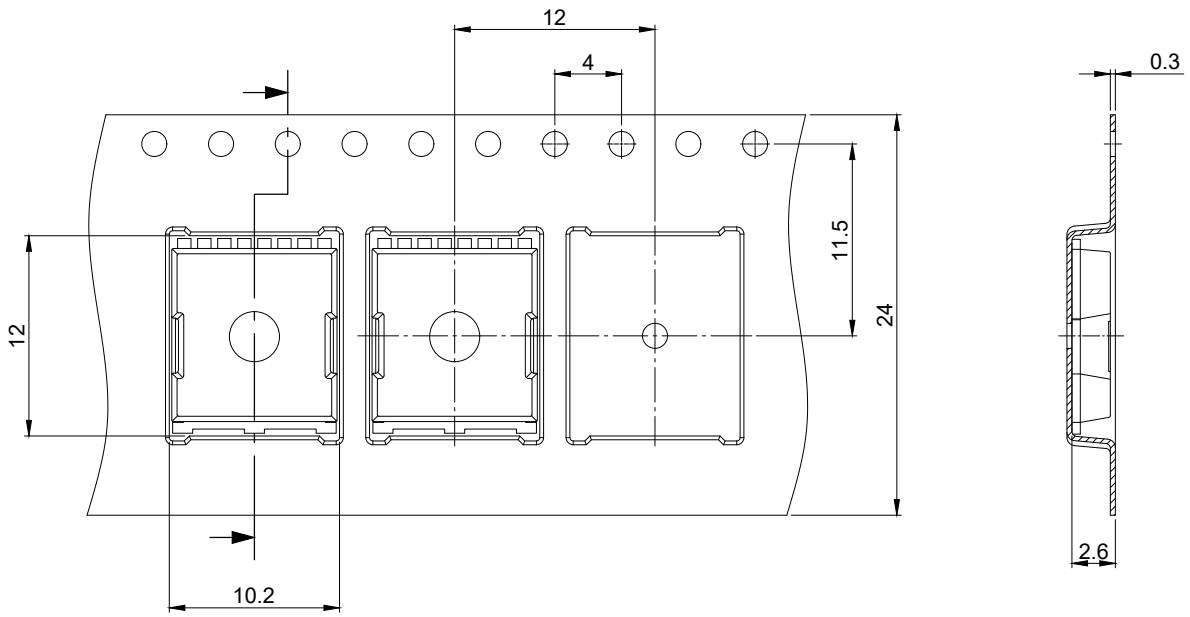


Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

Revision history

IPT129N20NM6

Revision 2025-12-05, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-07	Release of final version
2.1	2025-12-05	Update Rgext condition for timing and Qrr at di/dt=1000A/us

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