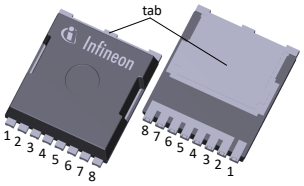
MOSFET

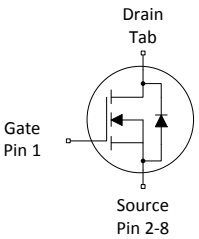
TOLL

OptiMOS™ 5 Power-Transistor, 100 V



Features

- Ideal for high frequency switching and sync. rec.
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

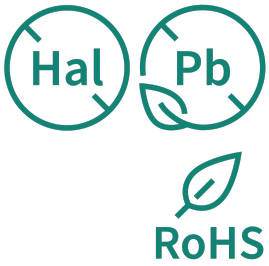


Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	2.0	mΩ
I_D	260	A
Q_{oss}	155	nC
Q_G(0V..10V)	122	nC



Part number	Package	Marking	Related links
IPT020N10N5	PG-HSOF-8	020N10N5	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	260	A	V_{GS}=10 V, T_C=25 °C
				184		V_{GS}=10 V, T_C=100 °C
				31		V_{GS}=10 V, T_A=25 °C, R_{thJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1039	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	406	-	I_D=150 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	-	-
Power dissipation	P_{tot}	-	-	273	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.33	0.55	°C/W	-
Device on PCB, minimal footprint	R_{thJA}		-	62		
Device on PCB, 6 cm^2 cooling area [5]	R_{thJA}		-	40		

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=202 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.6	2.0	mΩ	V_{GS}=10 V, I_D=150 A
			2.0	2.7		V_{GS}=6 V, I_D=75 A
Gate resistance [6]	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	120	240	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	8700	11000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [7]	C_{oss}		1300	1700		
Reverse transfer capacitance [7]	C_{rss}		58	100		
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.8 Ω
Rise time	t_r		13			
Turn-off delay time	$t_{d(off)}$		49			
Fall time	t_f		17			

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	39	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		26	-	nC	
Gate to drain charge [9)]	Q_{gd}		25	37	nC	
Switching charge	Q_{sw}		38	-	nC	
Gate charge total [9)]	Q_g		122	152	nC	
Gate plateau voltage	$V_{plateau}$		4.5	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	106	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [8)]	Q_{oss}	-	155	207	nC	V_{DS}=50 V, V_{GS}=0 V

8) See "Gate charge waveforms" for parameter definition

9) Defined by design. Not subject to production test.

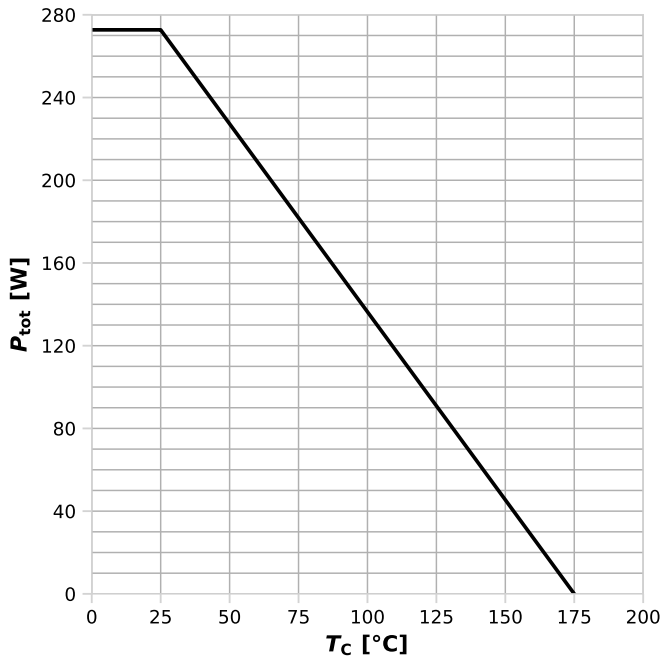
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	198	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			1039		
Diode forward voltage	V_{SD}	-	0.86	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	56	112	ns	V_R=50 V, I_F=100 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}		96	192	nC	

10) Defined by design. Not subject to production test.

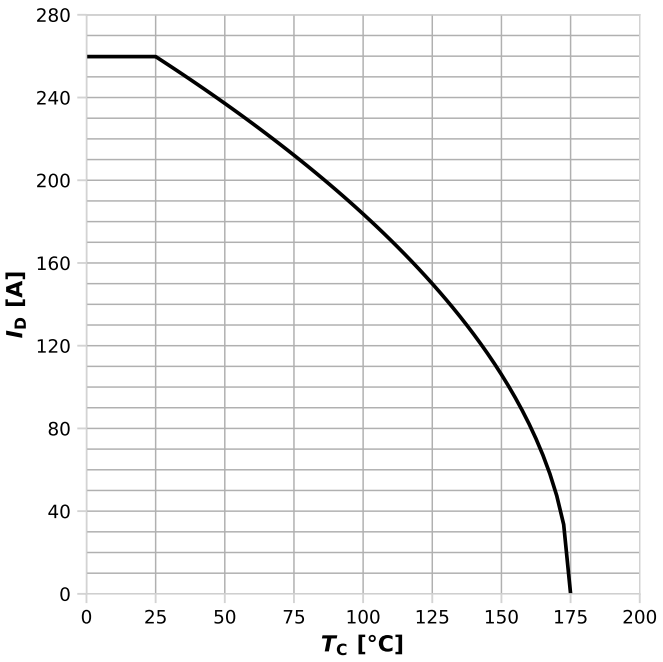
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



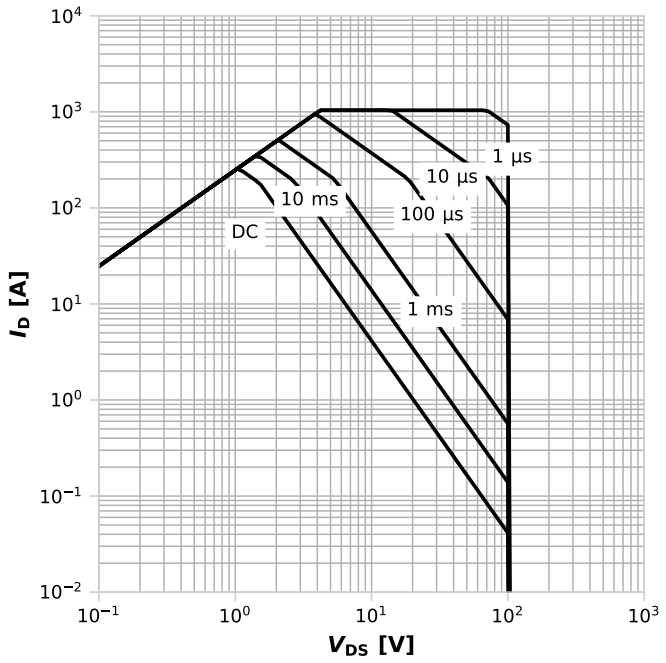
P_{tot}=f(T_C)

Diagram 2: Drain current



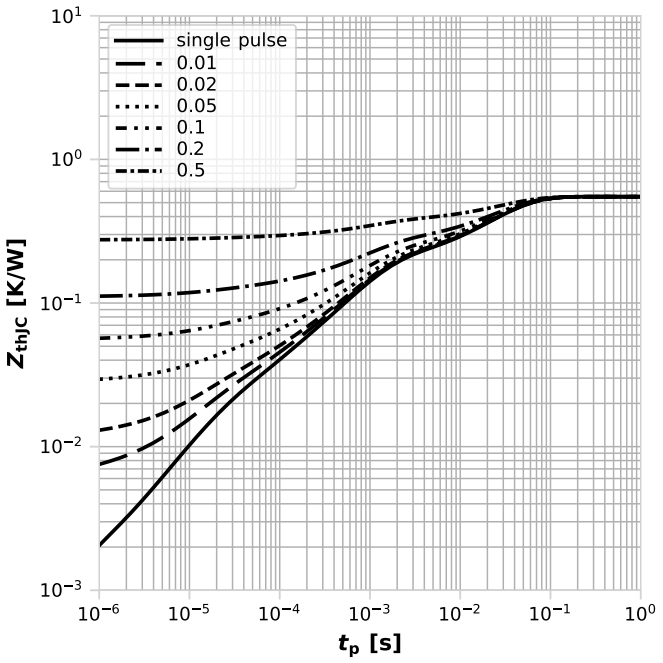
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



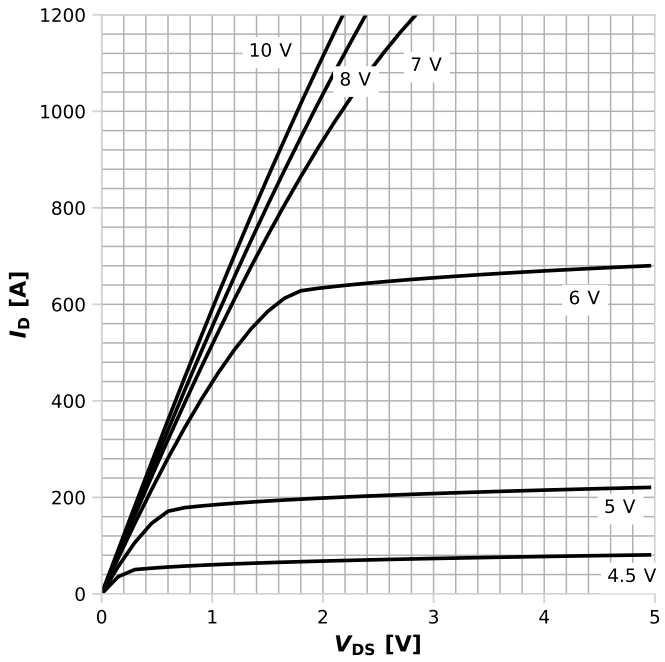
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



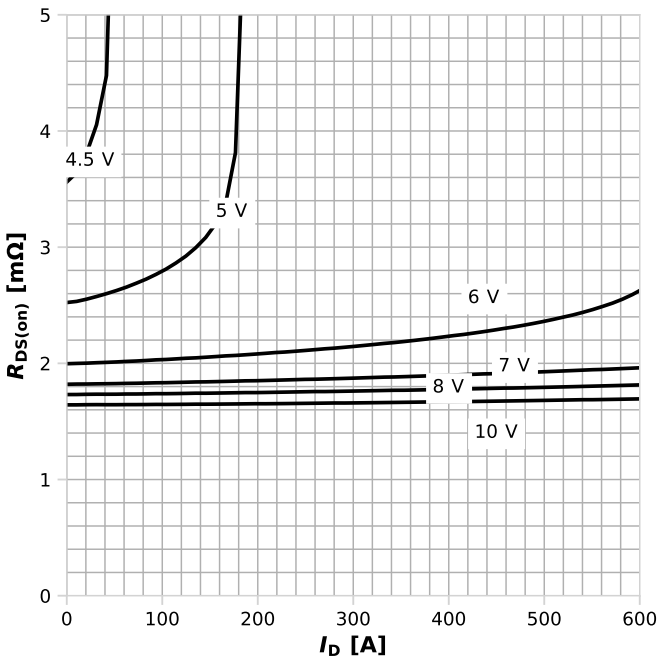
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



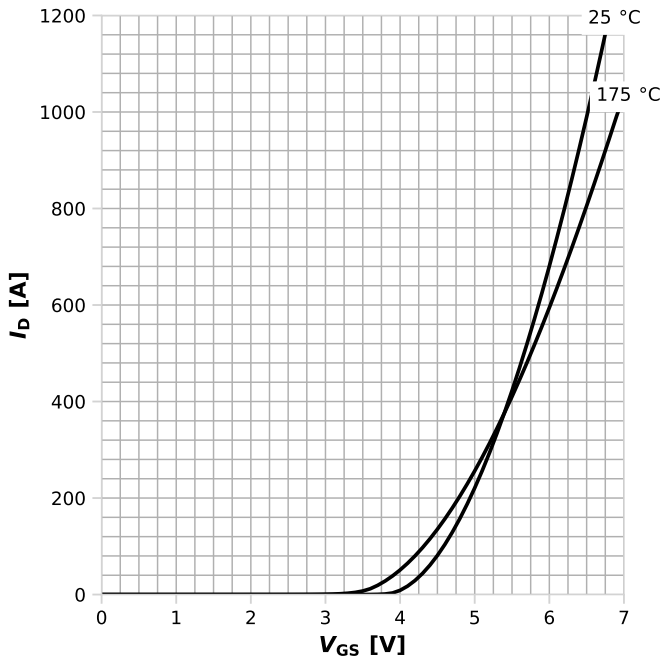
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



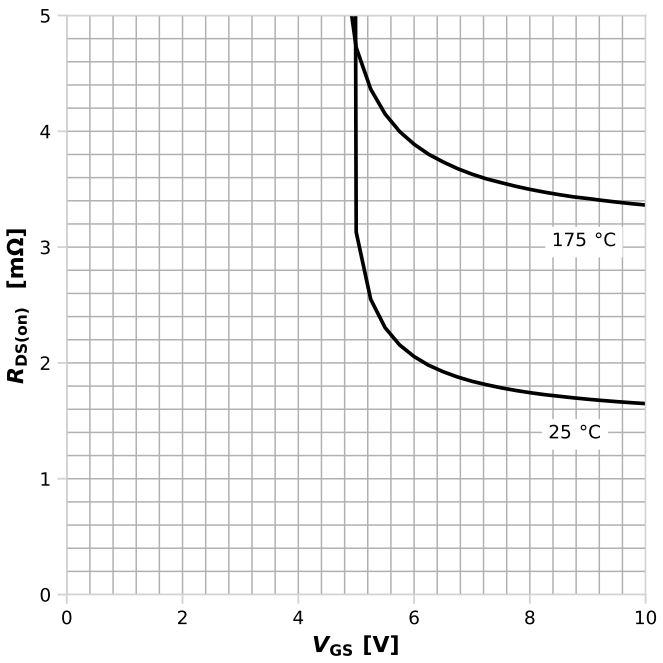
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=150 A; parameter: T_j

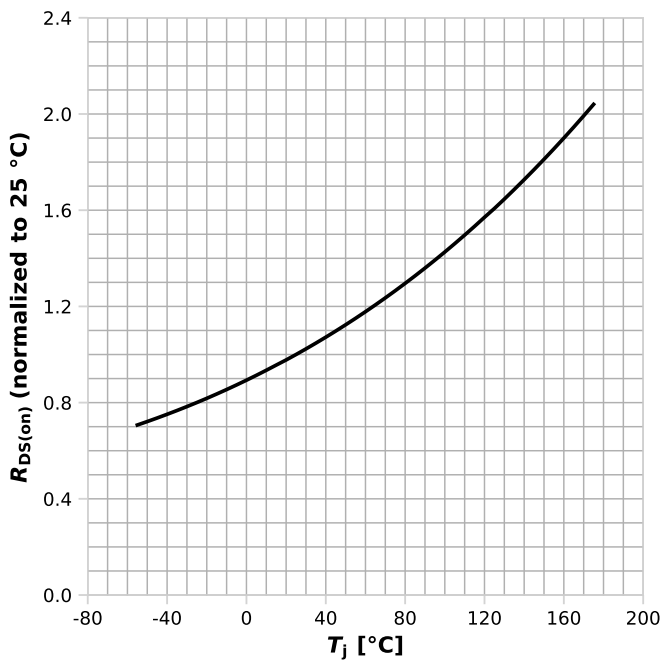
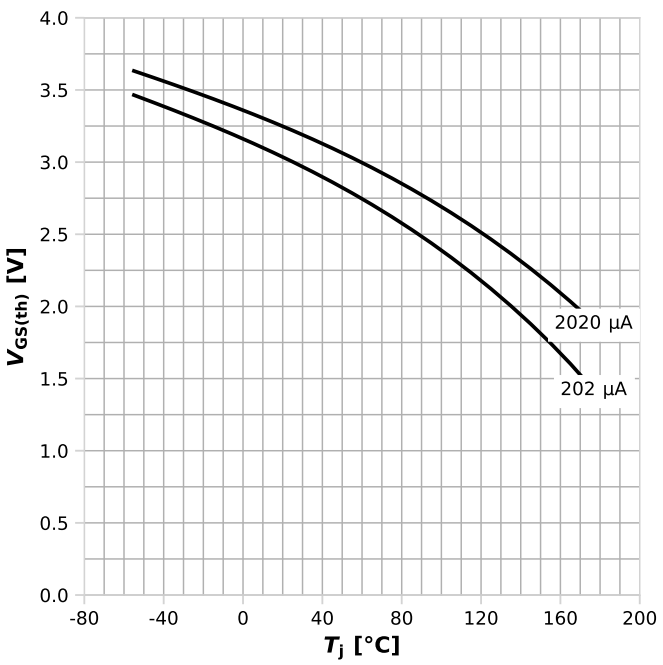
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=150 A, V_{GS}=10 V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

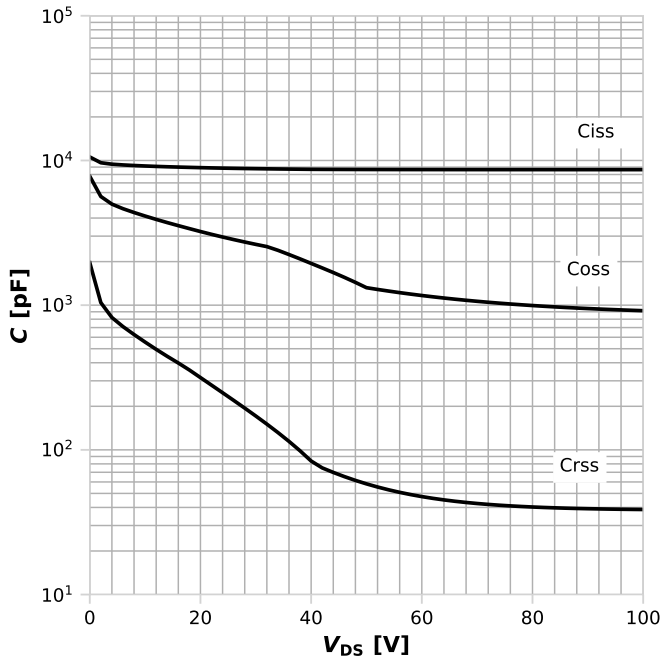
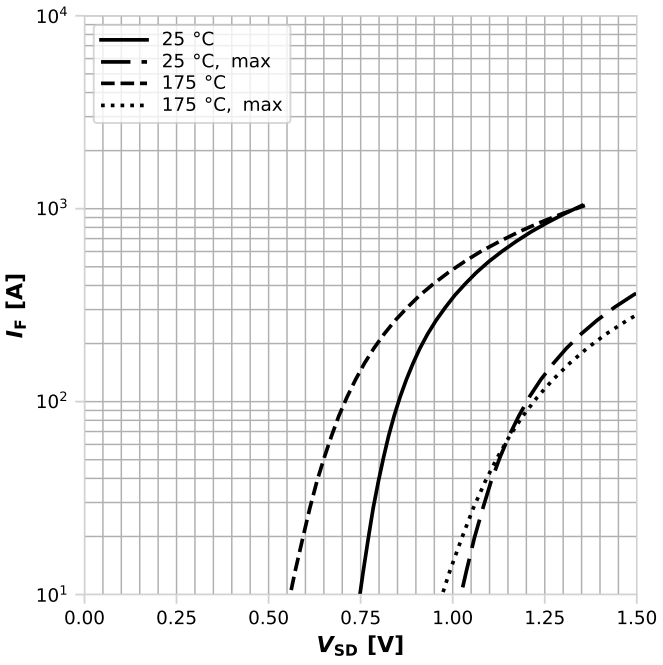
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

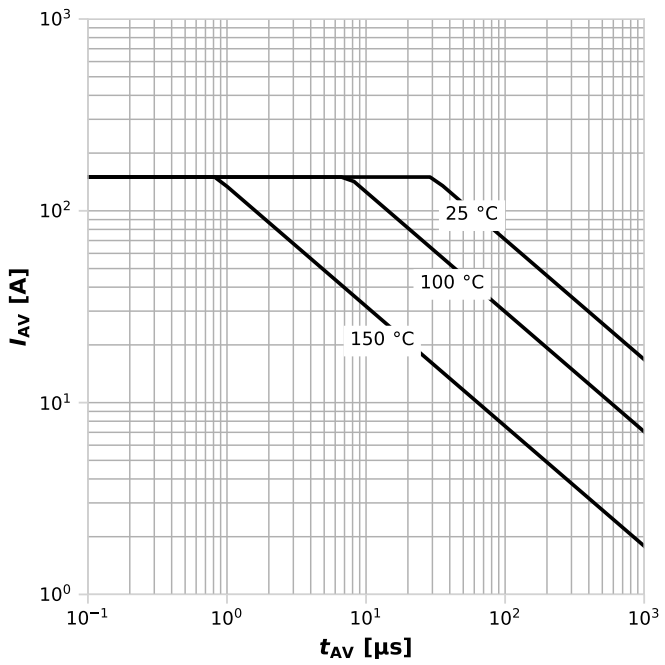
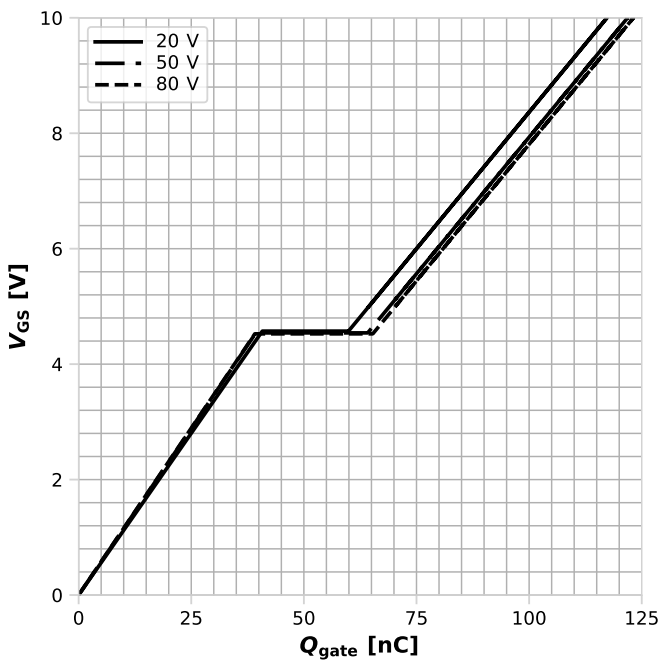
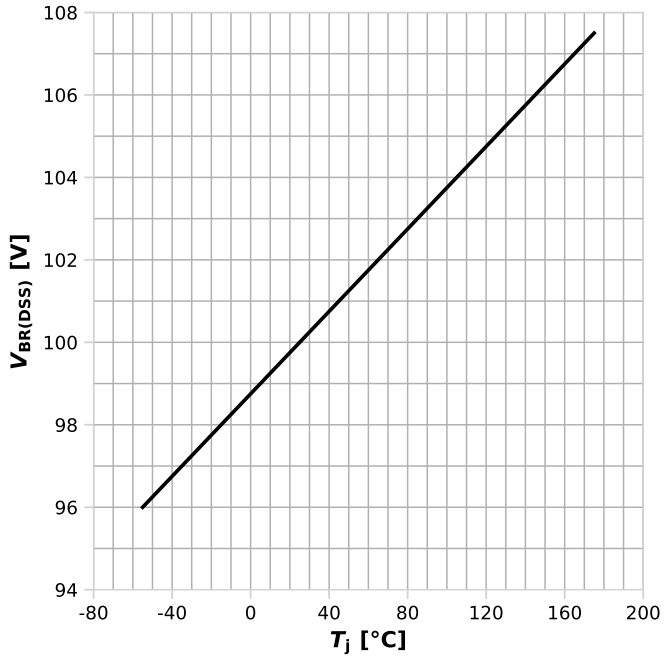
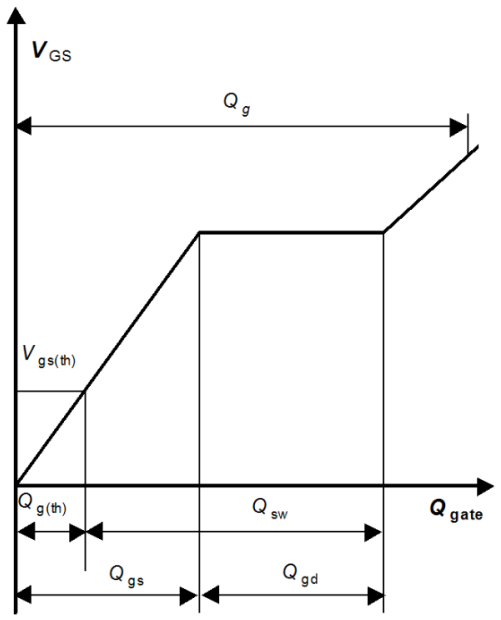
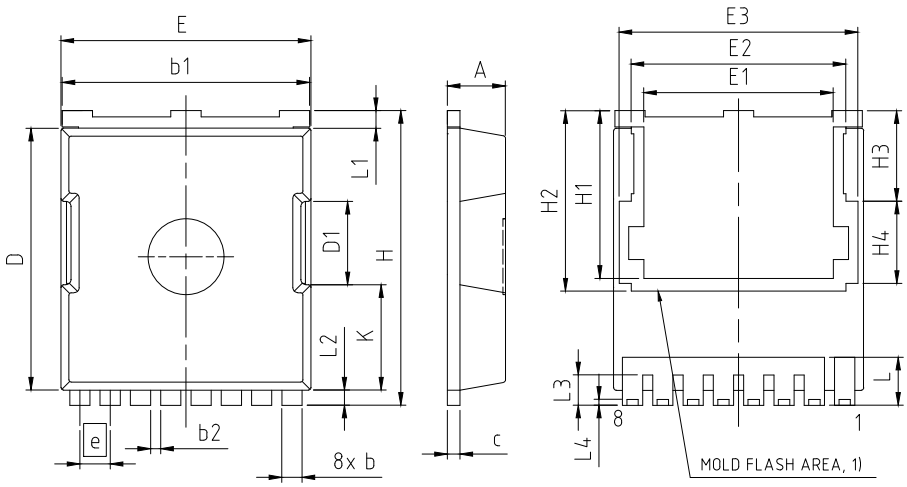
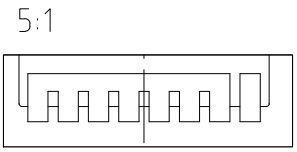
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K	4.18	
L	1.60	2.10
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	0.13	0.33



OPTIONAL LEAD FORM:
WITHOUT LTI OPTION

1) PATIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

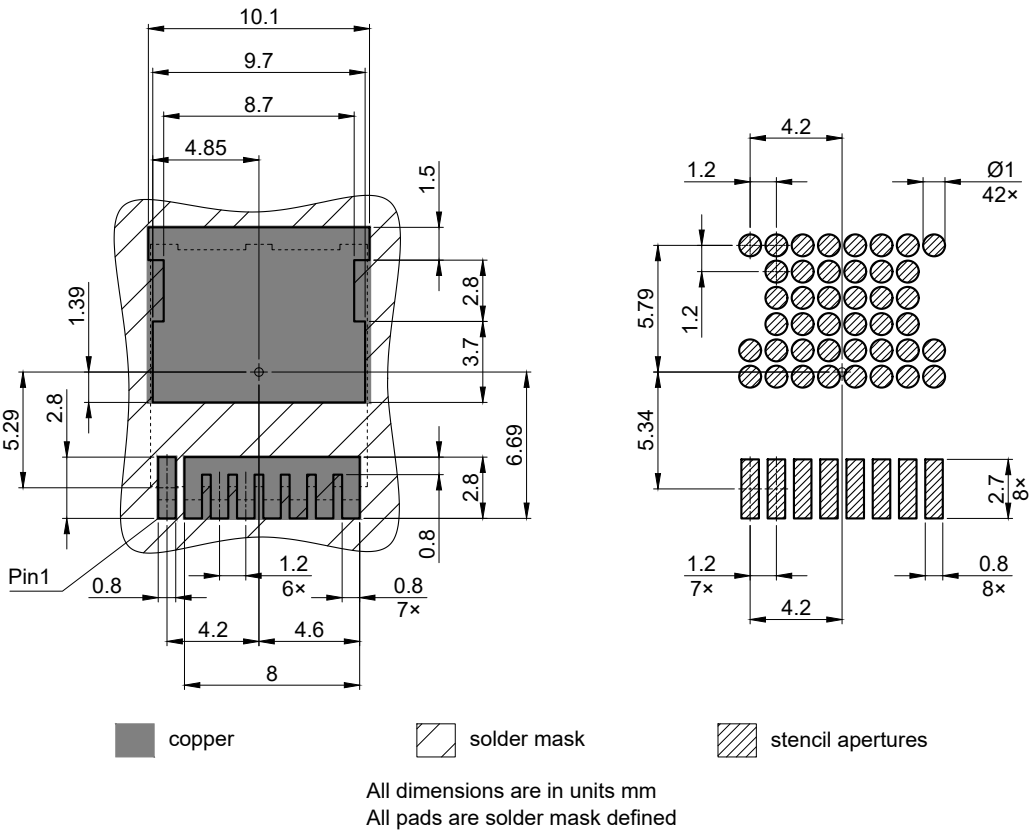


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm

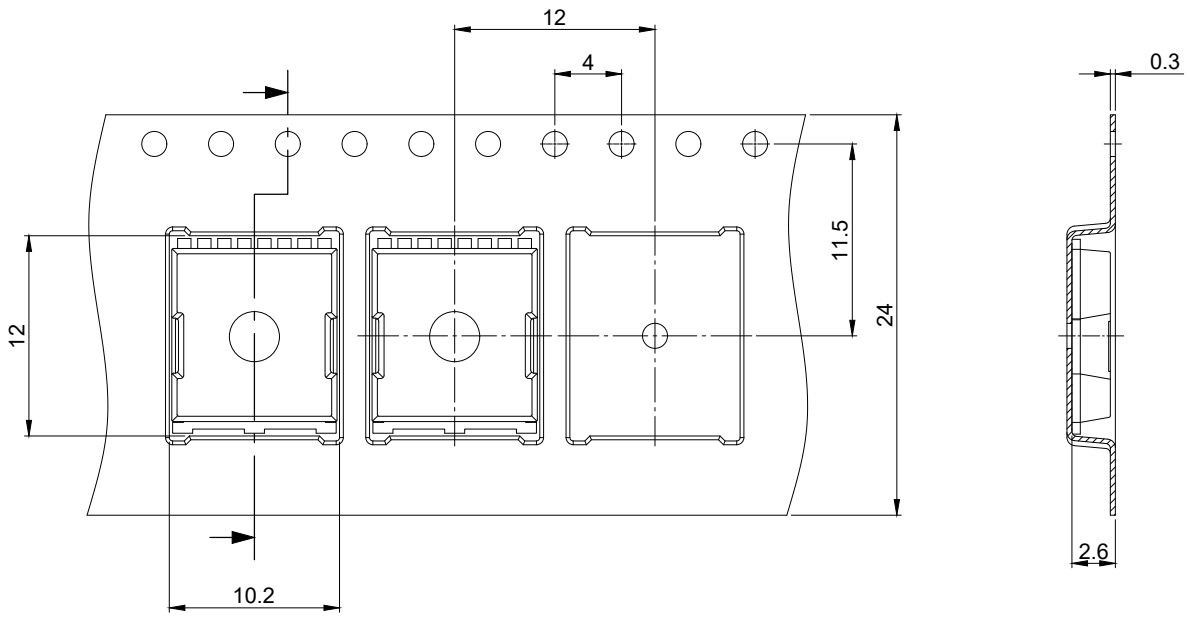


Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

Revision history

IPT020N10N5

Revision 2025-06-02, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2019-03-26	Release of final version
2.1	2025-06-02	Update IDSS 100V max limit

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