

MOSFET

英飞凌工业用 60 V StrongIRFET™2 功率晶体管

特性

- 针对多种应用进行了优化
- N沟道，正常电平
- 100% 雪崩测试
- 无铅镀层；符合RoHS标准
- 符合 IEC61249-2-21 标准的无卤素

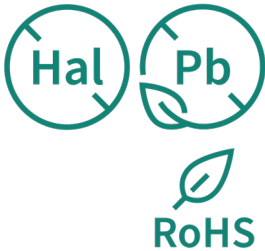
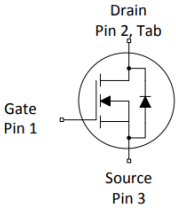
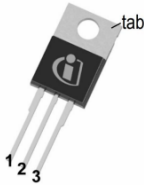
产品验证

符合 JEDEC 标准。

表 1 主要性能参数

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.4	mΩ
I_D	200	A
Q_{oss}	200	nC
$Q_G(0V..10V)$	203	nC

PG-TO220-3



Type/Ordering Code	Package	Marking	Related Links
IPP014N06NF2S	PG-TO220-3	014N06NS	-

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。



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1 最大额定值

除非另有规定， $T_A = 25\text{ °C}$

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	200 154 39	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{THJA}=40\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	800	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	1274	mJ	$I_D=100\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	375 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{THJA}=40\text{ °C/W}^{2)}$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) 额定值的适用条件：产品在数据手册中规定的绝对最大值条件下运行、确保外壳温度

符合规定要求。其他外壳温度请参见图 2。需要根据实际环境条件降低额定值。

2) 器件置于 $40\text{ mm} \times 40\text{ mm} \times 1.5\text{ mm}$ 环氧树脂 PCB FR4 基板上，配有 6 cm^2 （单层，70 微米厚）铜层，用于漏极连接。PCB 垂直放置在静止空气中。

3) 详细信息请参见图 3

4) 详细信息请参见图 13



2 热特性

表3 热特性

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.4	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

⁵⁾ 器件置于40 mm × 40 mm × 1.5 mm 环氧树脂 PCB FR4基板上，配有6 cm²（单层，70微米厚）铜层，用于漏极连接。PCB垂直放置在静止空气中。

3 电气特性

除非另有规定, $T_j = 25\text{ }^{\circ}\text{C}$

表4 静态特性

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}, I_D=246\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.5 10	1 100	μA	$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^{\circ}\text{C}$ $V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance ⁶⁾	$R_{DS(on)}$	-	1.23 1.45	1.40 2.10	m Ω	$V_{GS}=10\text{ V}, I_D=100\text{ A}$ $V_{GS}=6\text{ V}, I_D=50\text{ A}$
Gate resistance	R_G	-	2.7	-	Ω	-
Transconductance ⁷⁾	g_{fs}	140	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}, I_D=100\text{ A}$

⁶⁾ $R_{DS(on)}$ 规定距离封装主体 1.8 mm; 安装在更大的距离会增加整体
每条腿的封装电阻约为 0.04 m Ω m/mm。

⁷⁾ 由设计定义。未经过生产测试。

表5 动态特性

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	13800	-	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Output capacitance	C_{oss}	-	2860	-	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	85	-	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	26	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	34	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	69	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	25	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$

表6 栅极电荷特性 ⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	60	-	nC	$V_{DD}=30\text{ V}, I_D=100\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	39	-	nC	$V_{DD}=30\text{ V}, I_D=100\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	36	-	nC	$V_{DD}=30\text{ V}, I_D=100\text{ A}, V_{GS}=0\text{ to }10\text{ V}$

表 6 栅极电荷特性⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Switching charge	Q_{sw}	-	57	-	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ⁹⁾	Q_g	-	203	305	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	190	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	200	-	nC	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ 有关参数定义, 请参见“栅极电荷波形”。

⁹⁾ 由设计定义。未经过生产测试。

表 7 反向二极管

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	167	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	800	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.88	1.0	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	57	-	ns	$V_R=30\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	73	-	nC	$V_R=30\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time	t_{rr}	-	44	-	ns	$V_R=30\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	259	-	nC	$V_R=30\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$

4 电气特性图

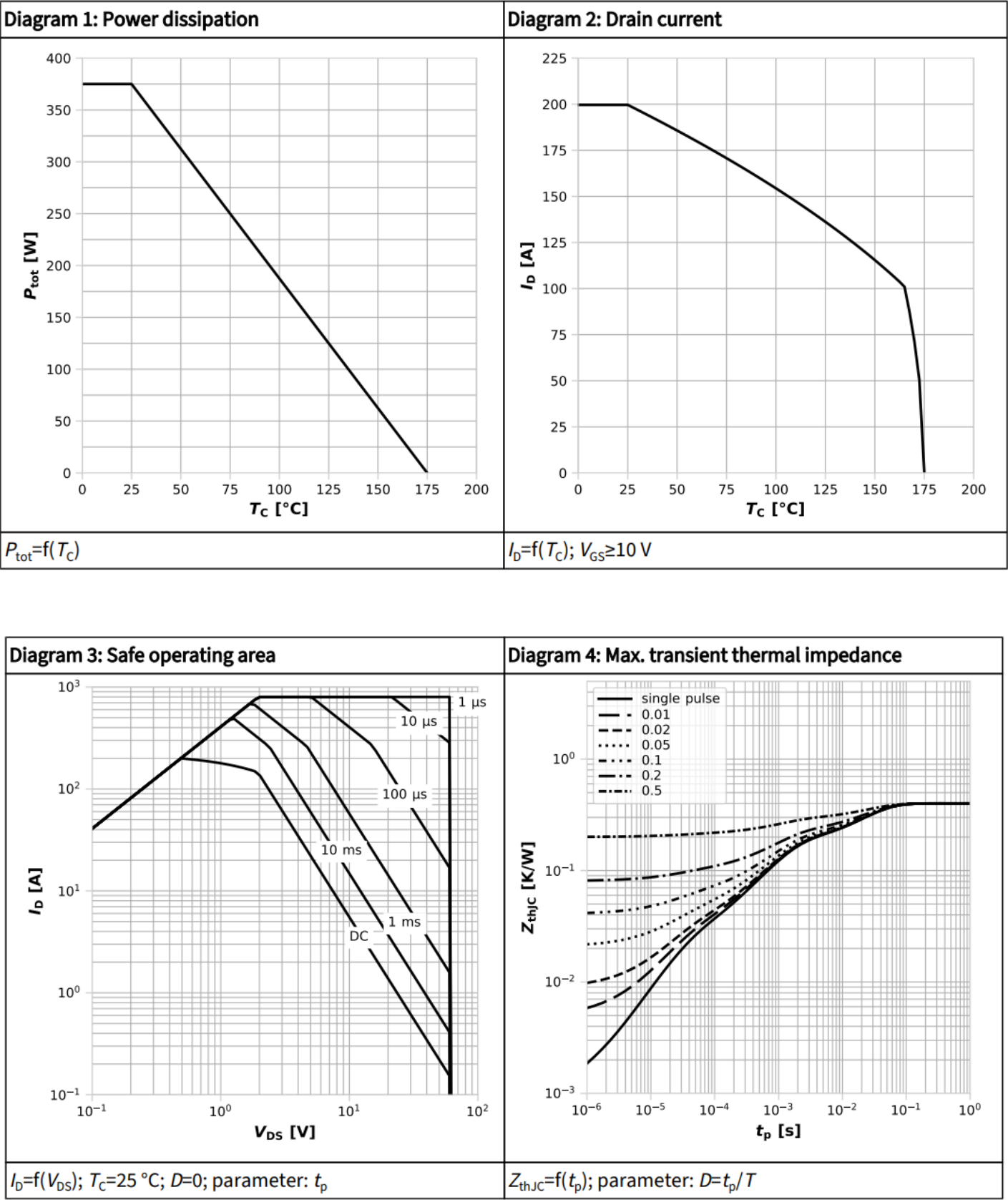


Diagram 5: Typ. output characteristics

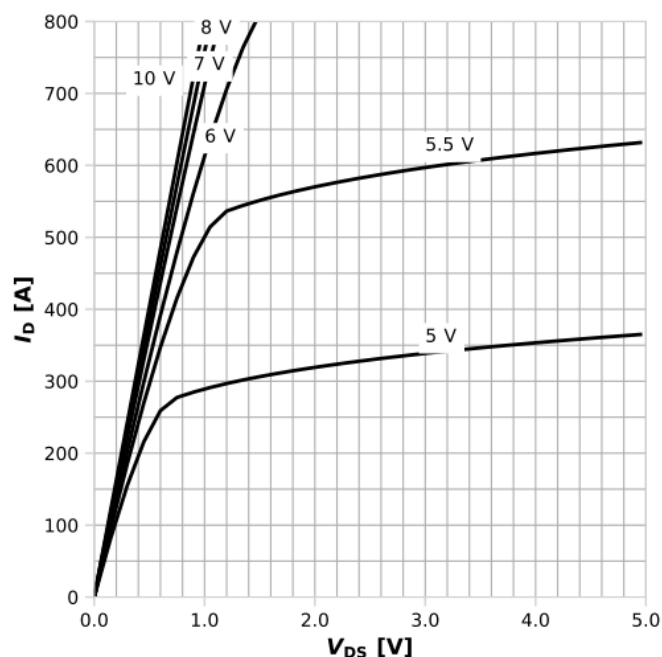

 $I_D = f(V_{DS}), T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance

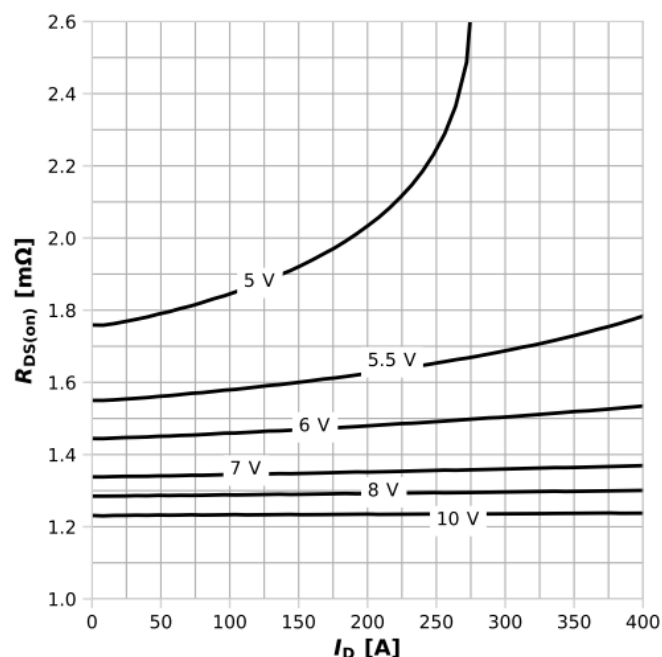

 $R_{DS(on)} = f(I_D), T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics

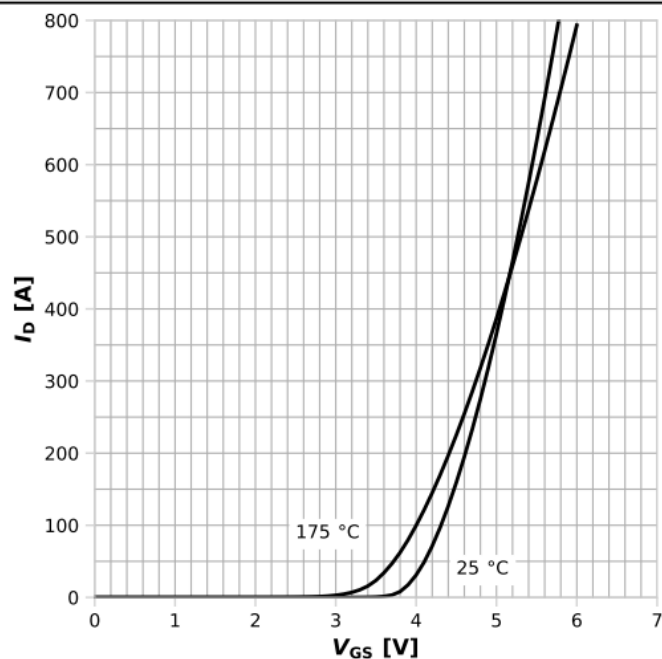

 $I_D = f(V_{GS}), |V_{DS}| > 2|I_D| R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. drain-source on resistance

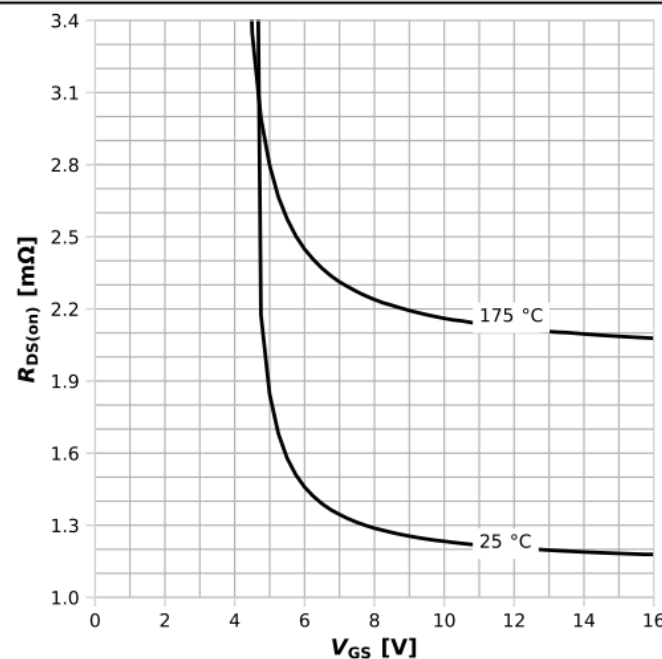
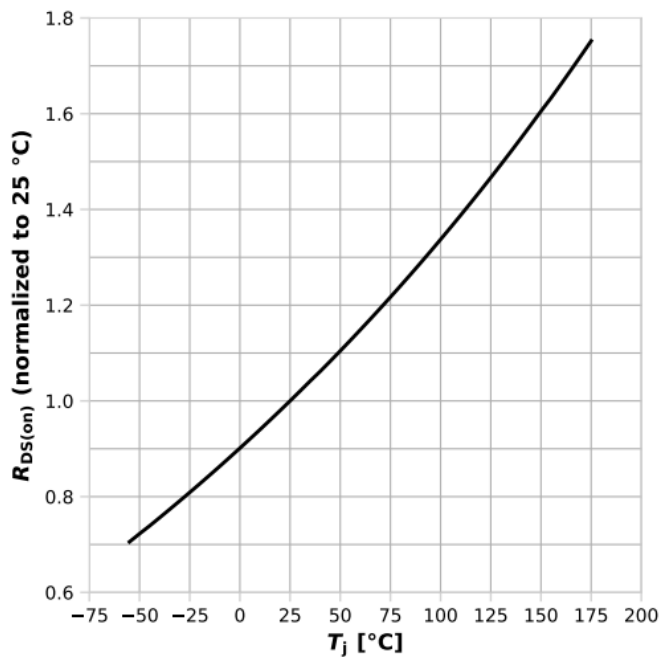
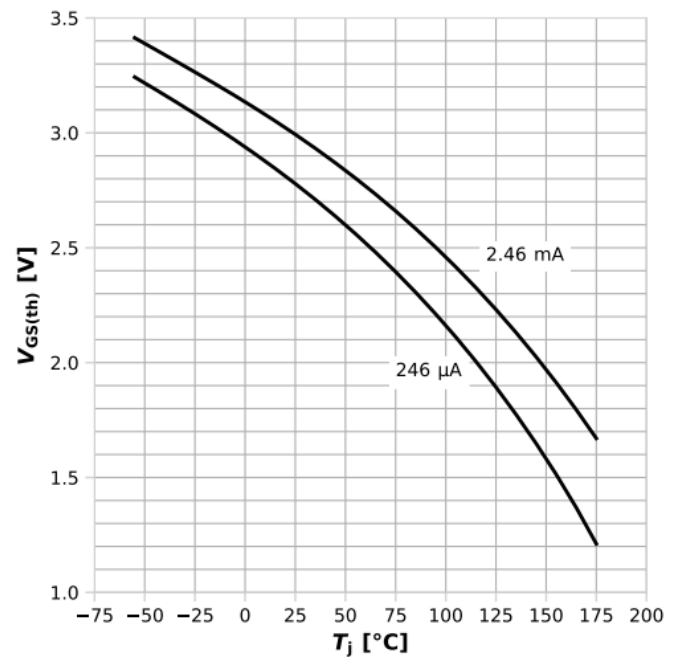

 $R_{DS(on)} = f(V_{GS}), I_D = 100\text{ A}; \text{parameter: } T_j$

Diagram 9: Normalized drain-source on resistance



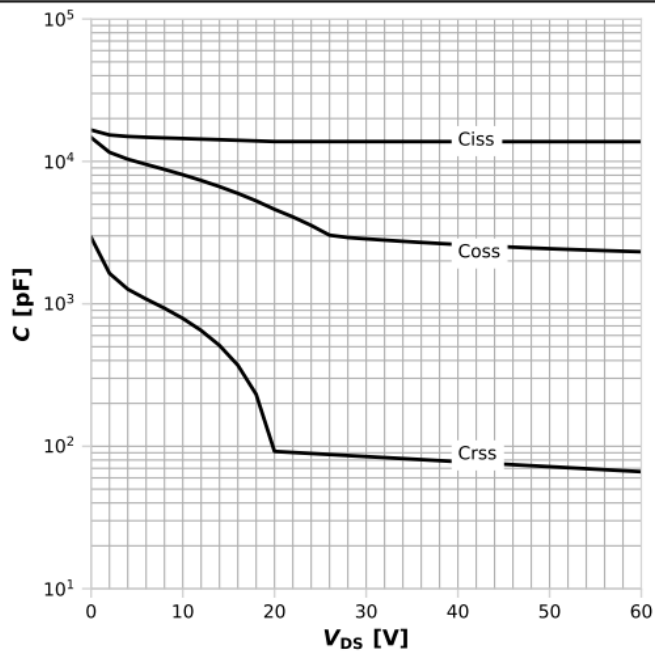
$$R_{DS(on)} = f(T_j), I_D = 100 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



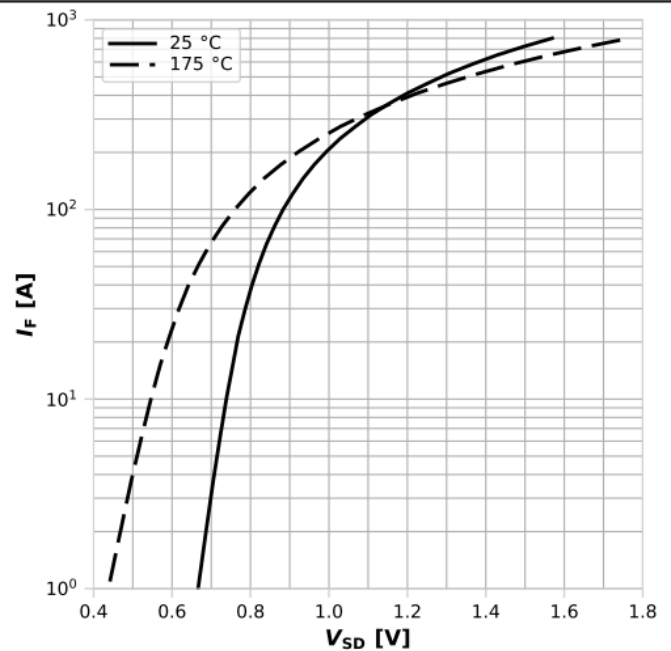
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



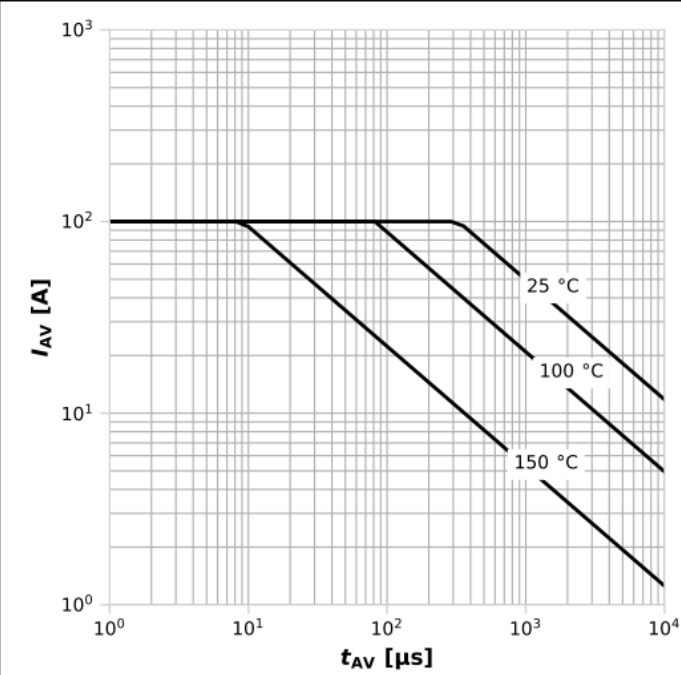
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



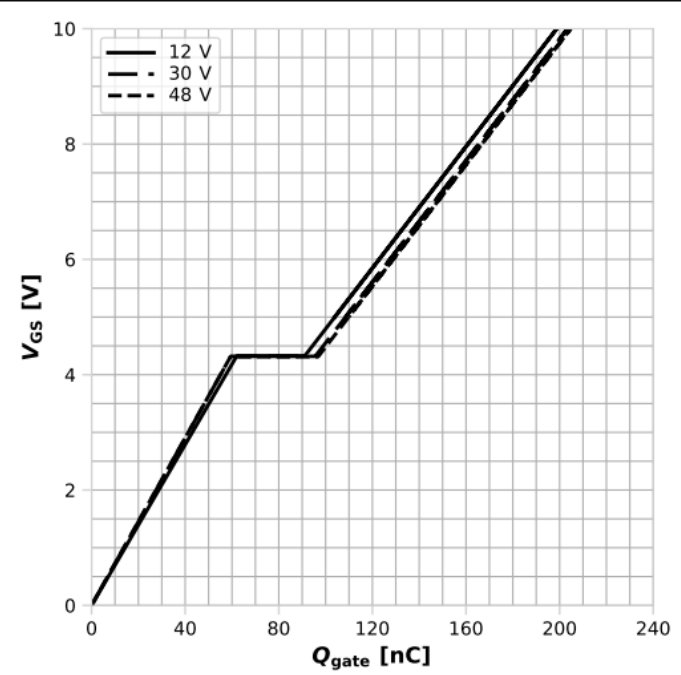
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



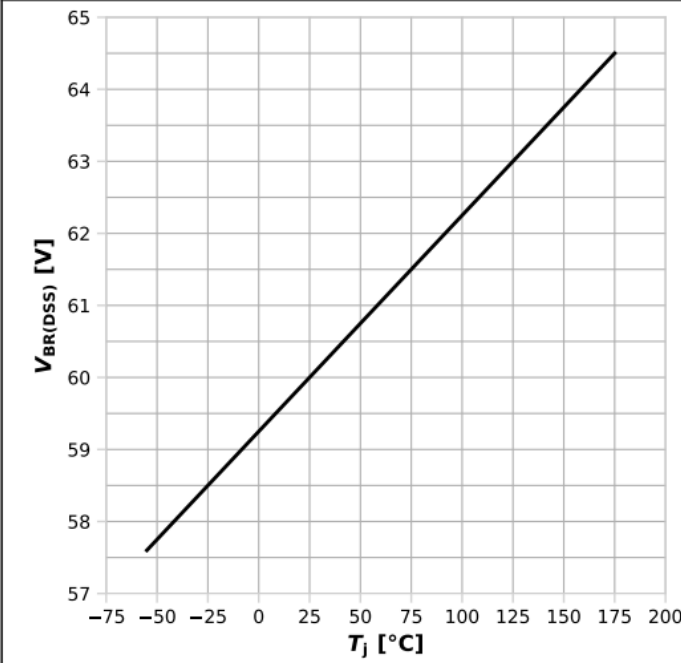
$$I_{AS}=f(t_{AV}); R_{GS}=25\,\Omega; \text{parameter: } T_{j,\text{start}}$$

Diagram 14: Typ. gate charge



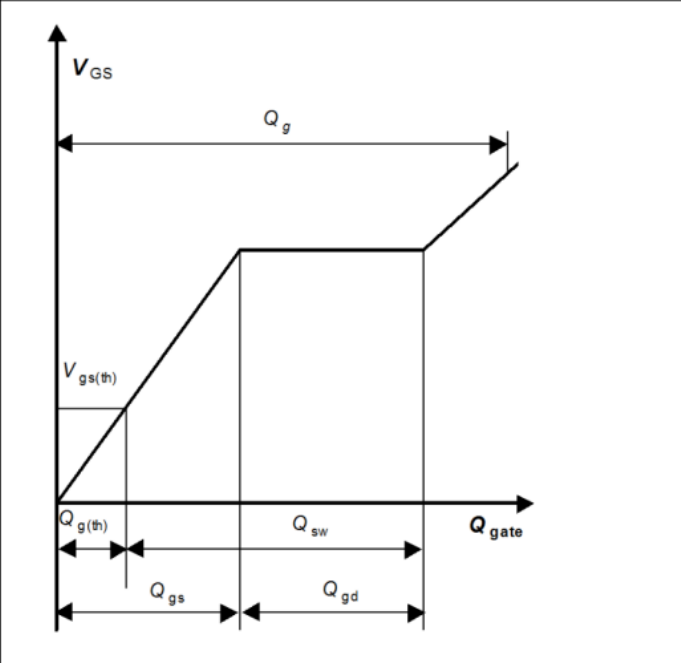
$$V_{GS}=f(Q_{gate}), I_D=100\,\text{A pulsed}, T_j=25\,^{\circ}\text{C}; \text{parameter: } V_{DD}$$

Diagram 15: Drain-source breakdown voltage



$$V_{BR(DSS)}=f(T_j); I_D=1\,\text{mA}$$

Gate charge waveforms



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5 封装外形尺寸

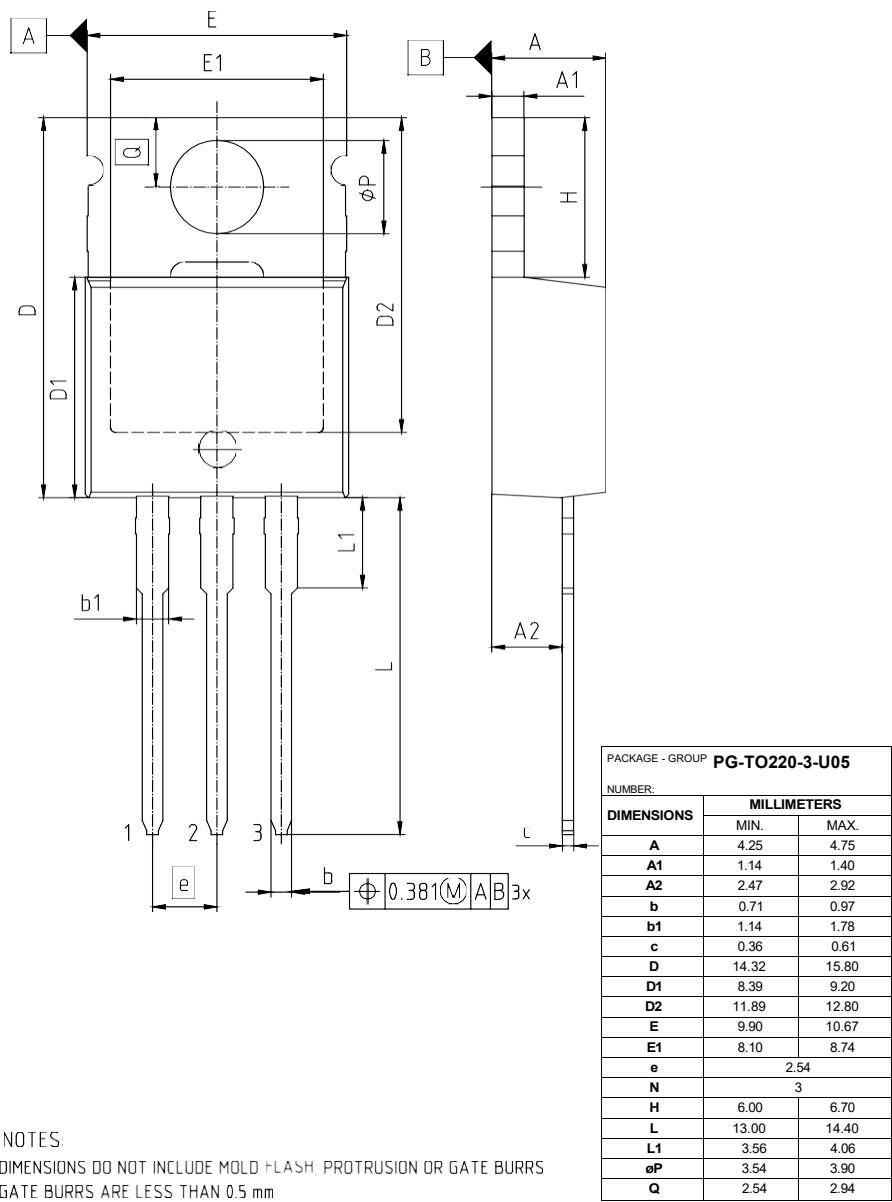


图 1 PG- TO220 - 3外形图，尺寸单位为毫米

修订记录

IPP014N06NF2S

Revision 2024 - 10 - 07 , Rev. 2 .3

历史修订版本

Revision	Date	Subjects (major changes since last revision)
2.0	2022-01-18	Release of final version
2.1	2022-02-15	Updated the x-axis scale on diagrams 6 & 15
2.2	2022-05-16	Updated diagram 12 title
2.3	2024-10-07	Added trr and Qrr at diF/dt=100 A/μs

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