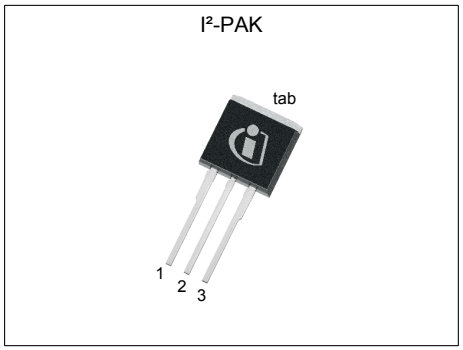
MOSFET

OptiMOS™3 Power-Transistor, 150 V



Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

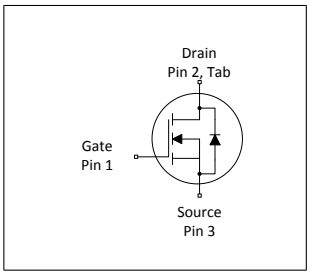


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on)}$	7.5	mΩ
I_D	120	A

Type / Ordering Code	Package	Marking	Related Links
IPI075N15N3 G	PG-TO 262-3	075N15N	-

[1] J-STD20 and JESD22

Table of Contents

1 Maximum ratings

at T_A= 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	120 91	A	T_C=25 °C T_C=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	480	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	780	mJ	I_D=100 A, R_{GS}=25 Ω
Reverse diode dv/dt	dv/dt	-	-	6	kV/µs	I_D=100 A, V_{DS}=120 V, di/dt=100 A/µs, $T_{j,max}$=175 °C
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area[2]	R_{thJA}	-	-	40	K/W	-

[1] See Diagram 3
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate theshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS}, I_D=270 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	6.2 6.4	7.5 7.7	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=8 V, I_D=50 A
Gate resistance	R_G	-	2.3	-	Ω	-
Transconductance	g_{fs}	65	130	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5470	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance	C_{oss}	-	638	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	10	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	25	38	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, R_G=1.6 Ω
Rise time	t_r	-	35	52	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, R_G=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	46	69	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, R_G=1.6 Ω
Fall time	t_f	-	14	21	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=100 A, R_G=1.6 Ω

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	30	40	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	11	17	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	25	35	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	70	93	nC	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	V_{DD}=75 V, I_D=100 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	179	239	nC	V_{DD}=75 V, V_{GS}=0 V

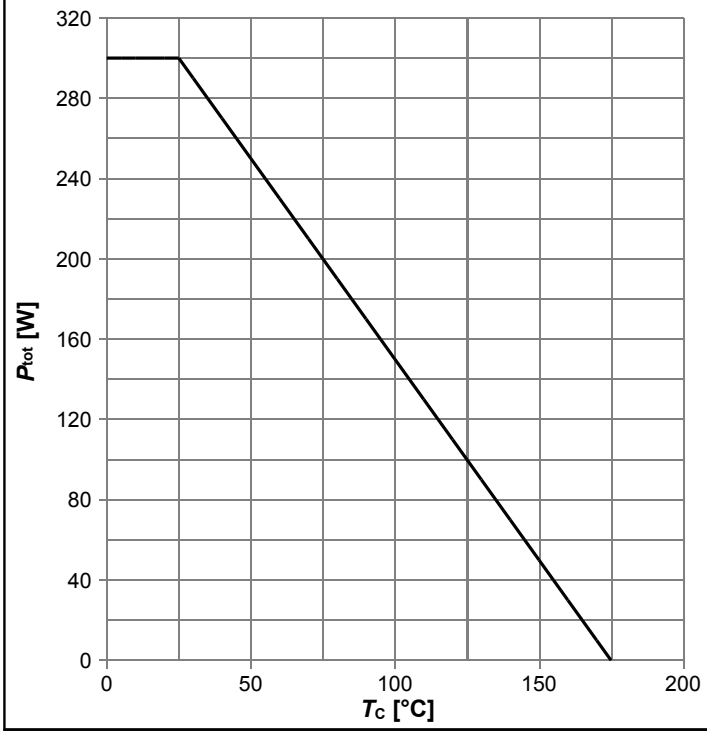
[1)] See ″Gate charge waveforms″ for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	120	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	480	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	1	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	146	-	ns	V_R=75 V, I_F=I_S, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	478	-	nC	V_R=75 V, I_F=I_S, di_F/dt=100 A/µs

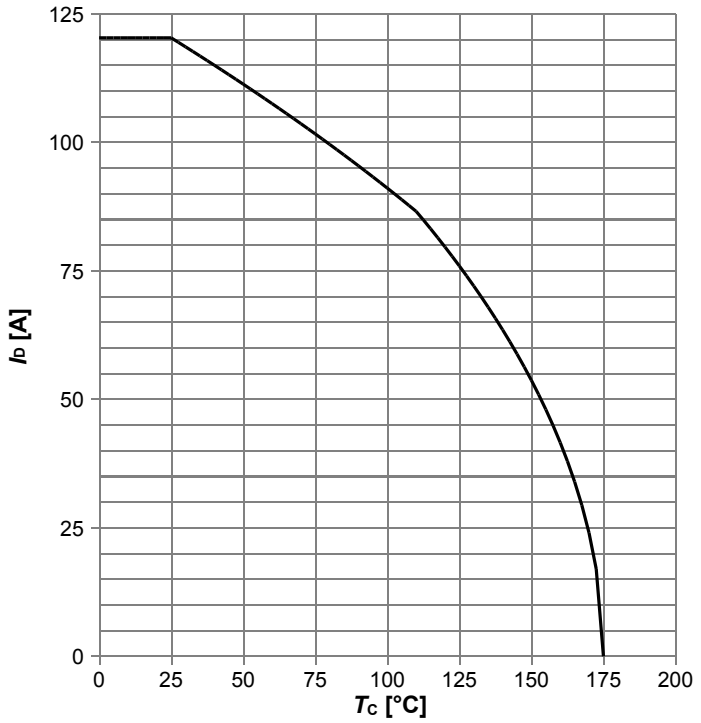
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



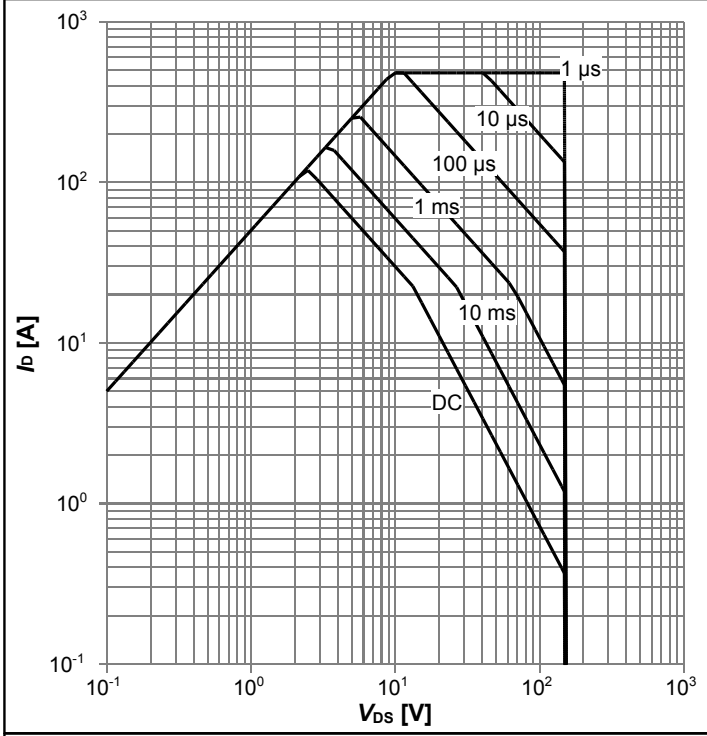
$P_{tot}=f(T_C)$

Diagram 2: Drain current



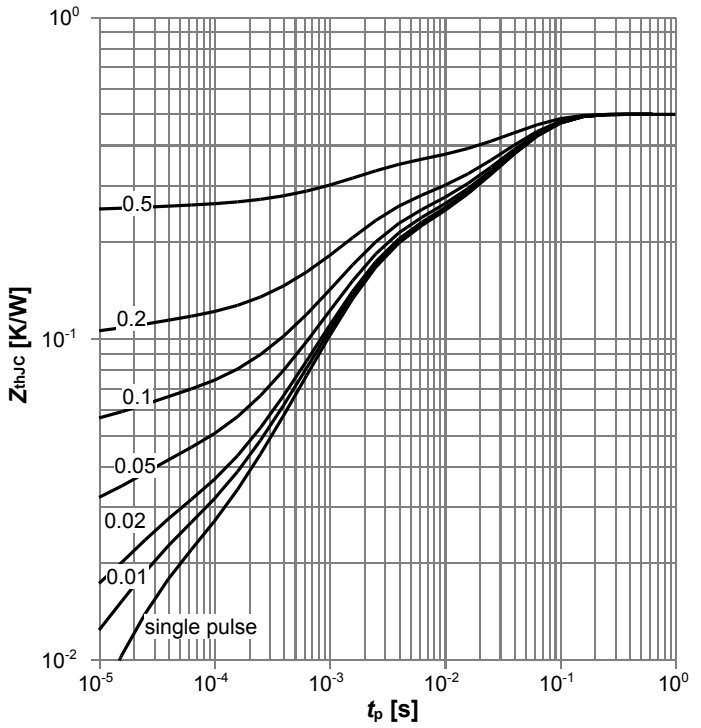
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



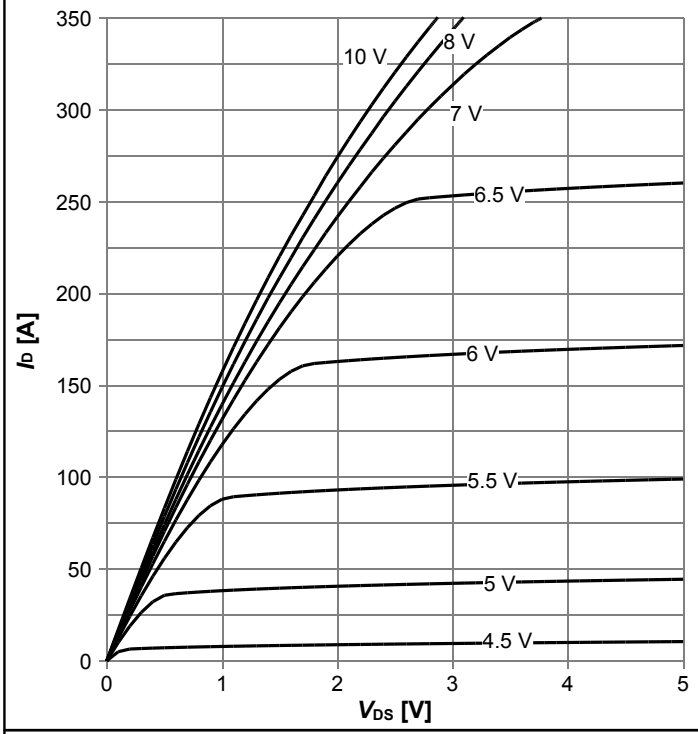
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



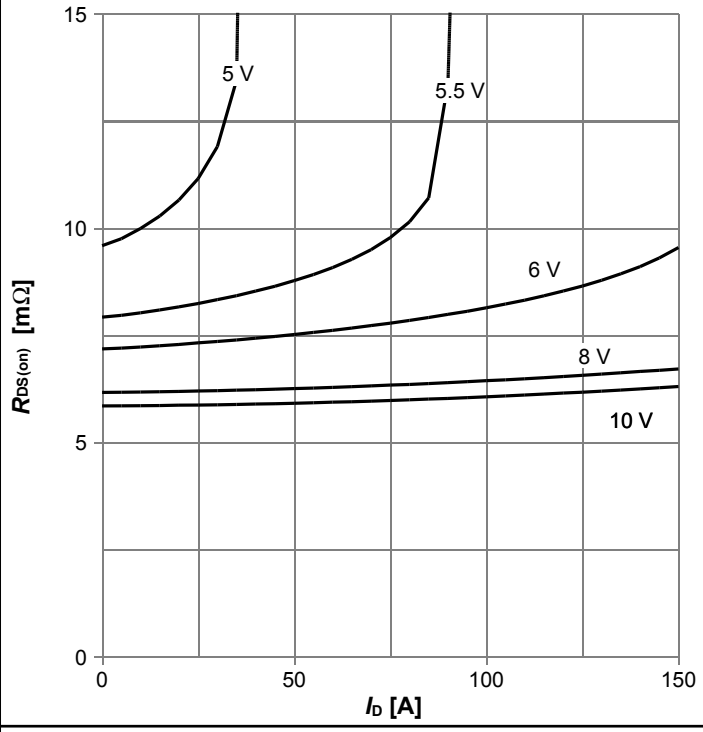
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



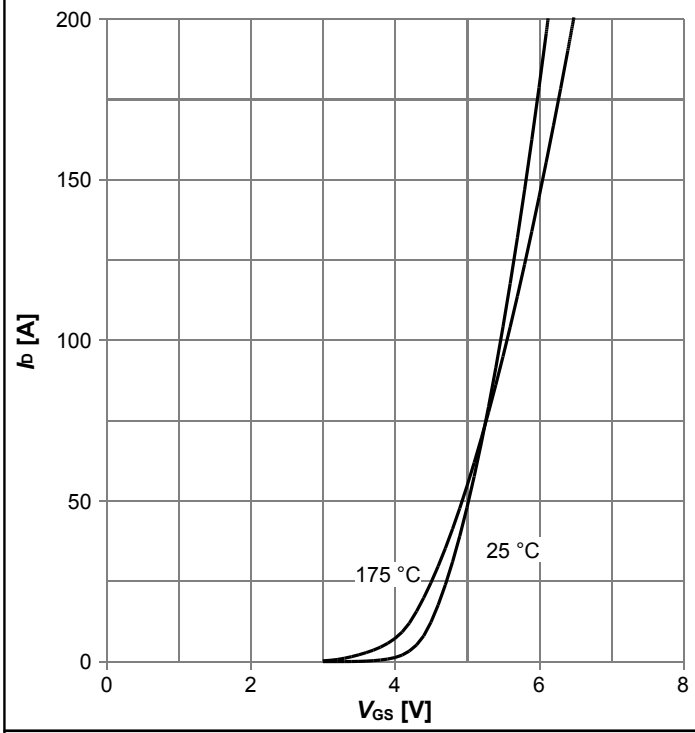
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



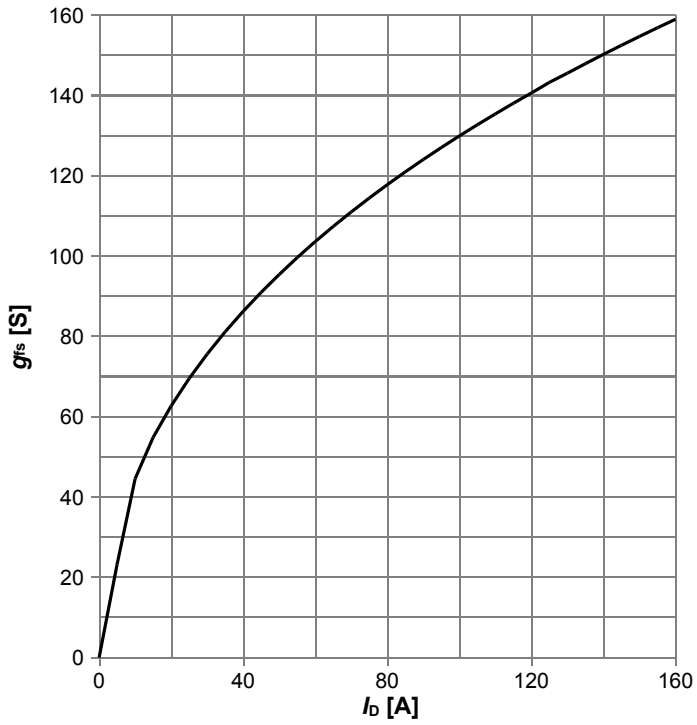
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



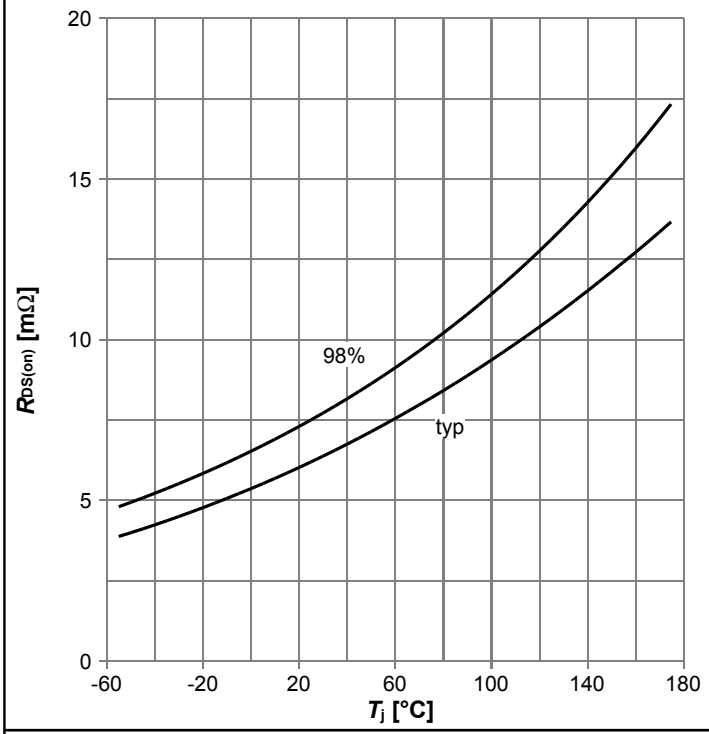
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



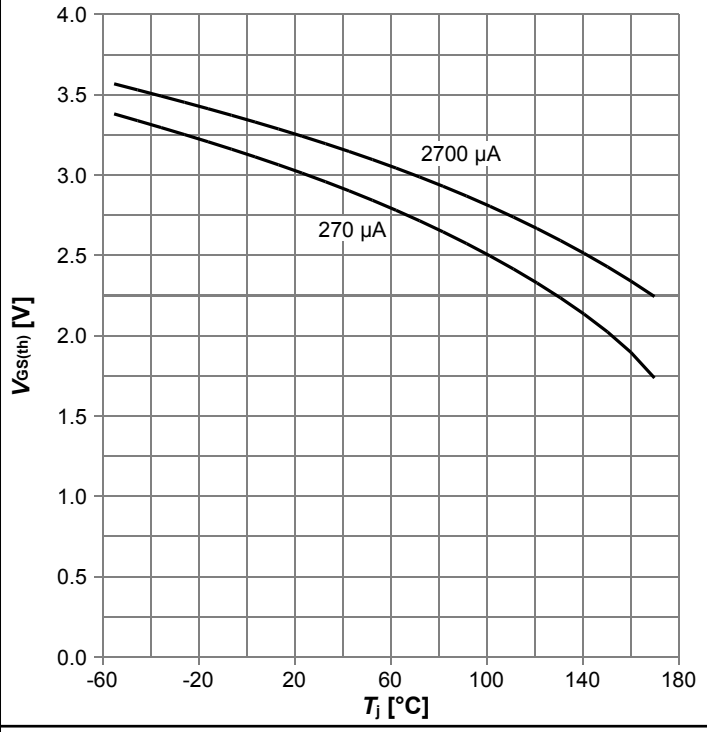
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



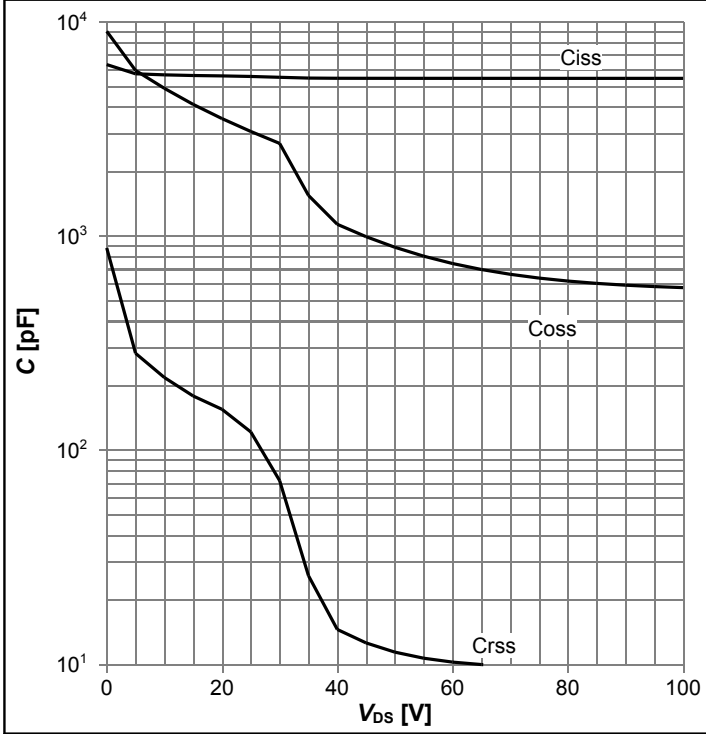
$R_{DS(on)}$=f(T_j); I_D=100 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



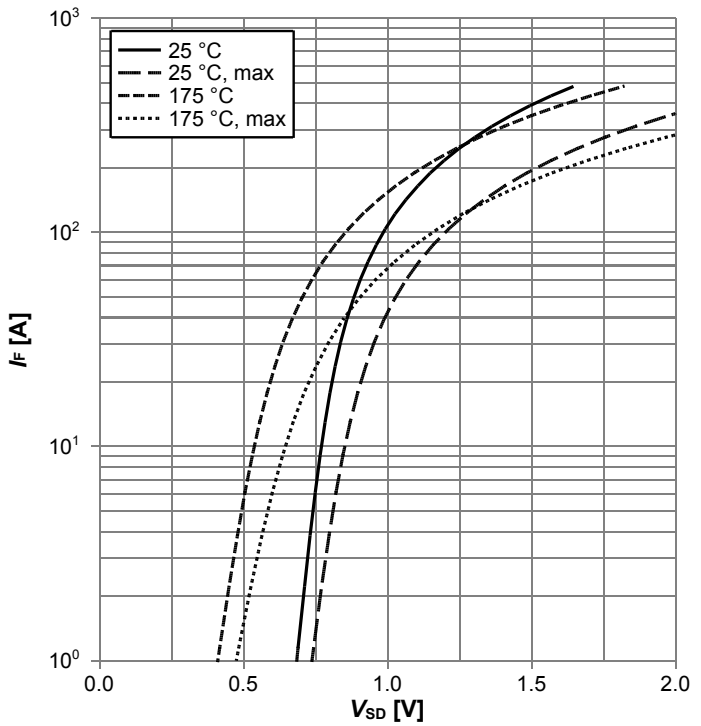
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



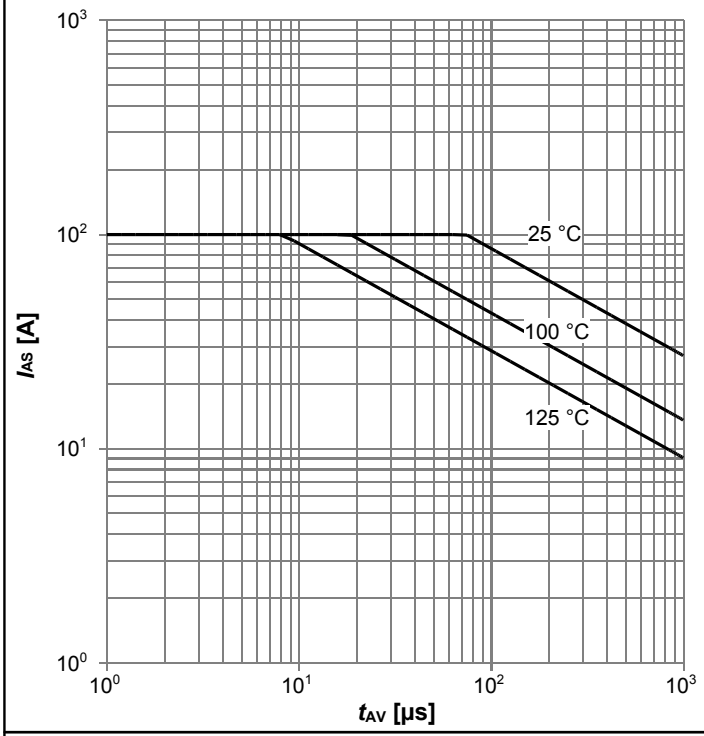
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



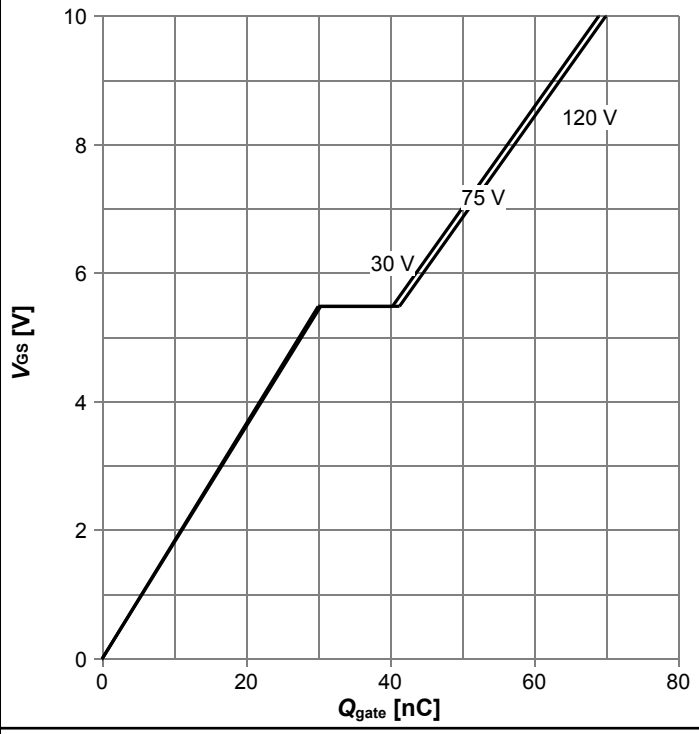
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



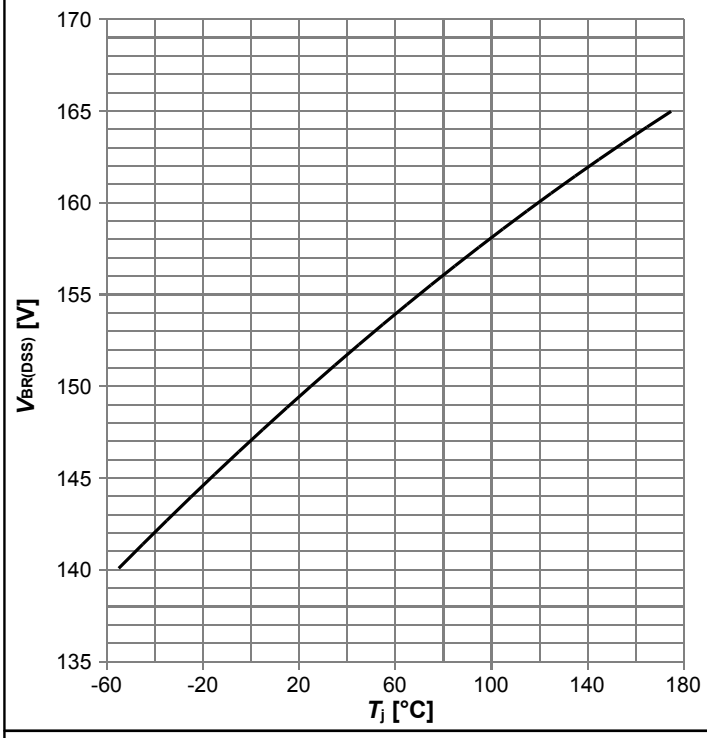
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



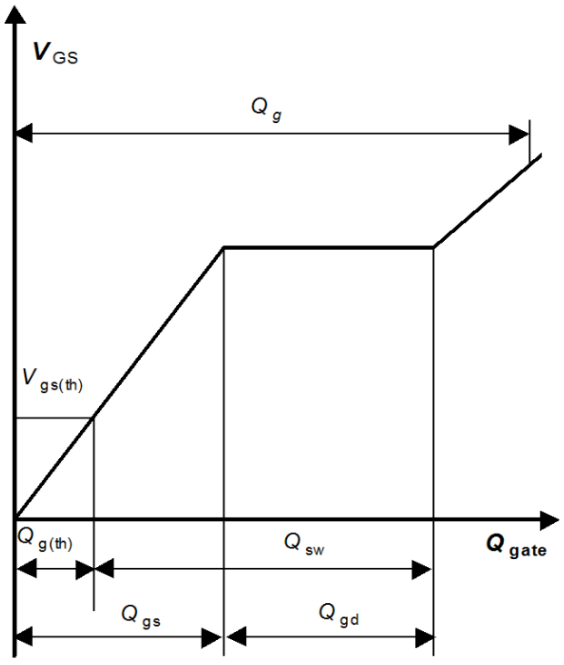
$V_{GS}=f(Q_{gate})$; $I_D=100$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

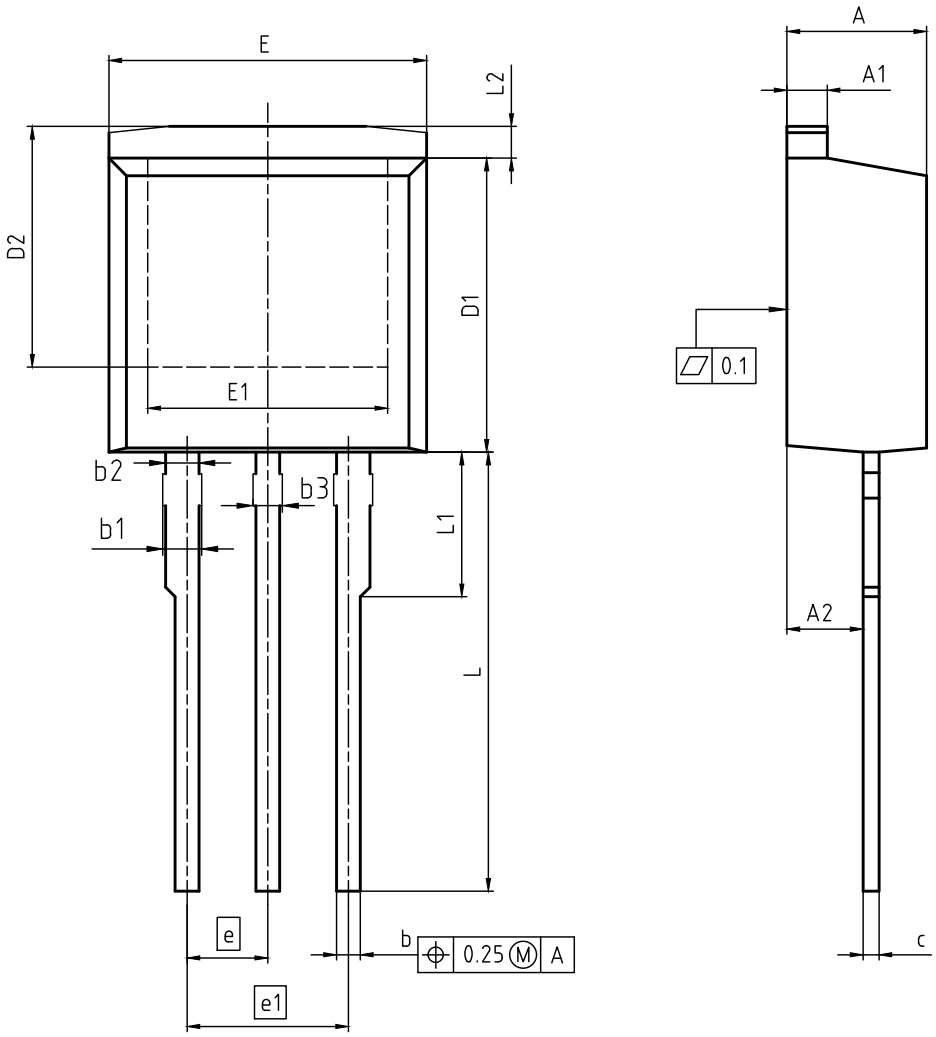


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.57
A1	1.17	1.40
A2	2.15	2.72
b	0.65	0.86
b1	0.95	1.40
b2	0.95	1.15
b3	0.65	1.15
c	0.33	0.60
D1	8.51	9.45
D2	6.90	-
E	9.70	10.36
E1	6.50	8.60
e	2.54	
e1	5.08	
N	3	
L	13.00	14.00
L1	-	4.80
L2	-	1.73

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REVISION
05

SCALE 5:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION

ISSUE DATE
29.11.2018

Figure 1 Outline PG-TO 262-3, dimensions in mm

Revision History

IPI075N15N3 G

Revision: 2019-02-04, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.1	2019-02-04	Update current and package outline

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