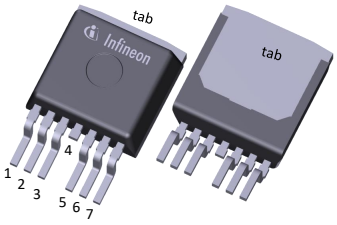
MOSFET

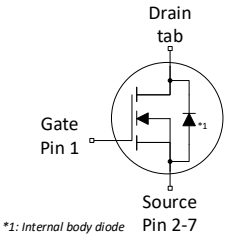
OptiMOS™ 8 Power-Transistor, 100 V

D²-PAK 7pin



Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- High I_D current rating
- Tight $V_{GS(th)}$ spread
- Soft body diode recovery and low Q_{rr}
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

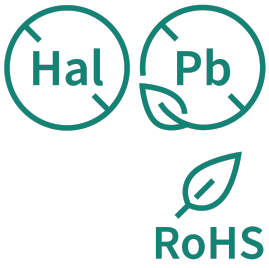


Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	0.94	mΩ
I_D	408	A
Q_{oss}	499	nC
Q_G (0 V...10 V)	255	nC
Q_{rr} (100 A/µs)	89	nC



Part number	Package	Marking	Related links
IPF009N10NM8	PG-TO263-7	009N10N8	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	408	A	V_{GS}=10 V, T_C=25 °C
				312		V_{GS}=10 V, T_C=100 °C
				312		V_{GS}=15 V, T_C=100 °C
				42		V_{GS}=10 V, T_A=25 °C, R_{THJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1632	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	1170	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	500	W	T_C=25 °C
				3.8		T_A=25 °C, R_{THJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 14 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.2	0.3	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5)]	R_{thJA}		-	40		
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}		-	62		

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.4	2.8	3.2	V	V_{DS}=V_{GS}, I_D=279 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C
Zero gate voltage drain current [6]	I_{DSS}	-	10	100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.83	0.94	mΩ	V_{GS}=15 V, I_D=100 A
			0.87	0.99		V_{GS}=10 V, I_D=100 A
			0.93	1.03		V_{GS}=8 V, I_D=50 A
Gate resistance [6]	R_G	-	1.1	2.3	Ω	-
Transconductance [6]	g_{fs}	160	320	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	16000	21000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [7]	C_{oss}		2400	3100		
Reverse transfer capacitance [7]	C_{rss}		450	790		
Turn-on delay time	$t_{d(on)}$	-	29	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		15			
Turn-off delay time	$t_{d(off)}$		86			
Fall time	t_f		30			

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	69	-	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		46	-	nC	
Gate to drain charge [9)]	Q_{gd}		62	93	nC	
Switching charge	Q_{sw}		85	-	nC	
Gate charge total [9)]	Q_g		255	319	nC	
Gate plateau voltage	$V_{plateau}$		4.2	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	213	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	499	664	nC	V_{DS}=50 V, V_{GS}=0 V

[8)] See "Gate charge waveforms" for parameter definition

[9)] Defined by design. Not subject to production test.

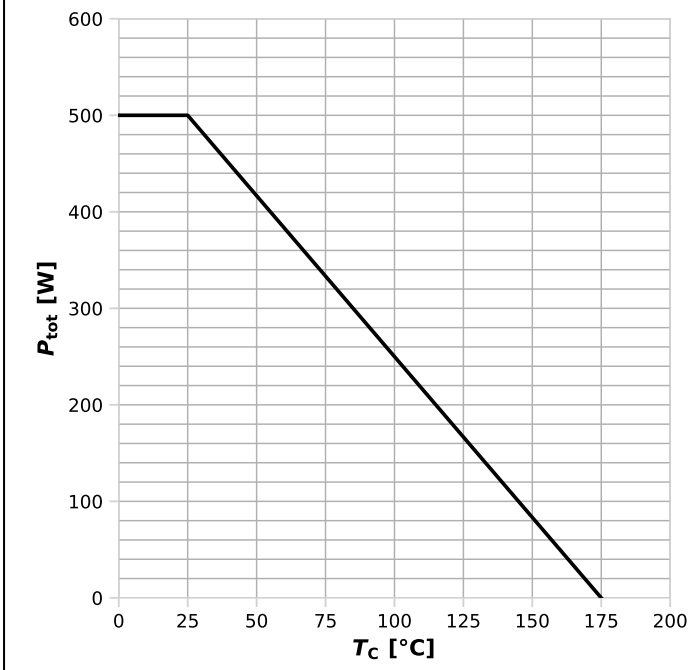
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	336	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			1632		
Diode forward voltage	V_{SD}	-	0.83	1	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	48	96	ns	V_R=50 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}		89	178	nC	
Reverse recovery time [10)]	t_{rr}	-	53	106	ns	V_R=50 V, I_F=50 A, di_F/dt=1000 A/µs
Reverse recovery charge [10)]	Q_{rr}		804	1608	nC	

[10)] Defined by design. Not subject to production test.

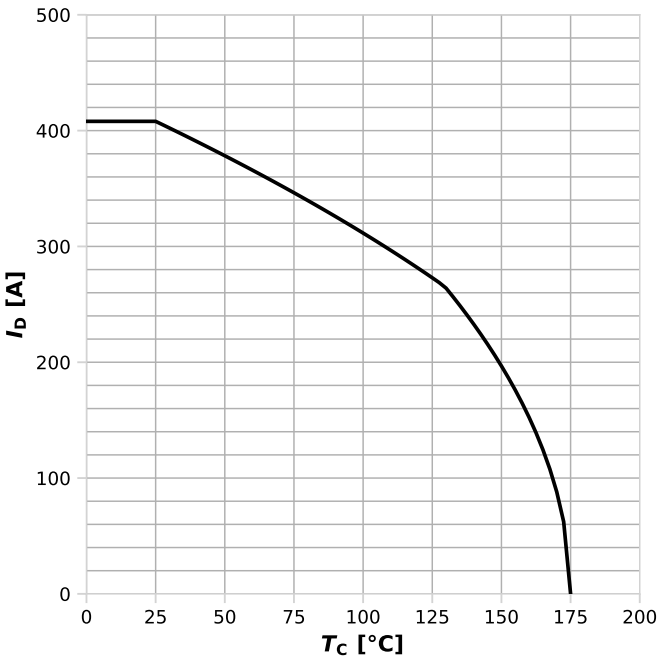
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



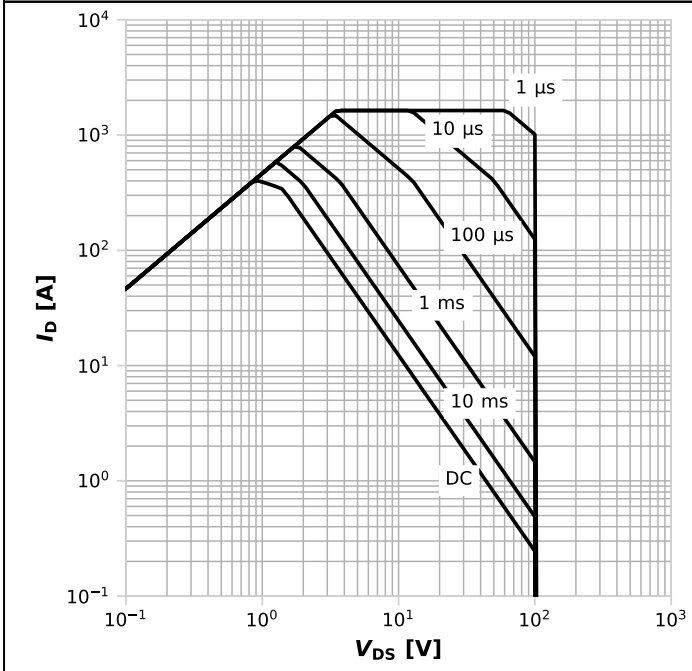
P_{tot}=f(T_C)

Diagram 2: Drain current



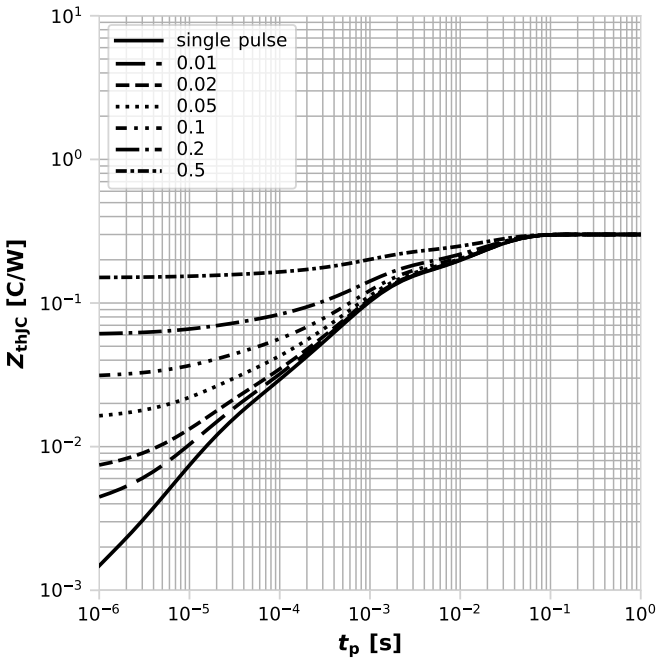
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



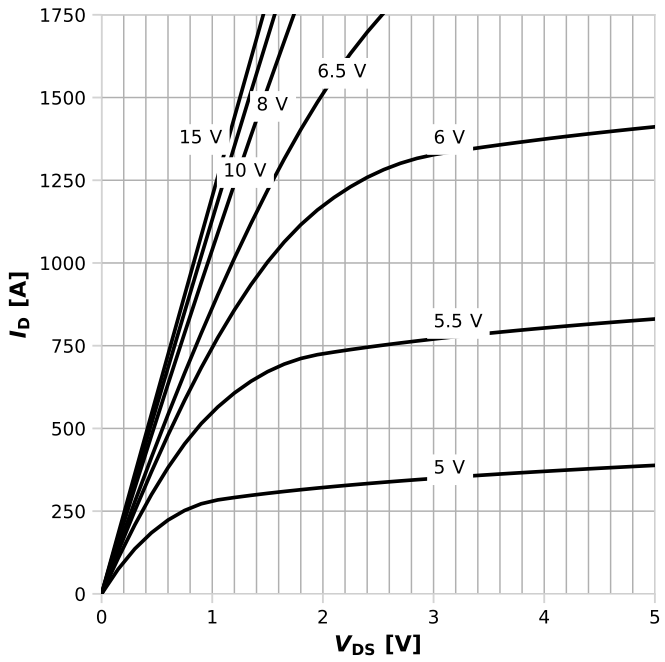
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



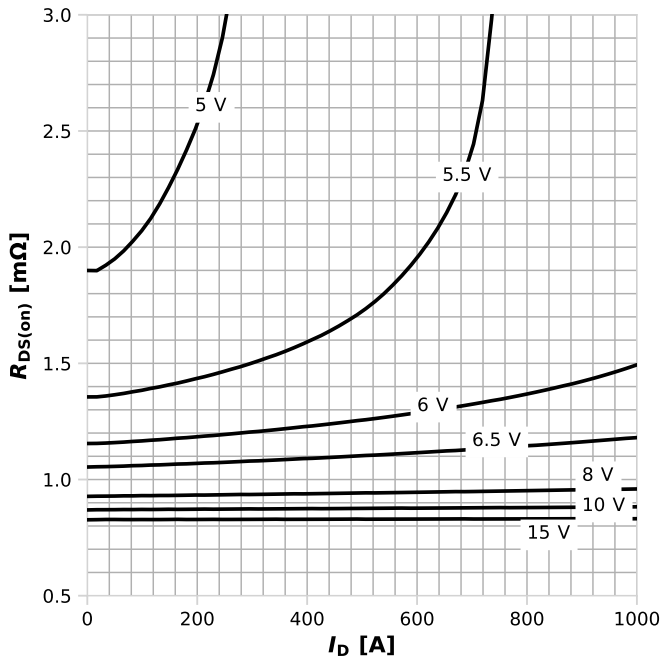
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



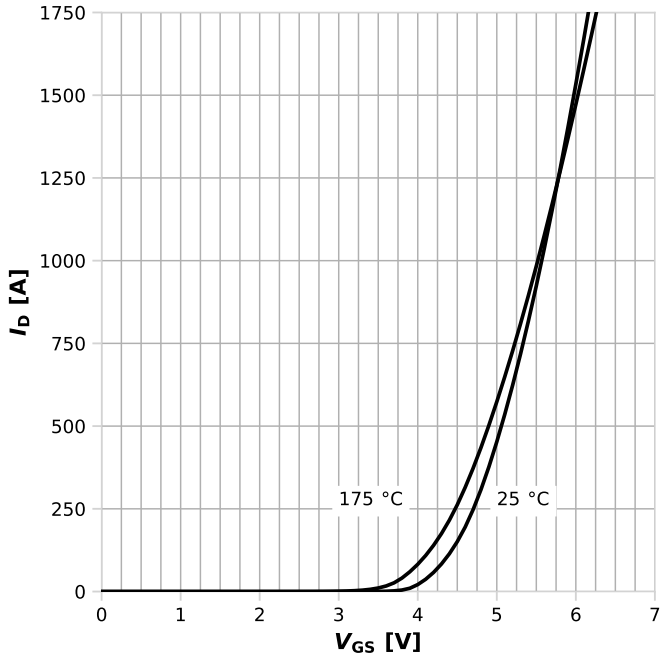
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



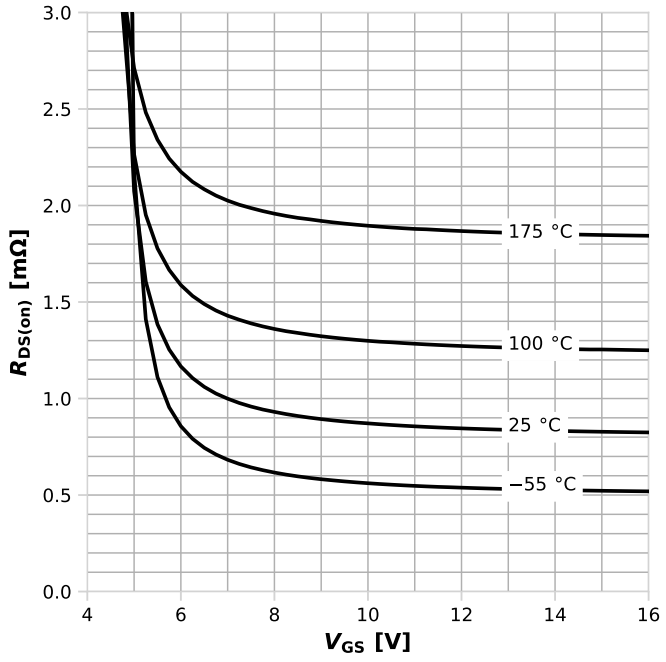
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



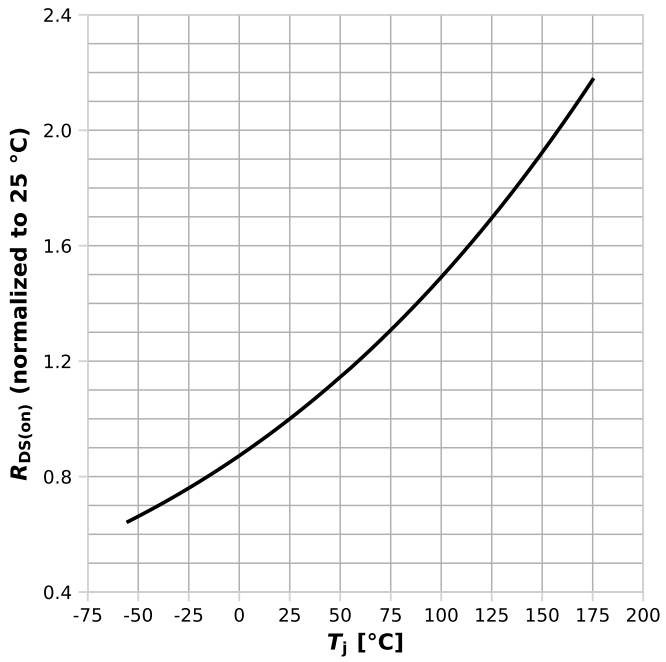
I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



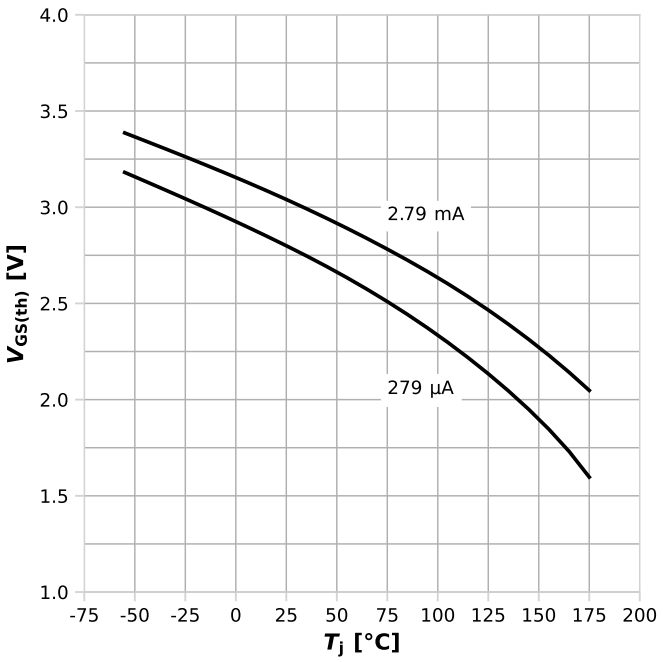
$R_{DS(on)}$=f(V_{GS}), I_D=100 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



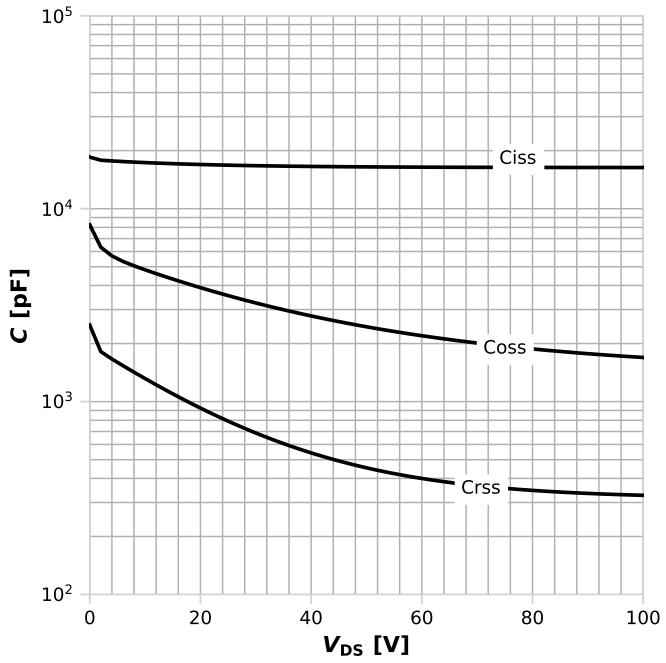
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



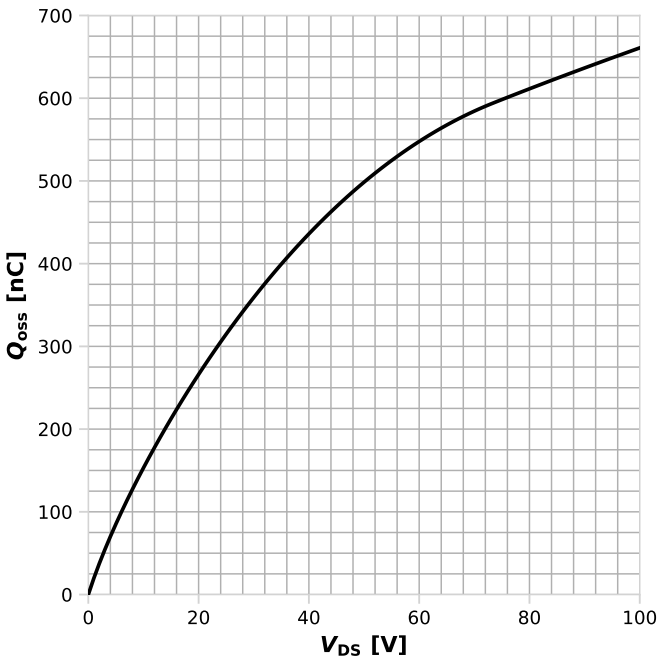
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



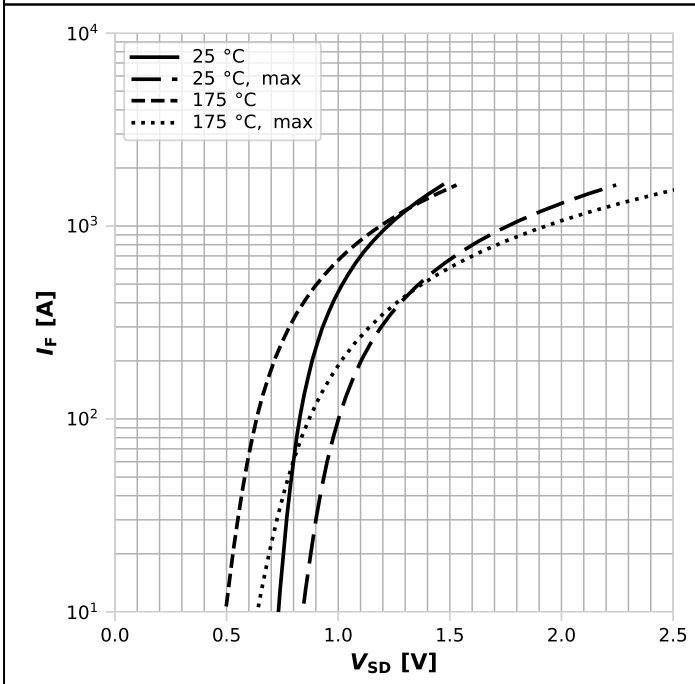
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Typ. output charge



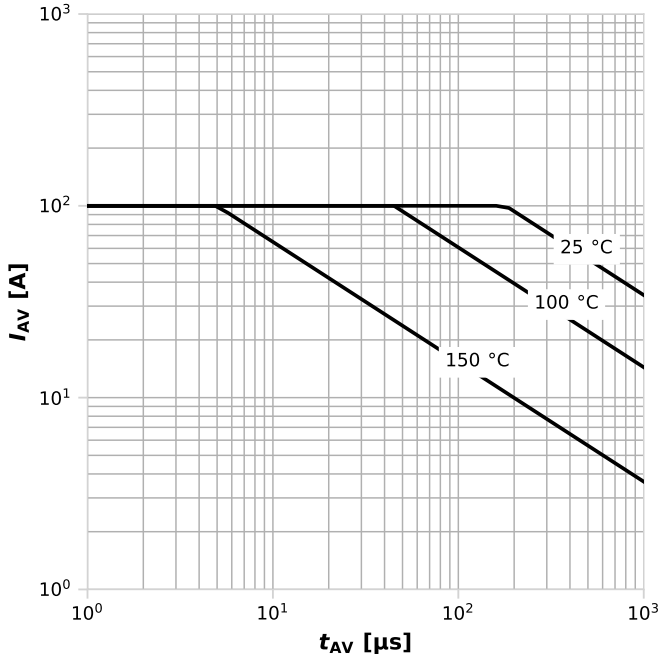
Q_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 13: Forward characteristics of reverse diode



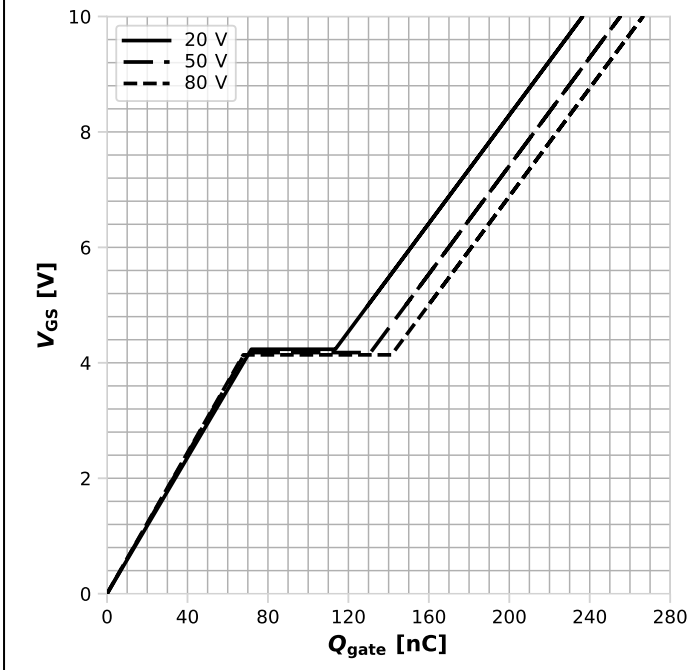
I_F=f(V_{SD}); parameter: T_j

Diagram 14: Avalanche characteristics



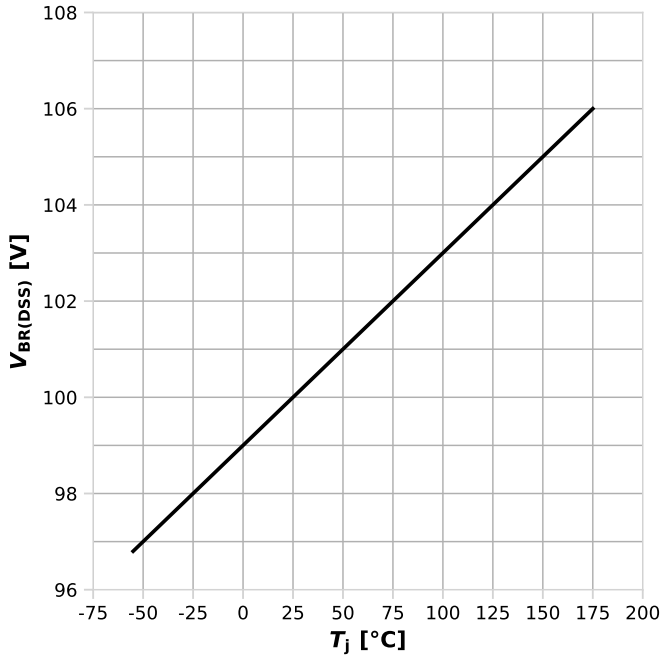
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 15: Typ. gate charge

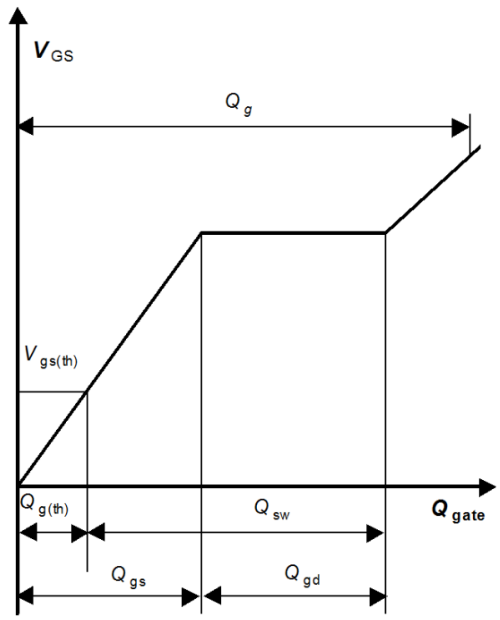


V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 16: Min. drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms

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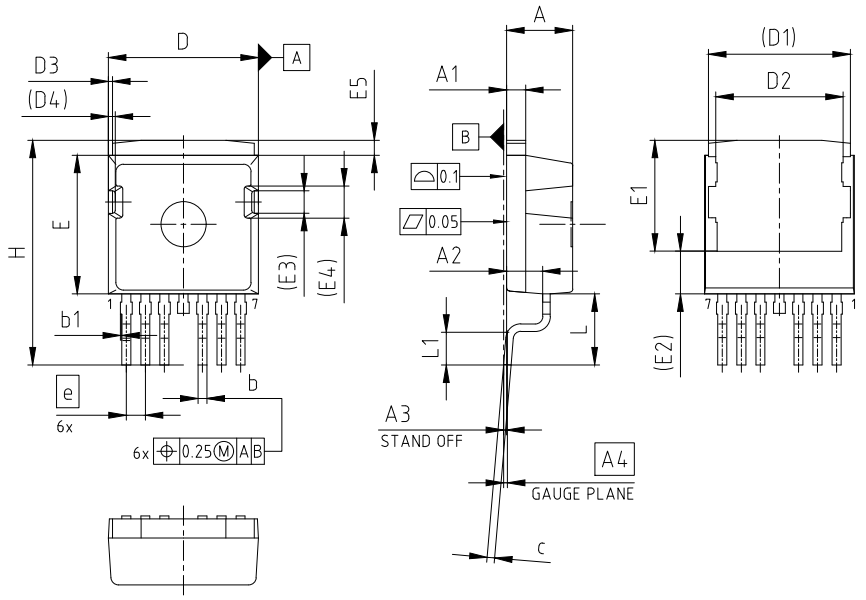
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO263-7-U06				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	4.30	4.50	E	9.05	9.45
A1	1.17	1.37	E1	7.30	7.50
A2	2.30	2.50	E2	2.85	
A3	0.00	0.20	E3	1.50	
A4	0.25		E4	2.13	
b	0.50	0.70	E5	0.70	1.30
b1	0.00	0.15	e	1.27	
c	0.40	0.60	H	14.90	15.10
D	9.80	10.20	L	4.20	5.20
D1	9.46		L1	1.90	2.10
D2	8.40	8.60	N	7	
D3	0.00	0.30			
D4	0.45				

NOTES: (1) DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
(2) N IS THE NUMBER OF LEADS

Figure 1 Outline PG-TO263-7, dimensions in mm

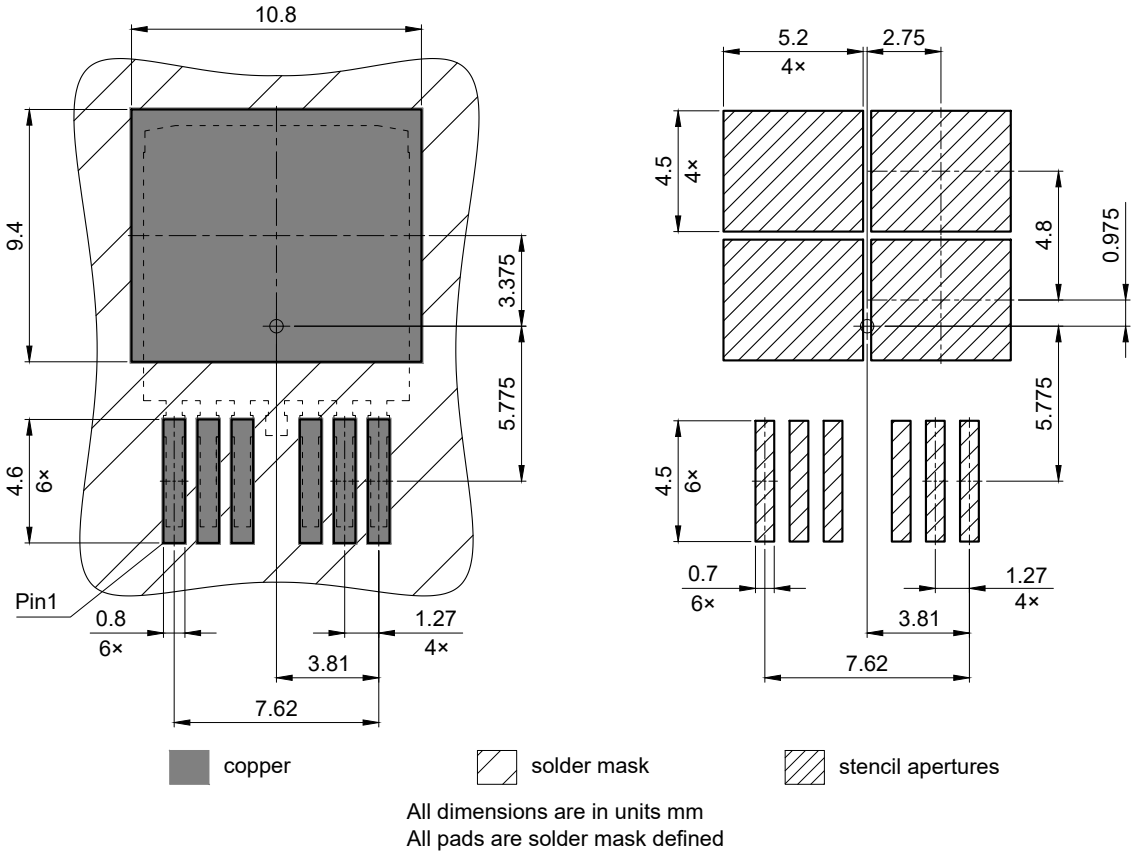


Figure 2 Footprint drawing PG-TO263-7, dimensions in mm

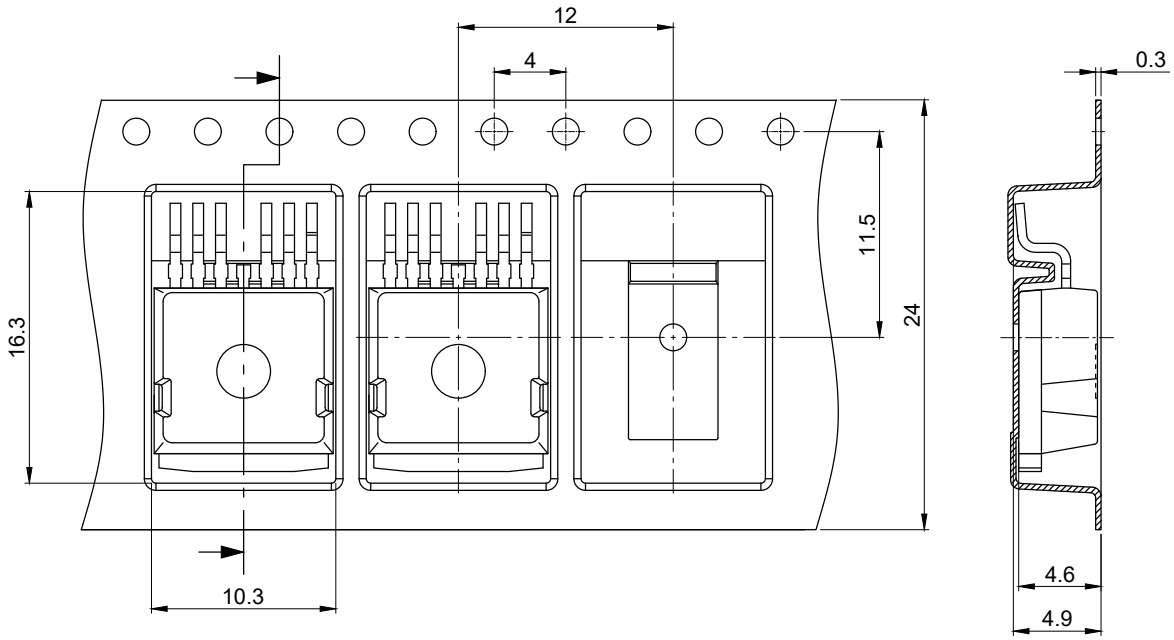


Figure 3 Packaging variant PG-TO263-7, dimensions in mm

Revision history

IPF009N10NM8

Revision 2025-12-10, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-12-10	Release of final version

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