

## MOSFET

### 650V CoolMOS™ CFD7A SJ Power Device

650V CoolMOS™ CFD7A is Infineon's latest generation of market leading automotive qualified high voltage CoolMOS™ MOSFETs. In addition to the well-known attributes of high quality and reliability required by the automotive industry, the new CoolMOS™ CFD7A series provides for an integrated fast body diode and can be used for PFC and resonant switching topologies like the ZVS phase-shift full-bridge and LLC.

### Features

- Latest 650V automotive qualified technology with integrated fast body diode on the market featuring ultra low  $Q_{rr}$
- Lowest FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- 100% avalanche tested
- Best-in-class  $R_{DS(on)}$  in SMD and THD packages

### Benefits

- Lower switching losses enabling higher switching frequencies
- High quality and reliability
- Advanced controllability due to kelvin source
- Increased efficiency in light load and full load conditions

### Potential applications

Suitable for PFC and DC-DC stages for:

- Unidirectional and bidirectional DC-DC converters,
- On-Board battery Chargers

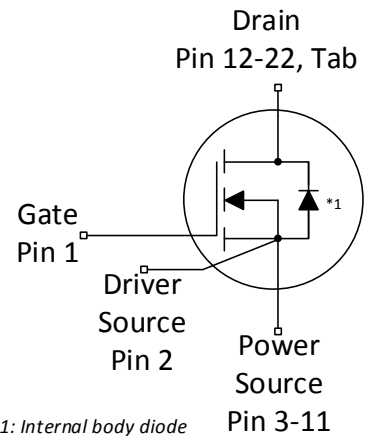
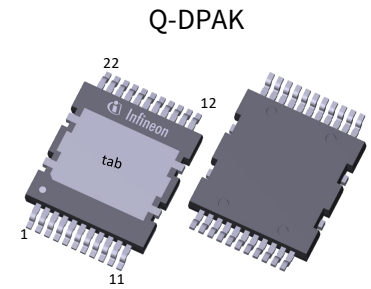
### Product validation

Qualified according to Automotive applications.  
 Product validation according to AEC-Q101.

*Please note: For production part approval process (PPAP) release we propose to share application related information during an early design phase to avoid delays in PPAP release. Please contact Infineon sales office. The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.*

**Table 1 Key performance parameters**

Parameter	Value	Unit
$V_{DS}$	650	V
$R_{DS(on),max}$	80	mΩ
$Q_{g,typ}$	50	nC
$I_{D,pulse}$	107	A
$E_{oss @ 400V}$	7.8	μJ
Body diode $di_F/dt$	1300	A/μs



Part number	Package	Marking	Related links
IPDQ65R080CFD7A	PG-HDSOP-22	65A080F7	see Appendix A



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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	36	A	$T_C=25^\circ\text{C}$
				22		$T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	107	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	125	mJ	$I_D=5.0\text{A}; V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	5.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS,pulse}$	-30	-	30	V	$f_{repetition} \leq 100\text{kHz}$ , $t_{pulse} \leq 2\text{ns}$
Power dissipation	$P_{tot}$	-	-	223	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	$I_S$	-	-	36	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	107		
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD} \leq 12.5\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	$di_F/dt$	-	-	1300	A/ $\mu\text{s}$	

1) Limited by  $T_{j,max}$ .

2) Pulse width  $t_p$  limited by  $T_{j,max}$ .

3) Identical low side and high side switch with identical  $R_G$ .

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.56	°C/W	-
Soldering temperature, reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

For applications with applied blocking voltage > 425 V, it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support by Infineon.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage <sup>4)</sup>	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=0.63mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ C$
			80	-		$V_{DS}=650V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	0.1	$\mu A$	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.068	0.080	$\Omega$	$V_{GS}=10V, I_D=12.5A, T_j=25^\circ C$
			0.15	-		$V_{GS}=10V, I_D=12.5A, T_j=150^\circ C$
Gate resistance	$R_G$	-	6	-	$\Omega$	$f=250kHz, \text{open drain}$

<sup>4)</sup> We do not recommend using the CoolMOS™ mentioned in this datasheet to operate in “linear mode”. For assessment of potential “linear mode”, please contact Infineon sales office.

**Table 5 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly. Stray inductances and coupling capacitances must be minimized. For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	2513	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	40	-		
Effective output capacitance, energy related <sup>5)</sup>	$C_{o(er)}$	-	97	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>6)</sup>	$C_{o(tr)}$	-	1022	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=12.5A, R_G=5.3\Omega; \text{see table 9}$
Rise time	$t_r$		10			
Turn-off delay time	$t_{d(off)}$		105			
Fall time	$t_f$		5			

<sup>5)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>6)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

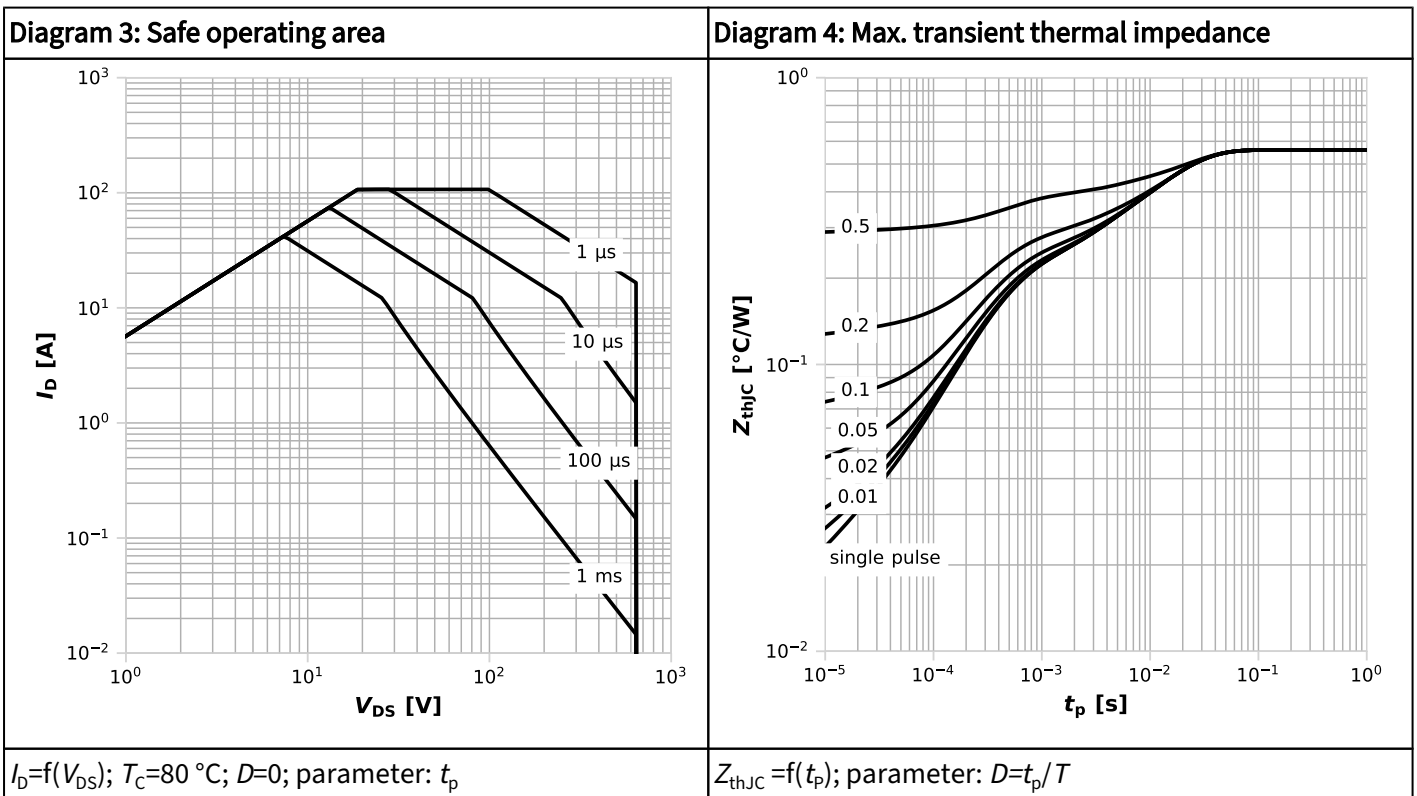
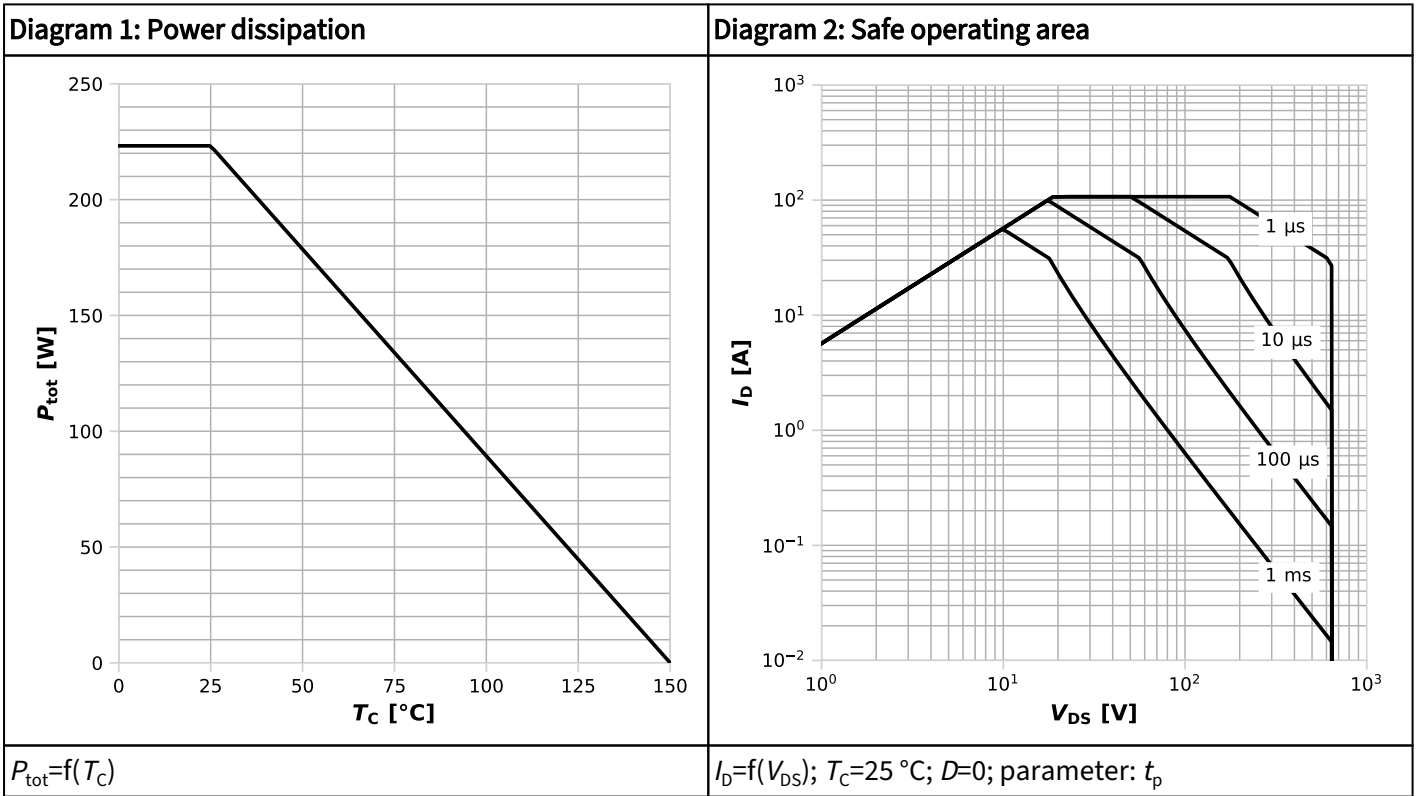
**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	14	-	nC	$V_{DD}=400V, I_D=12.5A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	15	-	nC	
Gate charge total	$Q_g$	-	50	-	nC	
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	

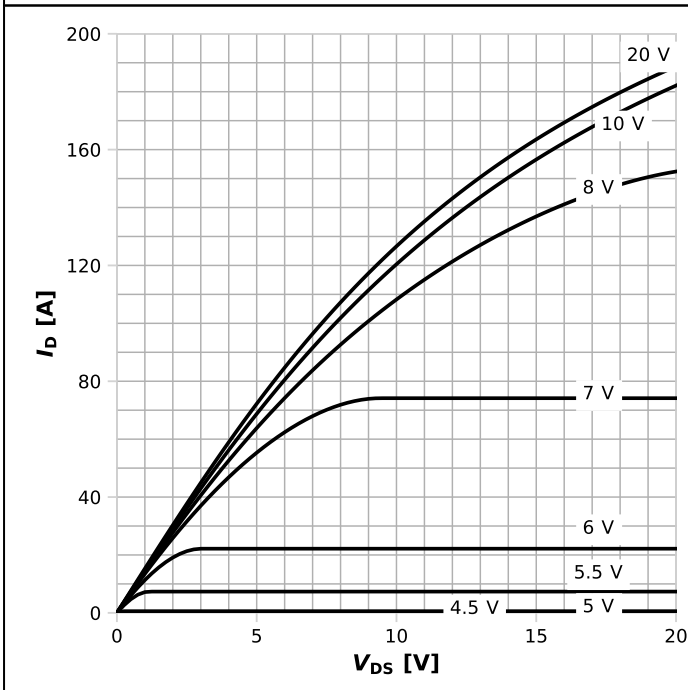
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.0	-	V	$V_{GS}=0V, I_F=12.5A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	132	-	ns	$V_R=400V, I_F=12.5A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	0.73	-	$\mu C$	
Peak reverse recovery current	$I_{rrm}$	-	9.8	-	A	

## 4 Electrical characteristics diagrams

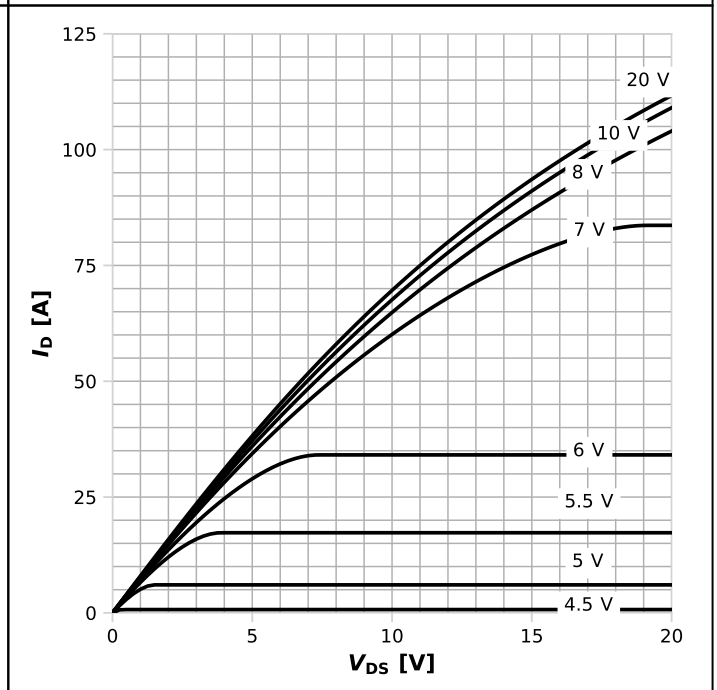


**Diagram 5: Typ. output characteristics**



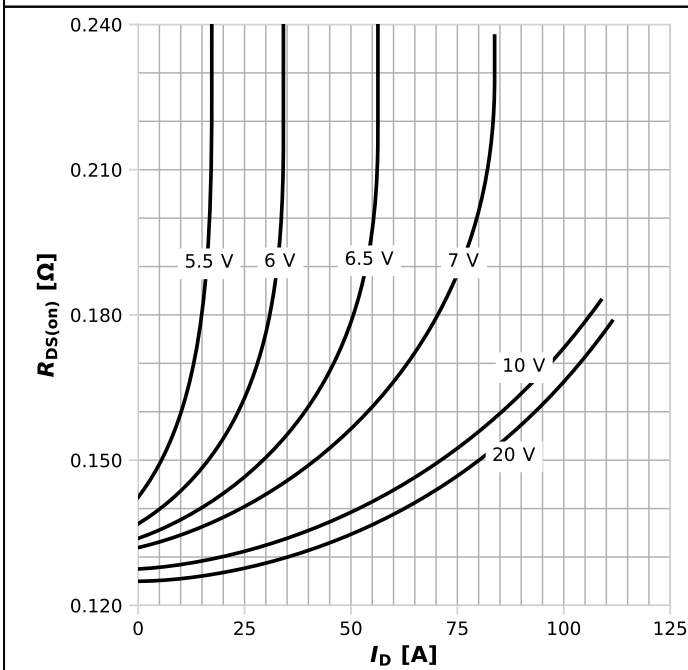
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

**Diagram 6: Typ. output characteristics**



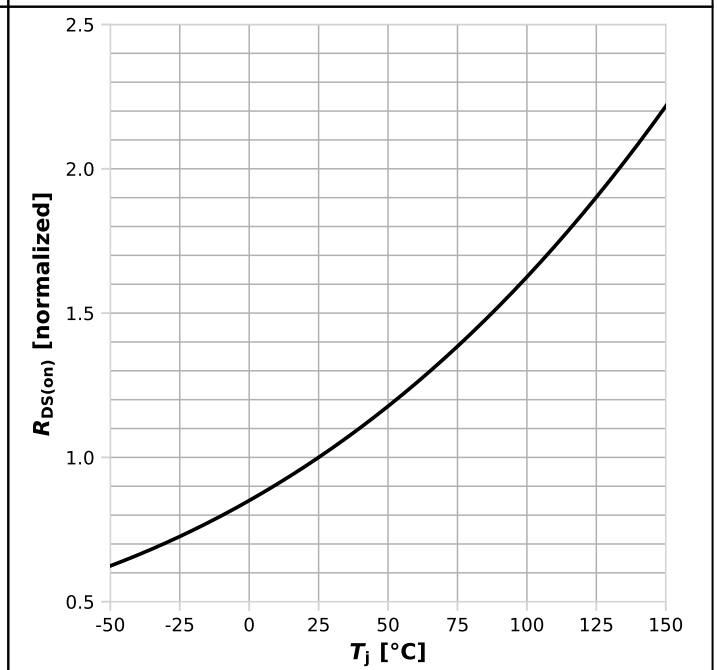
$I_D = f(V_{DS}); T_j = 125\text{ °C}; \text{parameter: } V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**

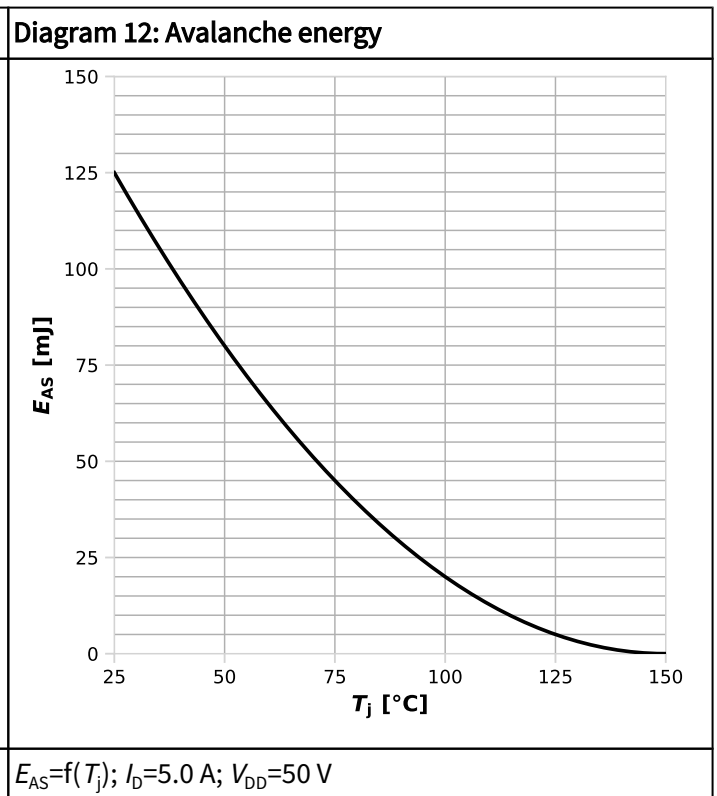
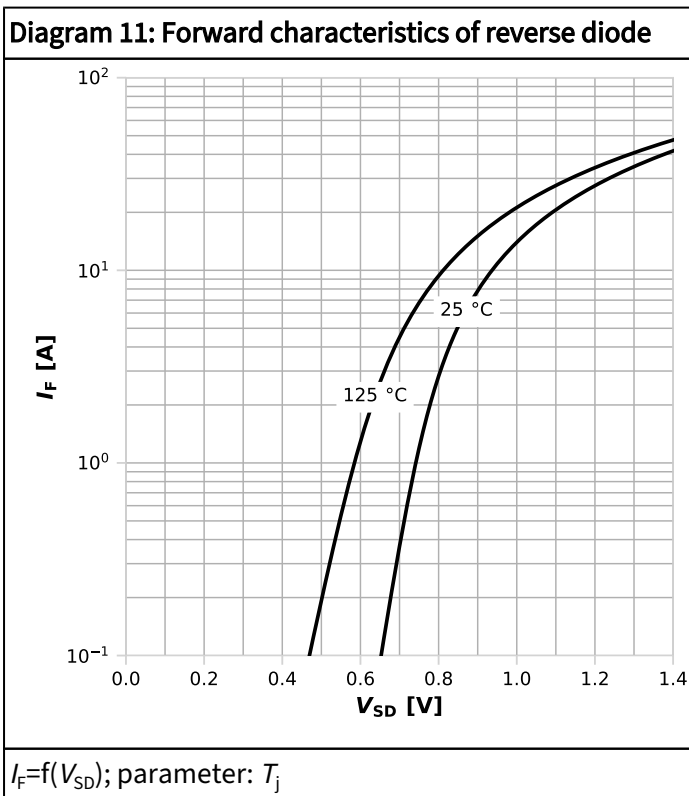
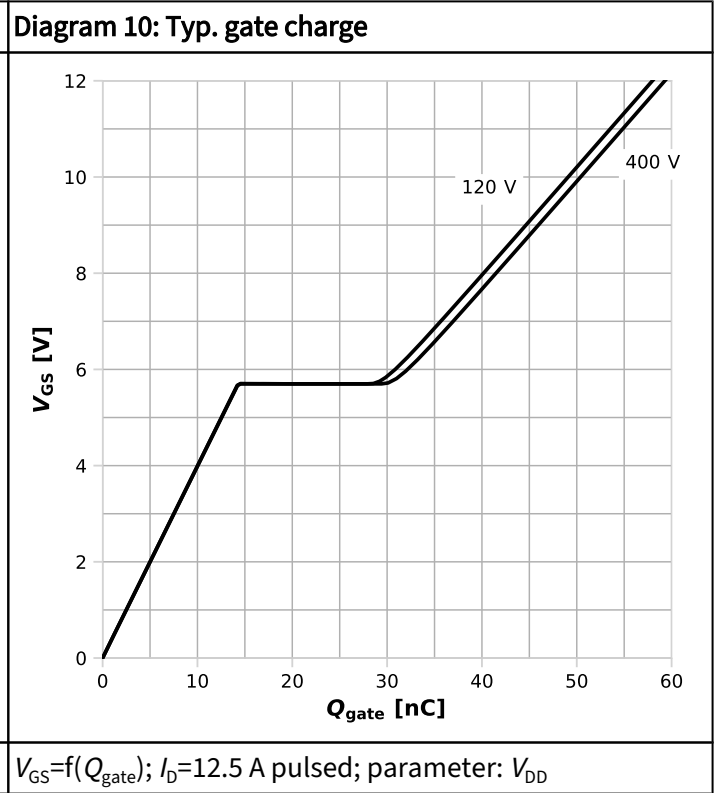
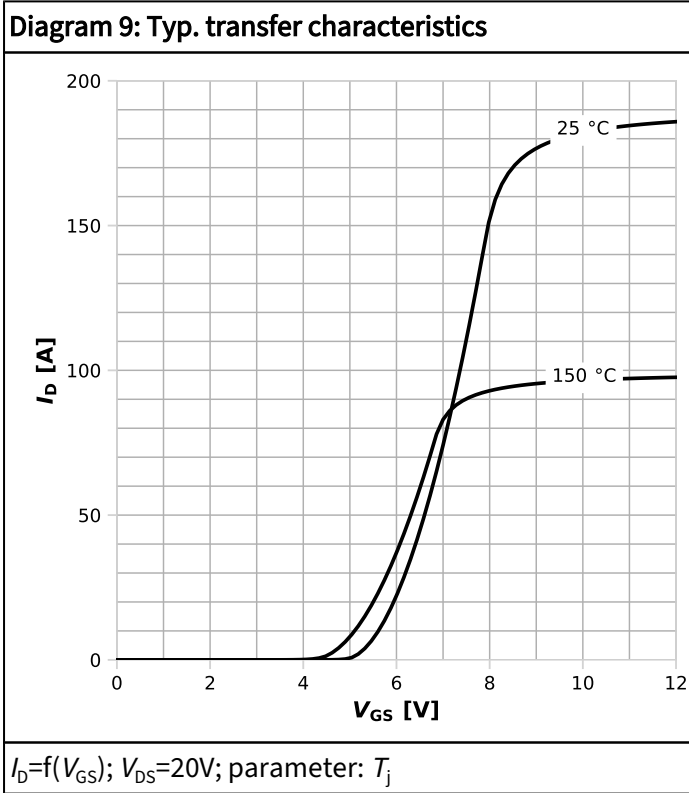


$R_{DS(on)} = f(I_D); T_j = 125\text{ °C}; \text{parameter: } V_{GS}$

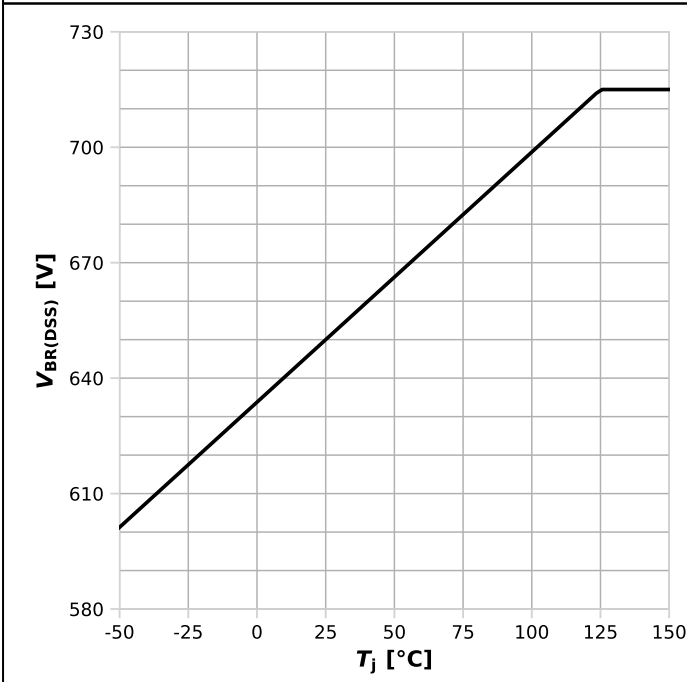
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)} = f(T_j); I_D = 12.5\text{ A}; V_{GS} = 10\text{ V}$

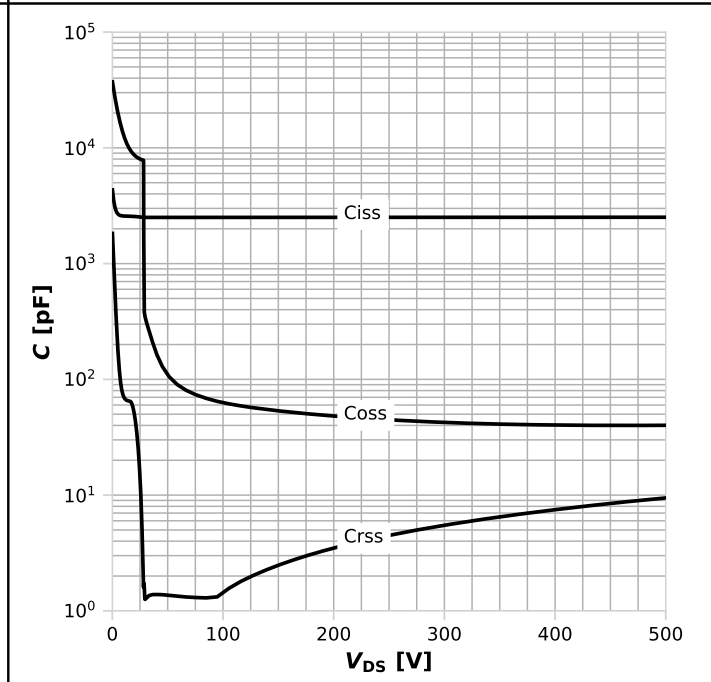


**Diagram 13: Drain-source breakdown voltage**



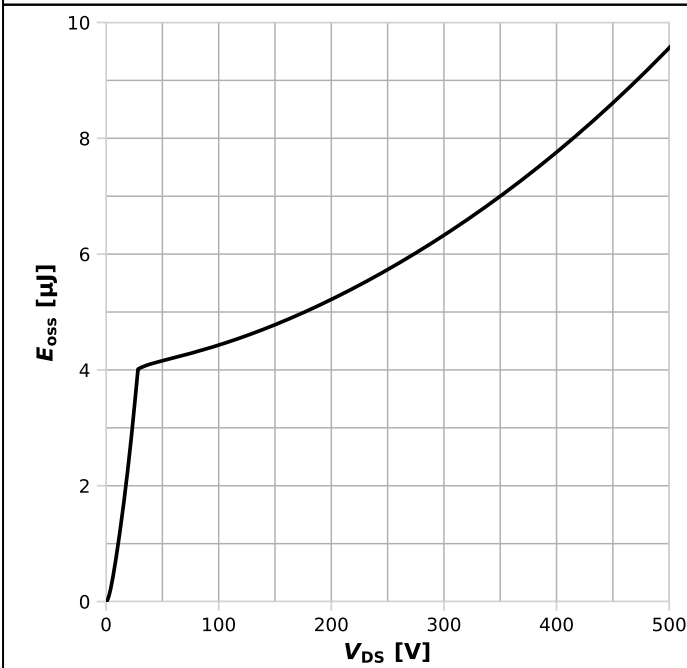
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform

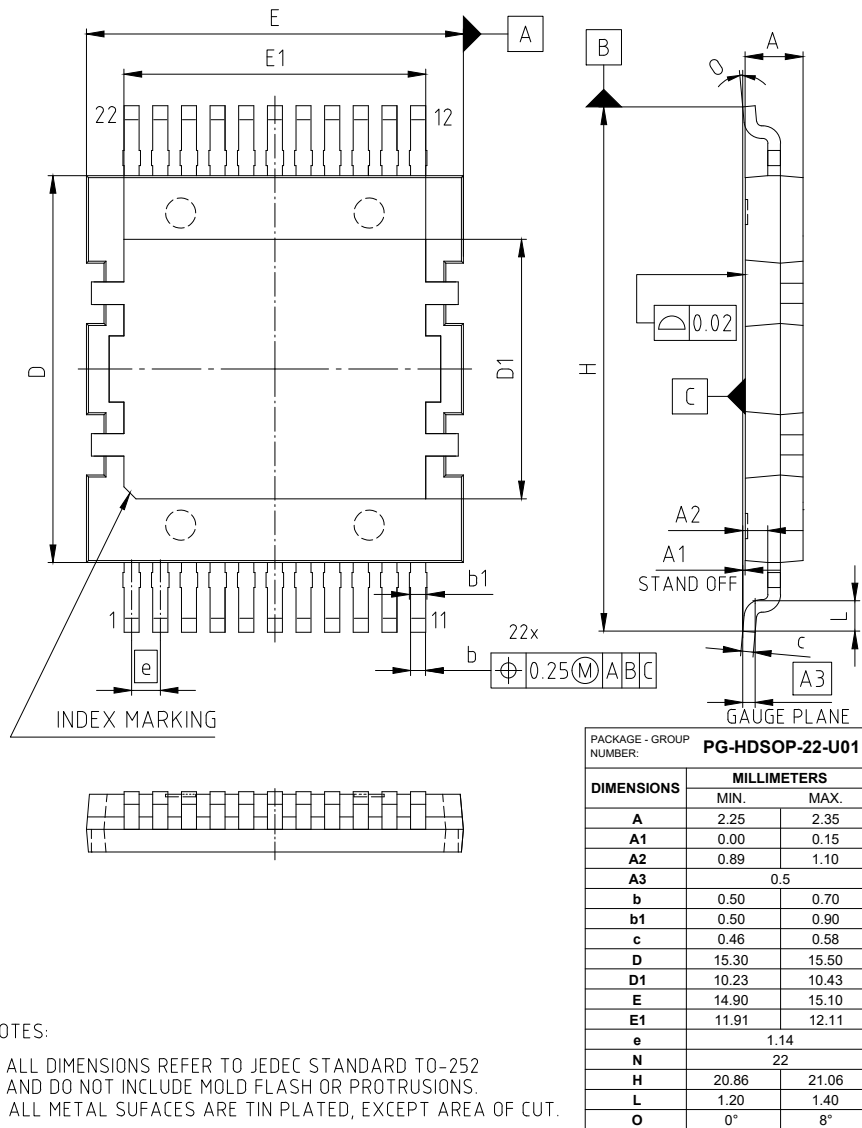
**Table 9 Switching times (ss)**

Switching times test circuit for inductive load	Switching times waveform

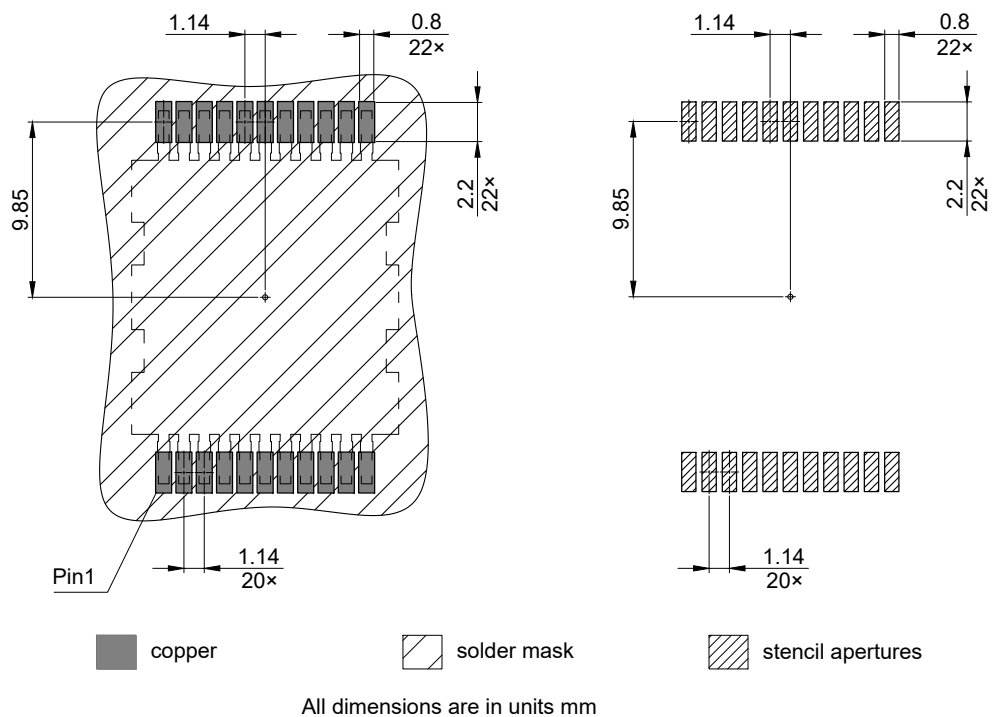
**Table 10 Unclamped inductive load (ss)**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 6 Package outlines



**Figure 1** Outline PG-HDSOP-22, dimensions in mm



**Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm**

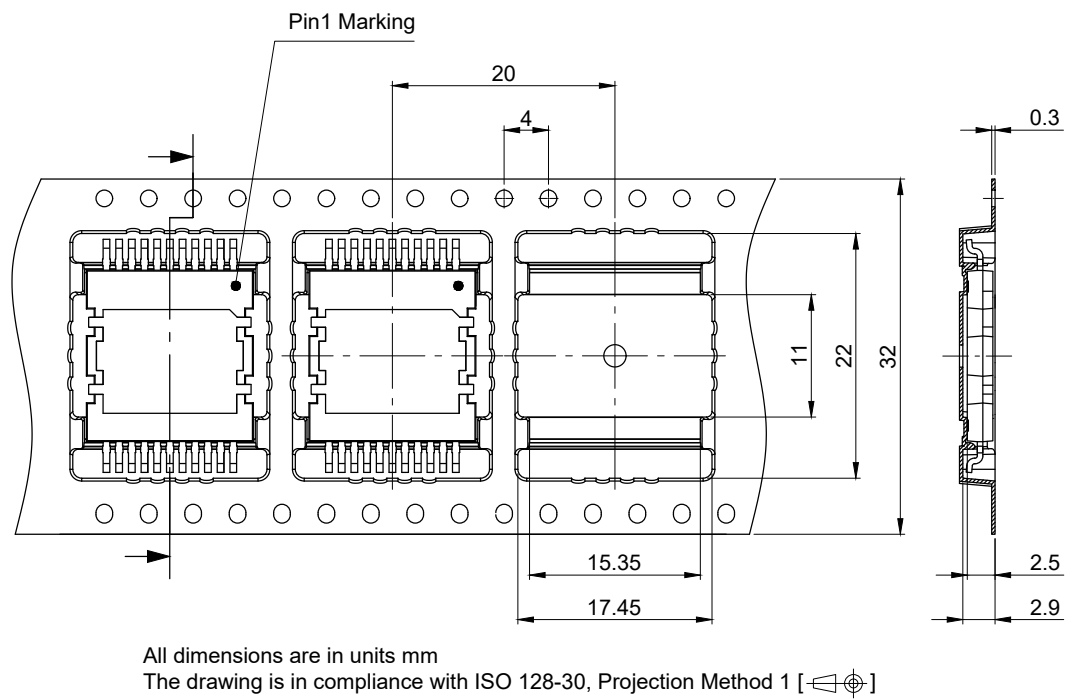


Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

## 7 Appendix A

Table 11 Related links

- [IFX CoolMOS™ CFD7A Webpage](#)
- [IFX CoolMOS™ CFD7A application note](#)
- [IFX CoolMOS™ CFD7A simulation model](#)
- [IFX Design tools](#)

**Revision history**

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IPDQ65R080CFD7A

**Revision 2026-03-01, Rev. 2.2**

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Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2022-08-30	Release of final version
2.1	2022-12-14	Updated Benefits section, Thermal characteristics parameter
2.2	2026-03-01	Implementation of standardized Infineon Umbrella-Templates for package drawings

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