OptiMOS™3 Power MOS Transistor Chip

Type	$V_{(BR)DSS}$	$R_{DS(on)}$	Die size	Thickness
IPC26N12NR	120 V	4.8 mΩ [2)]	6.0 * 4.36 mm²	250 µm

DESCRIPTION

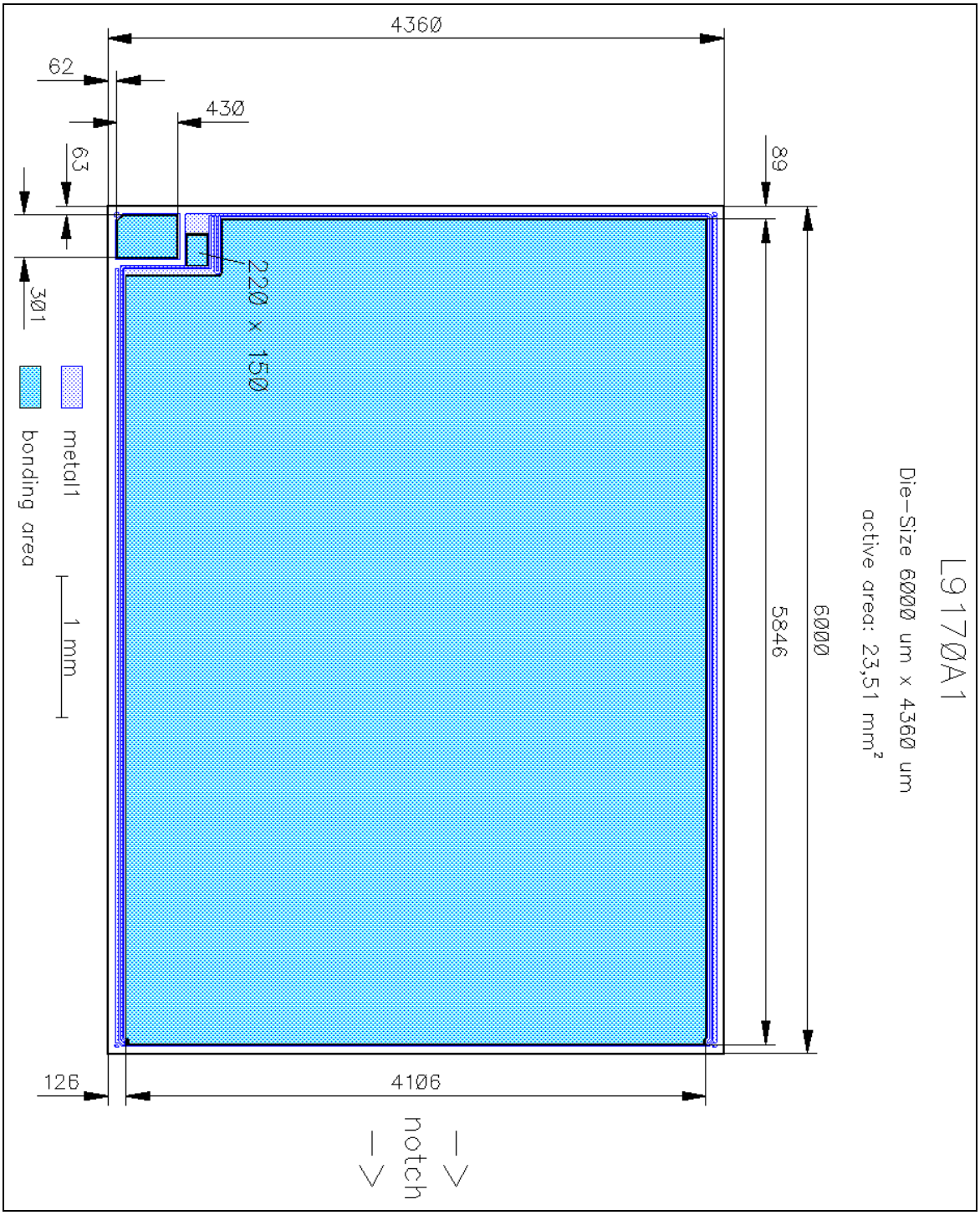
- N-channel enhancement mode
- For additional characteristic and max ratings refer to the datasheet of IPP048N12N3 G [1)]
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlSi system
- Passivation: nitride (only on edge structure)

Electrical Characteristics on Wafer Level

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Value			Unit	Conditions
		min.	typ.	max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	V_{GS} = 0V I_D = 1 mA
Gate threshold voltage	$V_{GS(th)}$	2	-	4	V	V_{DS} = V_{GS} I_D = 230 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{GS} = 0V V_{DS} = 100 V
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS} = 20 V V_{DS} = 0 V
Drain-source on-resistance	$R_{DS(on)}$	-	3.2 [4)]	100 [3)]	mΩ	V_{GS}= 10 V I_D= 2.0 A
Reverse diode forward on-voltage	V_{SD}	-	1.0	1.2	V	V_{GS}=0 V I_F= 1 A
Internal gate resistance	R_G	-	2	-	Ω	
Additional gate resistor	R_{Gadd}		16		Ω	
Avalanche energy, single pulse	E_{AS}	-	45 [5)]	-	mJ	I_D= 30 A, R_{GS}=25Ω

Chip-Layout:



[1] IPP048N12N3 G dynamic characterization does not include the internal added Rg

[2] packaged in a P-TO220-3-1 (see ref. product)

[3] limited by wafer test-equipment

[4] typical bare die $R_{DS(on)}$; V_{GS}=10V

[5] Wafer tested. For general avalanche capability refer to the datasheet of IPP048N12N3 G

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