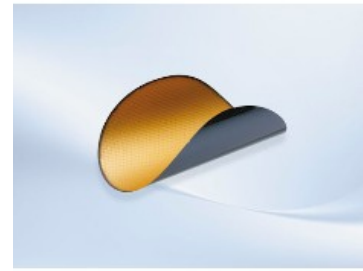


MOSFET

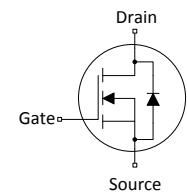
OptiMOS™3 Power MOS Transistor Chip

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPD060N03L G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride + imide

Power MOS Transistor Chip


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{(BR)DSS}$	30	V
$R_{DS(on)}$	6.0 ¹⁾	mΩ
Die size	2.26 x 1.24	mm ²
Thickness	175	μm



Type / Ordering Code	Package	Marking	Related Links
IPC028N03L3	Chip	not defined	-

1 Electrical Characteristics on Wafer Level

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1	-	2.2	V	$V_{DS}=V_{GS}$, $I_D=250\text{ μA}$
Zero gate voltage drain current	I_{DSS}	-	0.1	2	μA	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on- resistance	$R_{DS(on)}$	-	5 ²⁾	50 ³⁾	mΩ	$V_{GS}=10\text{ V}$, $I_D=2.0\text{ A}$
Reverse diode forward on-voltage	V_{SD}	-	0.86	1.1	V	$V_{GS}=0\text{ V}$, $I_F=1\text{ A}$

¹⁾ packaged in a PG-TO252-3 (see ref. product)

²⁾ typical bare die $R_{DS(on)}$; $V_{GS}=10\text{ V}$, when used with 1x500μm Al-wedge

³⁾ limited by wafer test-equipment

2 Package Outlines

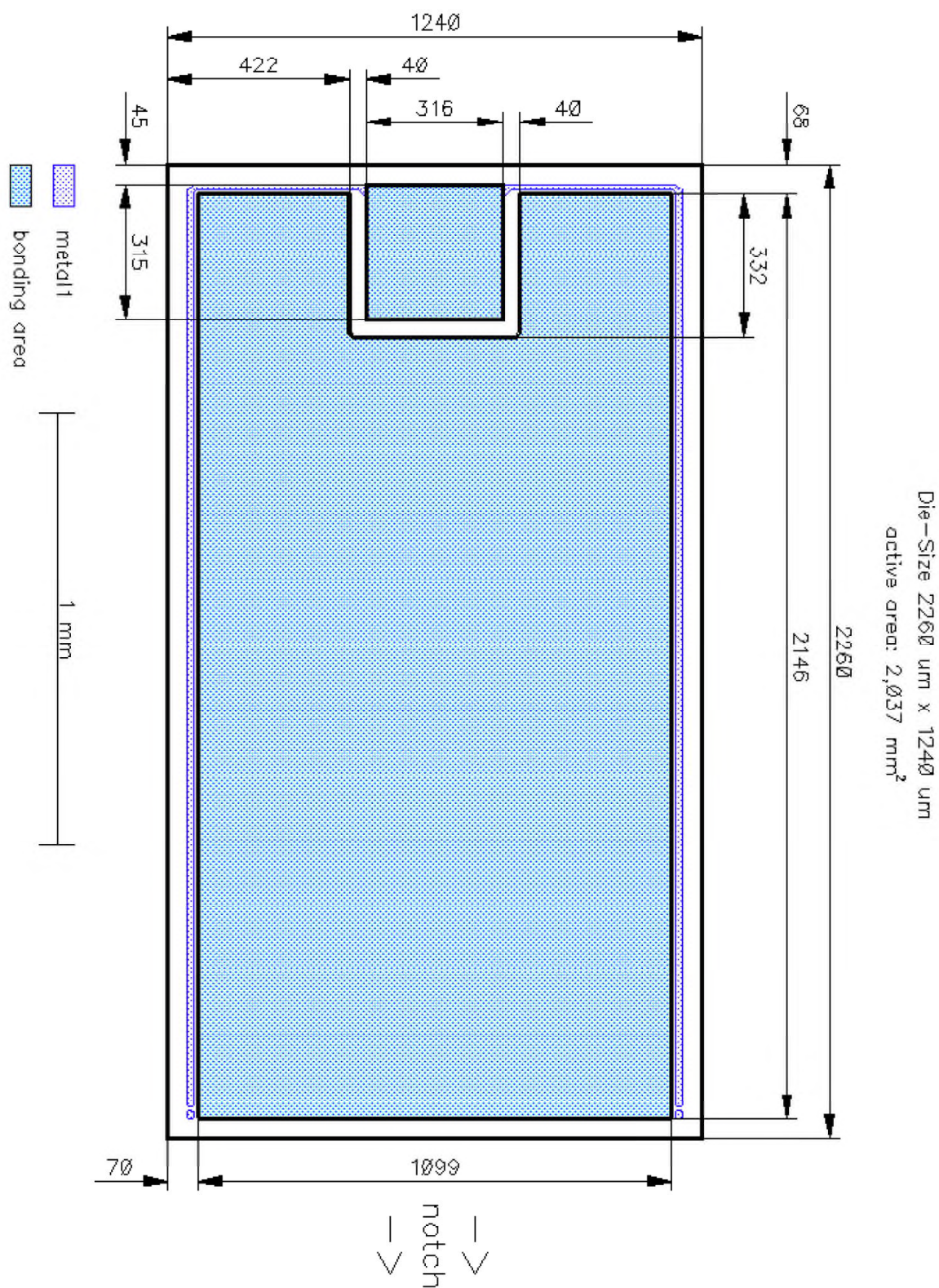


Figure 1 Outline Chip, dimensions in μm

Revision History

IPC028N03L3

Revision: 2017-08-25, Rev. 2.6

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-23	Release of Final Version
2.6	2017-08-25	Update Typ Rds(on)

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81726 München, Germany
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