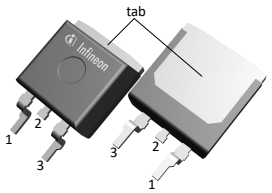
MOSFET

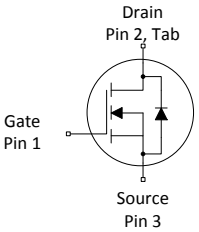
OptiMOS™ 5 Power-Transistor, 100 V

D²PAK



Features

- Ideal for high frequency switching and sync. rec.
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	2.7	mΩ
I_D	166	A
Q_{oss}	142	nC
Q_G(0V..10V)	112	nC

Hal Pb RoHS

Part number	Package	Marking	Related links
IPB027N10N5	PG-TO263-3	027N10N5	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	166	A	T_C=25 °C
				127		T_C=100 °C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	664	A	T_C=25 °C
Avalanche energy, single pulse [3]	E_{AS}	-	-	502	mJ	I_D=100 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	250	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] See Diagram 3

[3] See Diagram 13

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.4	0.6	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}		-	62		
Thermal resistance, junction - ambient, 6 cm^2 cooling area [4]	R_{thJA}		-	40		
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL1

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=184 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4	2.7	mΩ	V_{GS}=10 V, I_D=100 A
			2.8	3.5		V_{GS}=6 V, I_D=50 A
Gate resistance [5]	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	102	204	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A

[5] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	7920	10300	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [6]	C_{oss}		1210	1570		
Reverse transfer capacitance [6]	C_{rss}		53	93		
Turn-on delay time	$t_{d(on)}$	-	26	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		15			
Turn-off delay time	$t_{d(off)}$		52			
Fall time	t_f		17			

[6] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	37	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge [8)]	Q_{gd}		23	34	nC	
Switching charge	Q_{sw}		36	-	nC	
Gate charge total [8)]	Q_g		112	139	nC	
Gate plateau voltage	$V_{plateau}$		4.6	-	V	
Output charge [8)]	Q_{oss}	-	142	189	nC	V_{DD}=50 V, V_{GS}=0 V

7) See "Gate charge waveforms" for parameter definition

8) Defined by design. Not subject to production test.

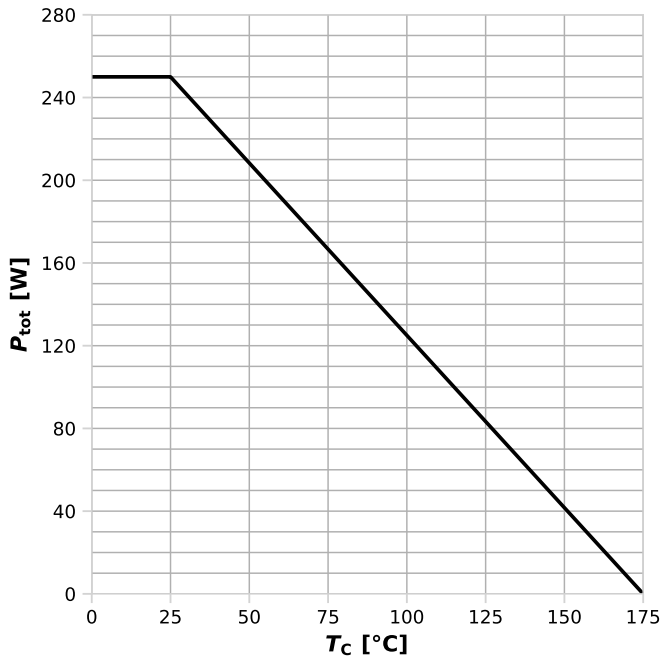
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	148	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			664		
Diode forward voltage	V_{SD}	-	0.92	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	74	148	ns	V_R=50 V, I_F=100, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}		166	332	nC	

9) Defined by design. Not subject to production test.

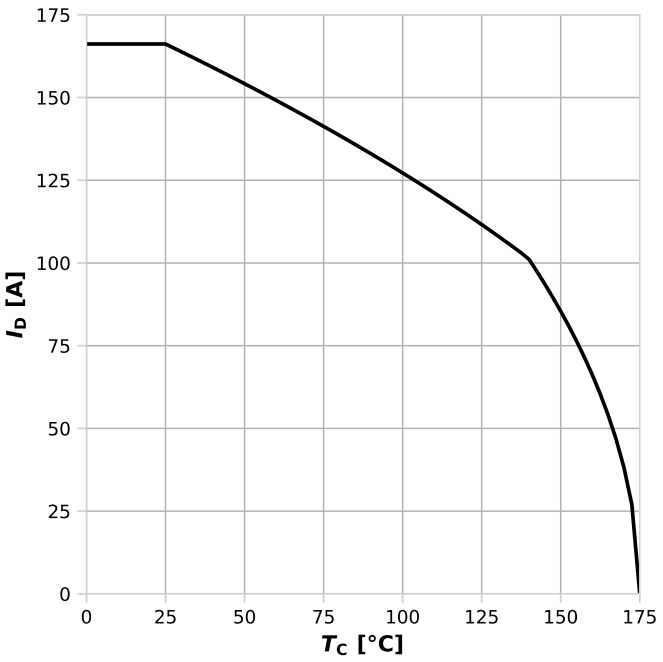
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



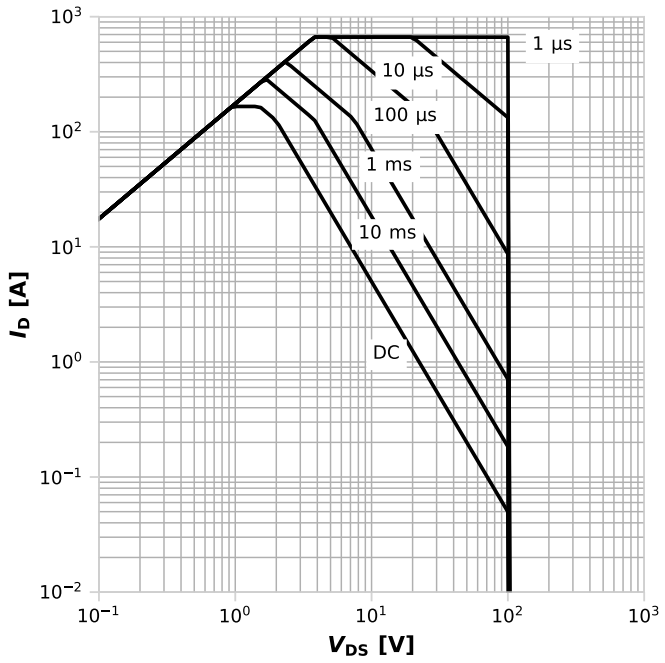
P_{tot}=f(T_C)

Diagram 2: Drain current



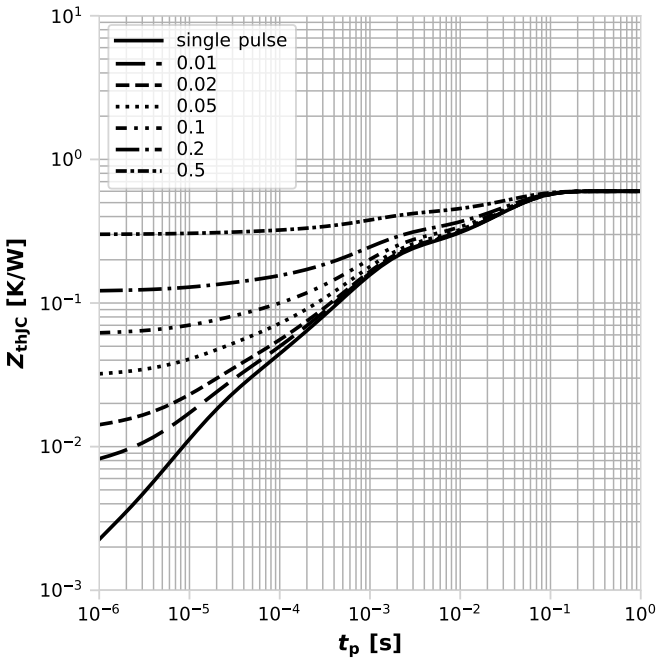
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



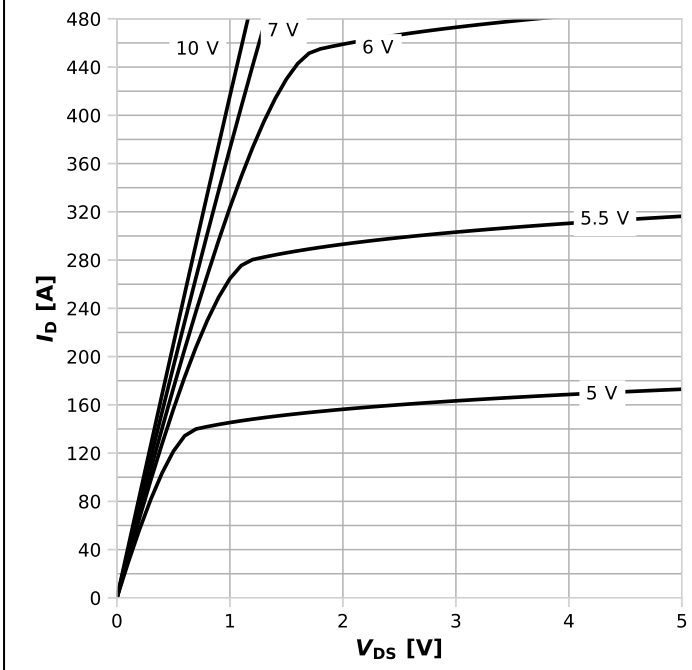
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



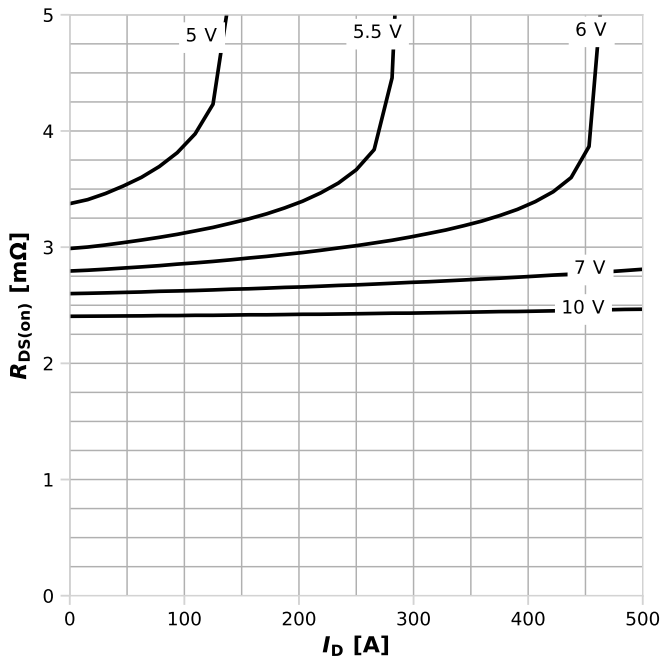
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



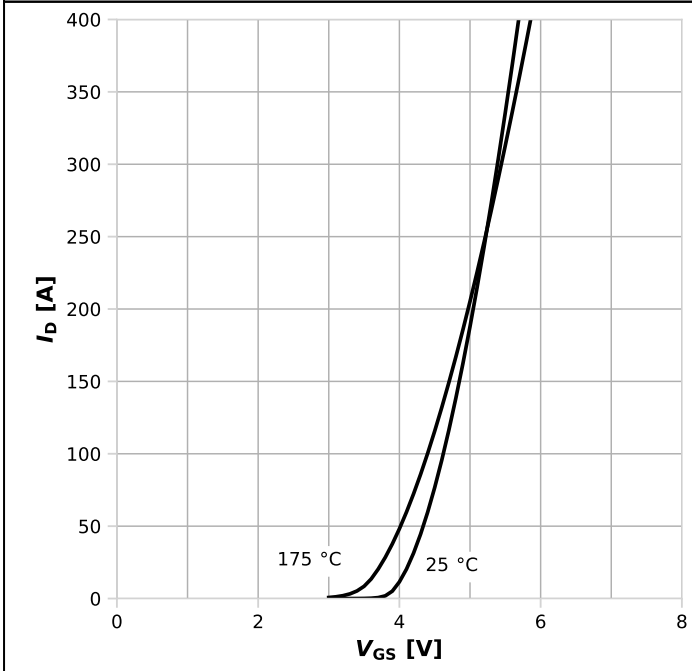
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



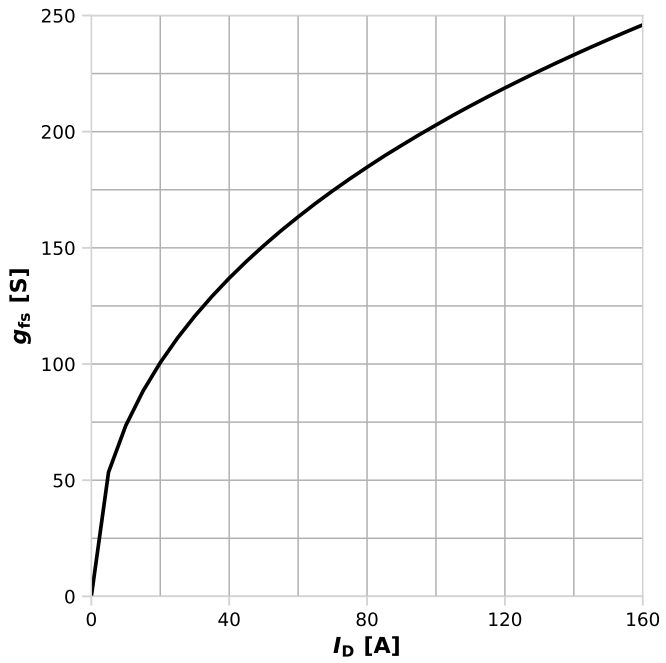
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



g_{fs}=f(I_D); T_j=25 °C

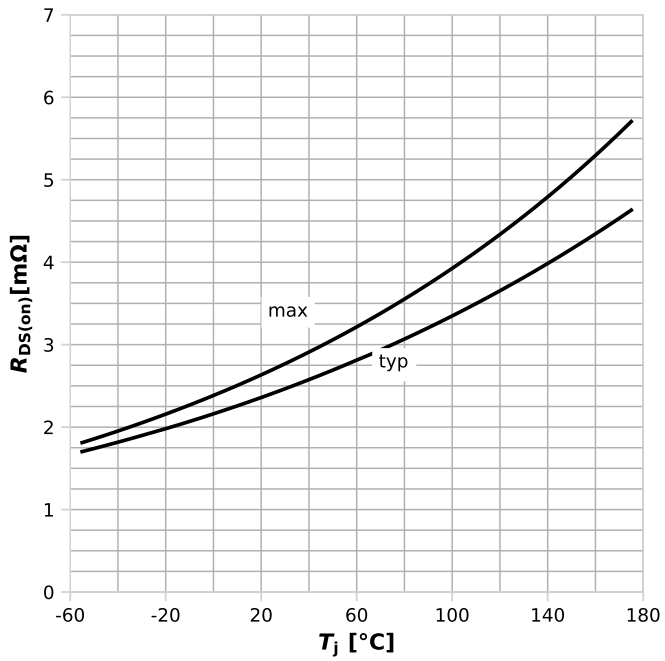
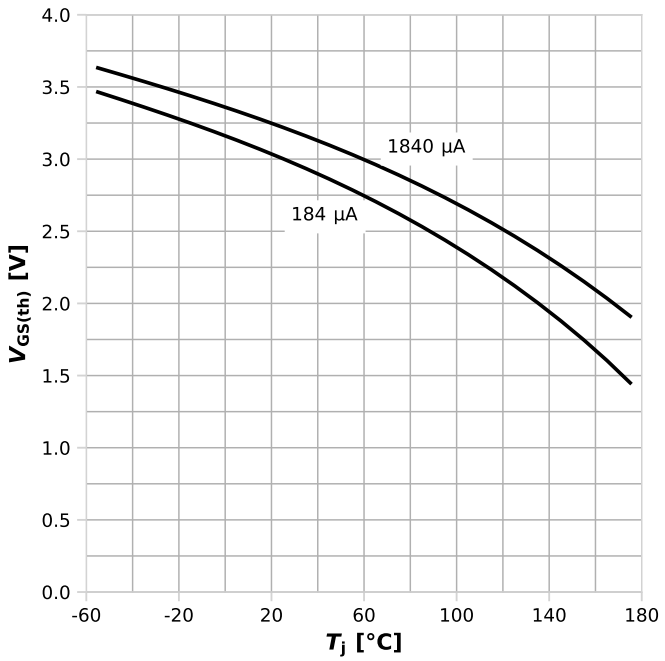
Diagram 9: Drain-source on-state resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=100 A; V_{GS}=10 V	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D

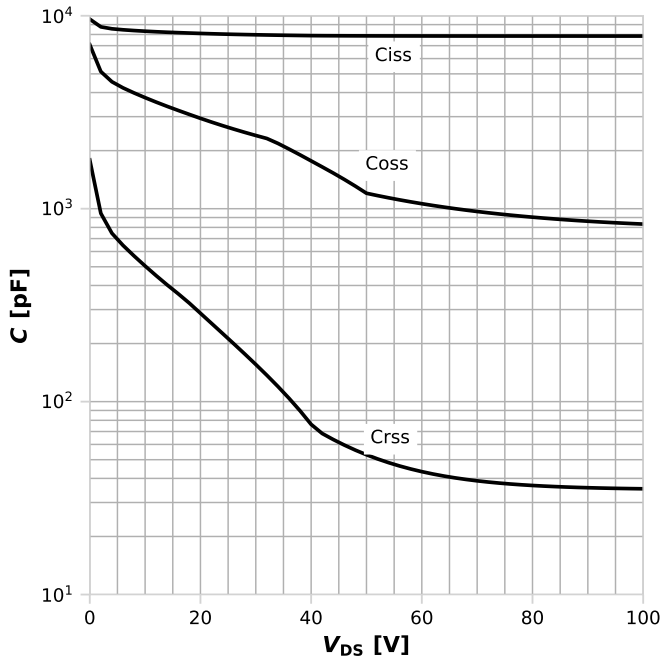
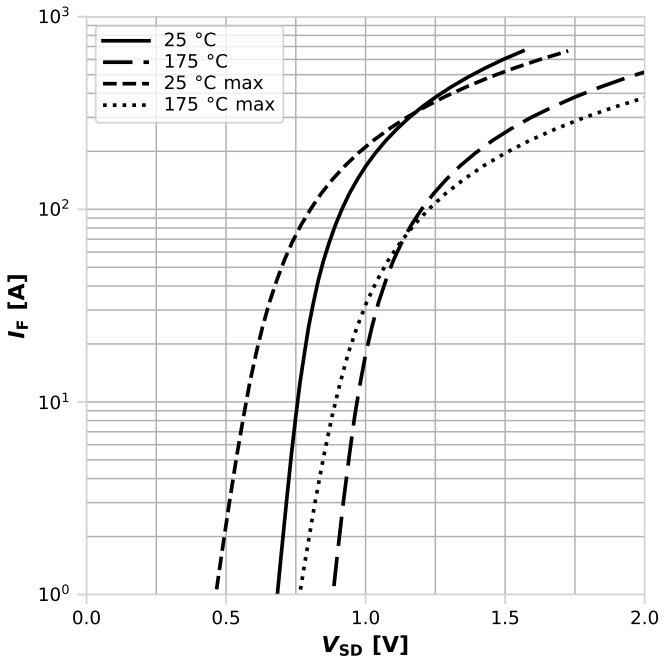
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

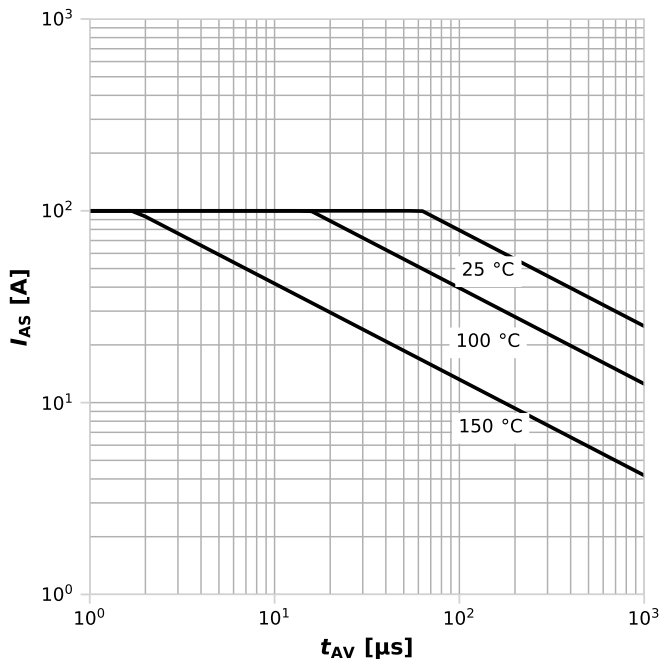
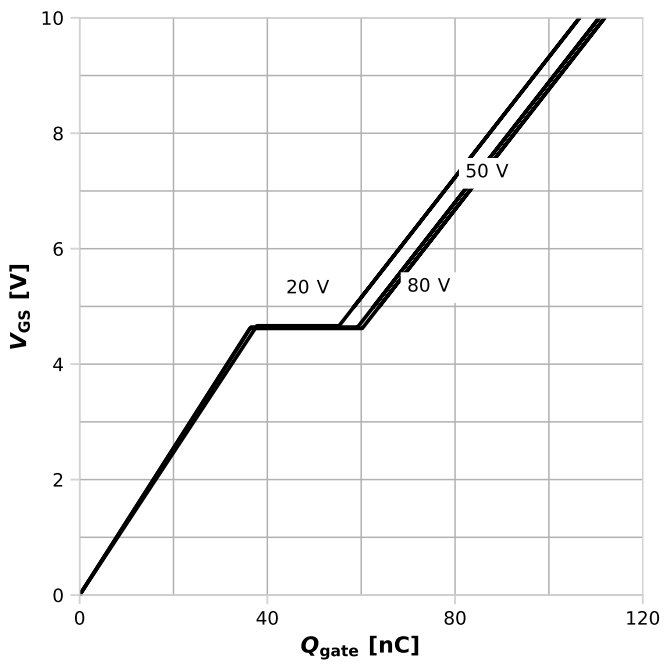
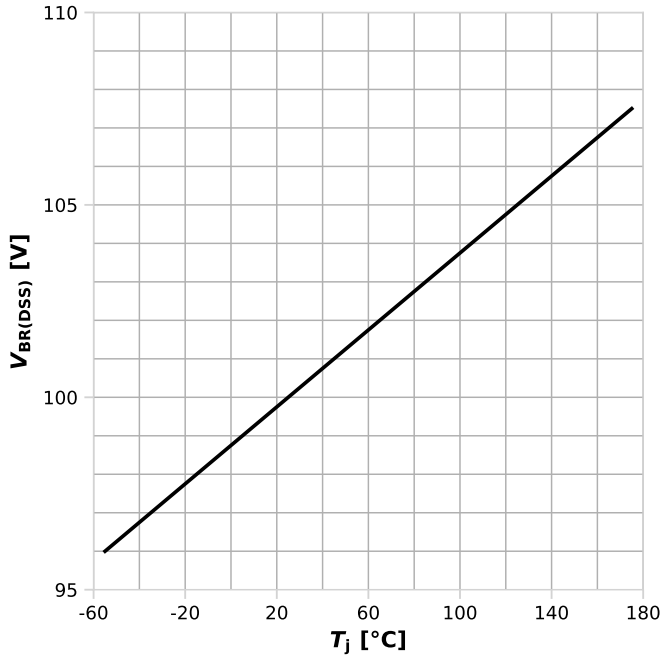
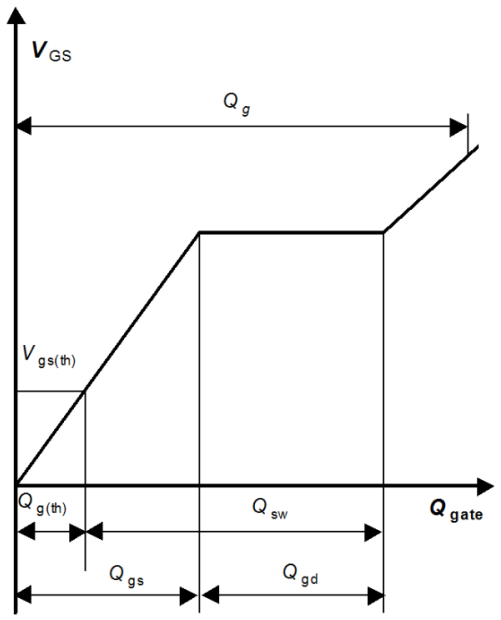
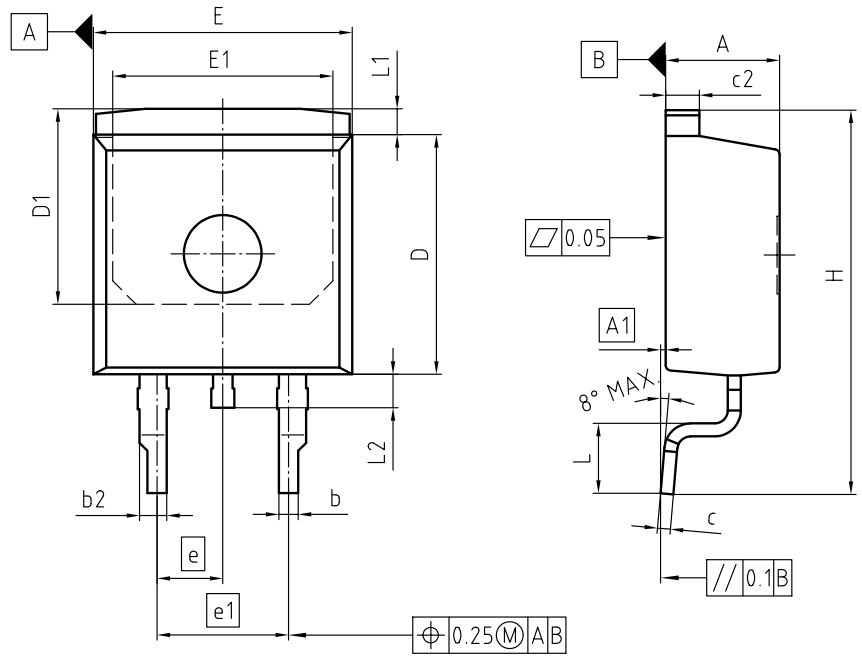
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=100 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO263-3-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.10
b	0.65	0.85
b2	0.95	1.15
c	0.40	0.60
c2	1.17	1.37
D	9.05	9.45
D1	7.45	7.65
E	9.80	10.20
E1	8.40	8.60
e	2.54	
e1	5.08	
N	2	
H	14.60	15.90
L	2.40	3.00
L1	0.70	1.30
L2	1.00	1.60

Figure 1 Outline PG-TO263-3, dimensions in mm

Revision history

IPB027N10N5

Revision 2025-09-22, Rev. 2.5

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-17	Release of final version
2.1	2015-01-30	Reduce active area by 0.7%
2.2	2016-07-20	Update SOA Diagram
2.3	2016-10-03	Update Avalanche Energy
2.4	2017-07-11	Update product current
2.5	2025-09-22	Update IDSS 100V max limit and IGSS typ

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