RIC70115 - Rad hard high/low side gate driver for GaN HEMT and LL Si FET

Features

- Truly differential input enhances immunity to noise on input and enables both high and low side operation
- Integrated linear regulator provides regulated optimal gate drive voltage for GaN HEMT and logic level (LL) Si FET while supporting wide bias voltage range
- Short propagation delay enables high switching frequency
- Integrated miller clamp improves robustness against undesired induced turn-on
- Target radiation tolerance
  - High dose rate (50-300 rad(Si)/s) of 100 krad(Si), characterized to 150 krad(Si)
- Target Single event effect (SEE) hardness
  - No SEB or SEL up to LET of 81.9 MeV·cm^2/mg
  - SET characterized up to LET of 81.9 MeV·cm^2/mg
- Planned to be electrically screened and qualified to MIL-PRF-38535, Class V

Product summary

- V_{DD} = 17.1 V (abs max)
- V_{DRV} = 4.8 V
- $I_{SRC/SNK}$ = 1.5 A / 2.5 A
- T_A = -55°C to 125°C

16 pin LCC

Potential applications

- Satellite Bus and Payload
- Power Conditioning Unit
- Power Distribution Unit
- DC-DC Converter

Ordering information

Table 1 Ordering information

Orderable part number	Package type	Device level	Total ionizing dose level
5962R2420701VXA	16-pin LCC	Level V[1, 3]	100 krad(Si)
RIC70115	16-pin LCC	COTS[2]	
RIC70115EVAL1	Evaluation board		

[1] Per MIL-PRF-38535

[2] Intended for engineering evaluation only, devices are only electrically tested at 25°C and for hermeticity

[3] MIL-PRF-38535 QMLV certification pending

Description

RIC70115 is a radiation hardened gate driver. It is intended for harsh radiation environments such as space, with electrical parameters specified pre and post-irradiation up to 100 krad(Si) and single event effects (SEE) characterized up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg. RIC70115 is available in a hermetically sealed 16 pin CLCC package and operates over the full military ambient temperature range of -55°C to 125°C.

RIC70115 is intended for use with rad hard GaN Schottky gate (SG) HEMT or rad hard logic level gate drive FET. It features high gate drive strength and fast propagation delay to enable high frequency, low loss switching. It integrates an optional LDO, which allows a wide bias supply to be used while providing an ideal and tightly regulated drive voltage. It additionally includes a miller clamp, which helps to prevent against induced turn on from high slew rates on the drain of the power switch.

RIC70115 features truly differential input (TDI) logic, which improves robustness against noise on the input pins as well as enable support for high side operation.

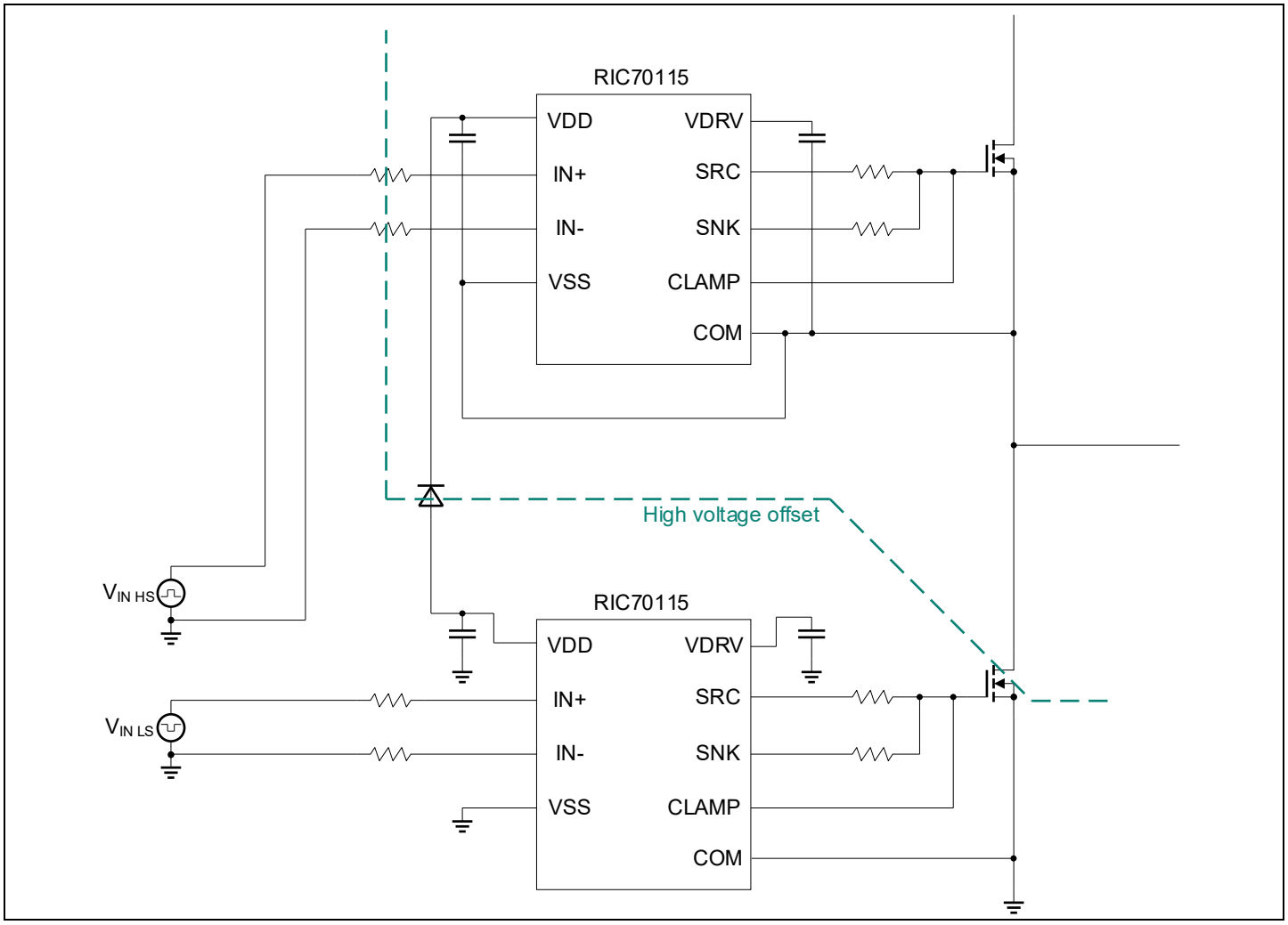

Figure 1 Typical half bridge application block diagram

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1 Block diagram

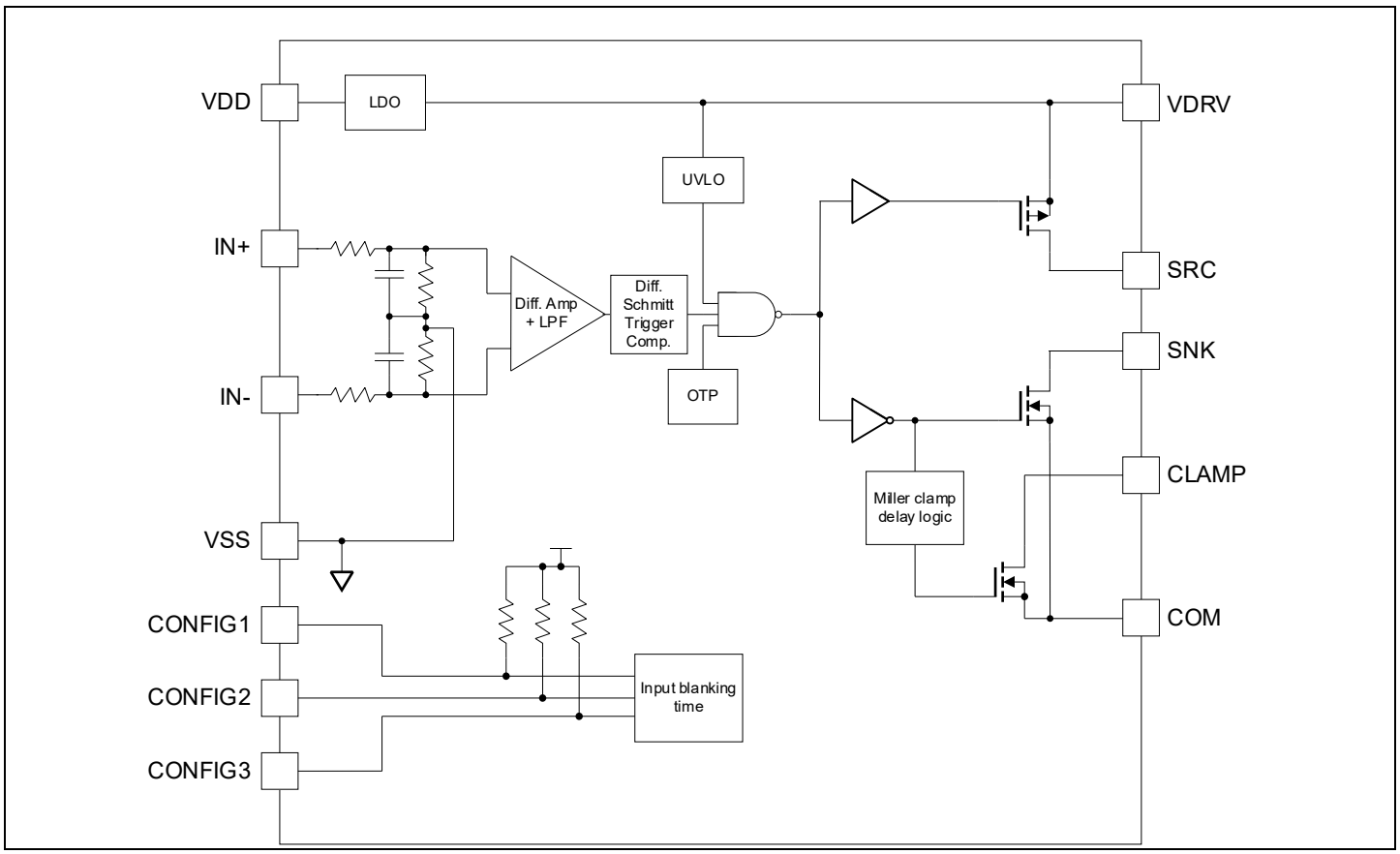
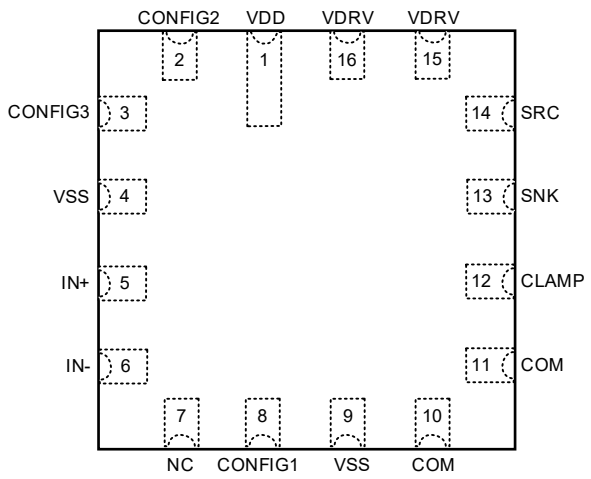


Figure 2 Block diagram

2 Pin configuration and functionality

2.1 Pin configuration



16 pin LCC

Figure 3 RIC70115 pin assignments (top view)

2.2 Pin functionality

Table 2 Pin functionality

Pin	Symbol	Description
1	VDD	Bias power input for internal LDO
2	CONFIG2	Configuration pin. Pin has internal pull up resistor. Leave open or connect to VSS to program input blanking time
3	CONFIG3	Configuration pin. Pin has internal pull up resistor. Leave open or connect to VSS to program input blanking time
4, 9	VSS	Return. Connect to ground.
5	IN+	Positive input
6	IN-	Negative input
7	NC	No connection. Leave pin disconnected (pin is internally electrically connected)
8	CONFIG1	Configuration pin. Pin has internal pull up resistor. Leave open or connect to VSS to program input blanking time
10, 11	COM	Return for output drive stage. Connect to VSS for 0 V turn off or apply negative voltage for negative voltage turn off
12	CLAMP	Miller clamp, connect to gate of GaN HEMT / Si FET
13	SNK	Negative output of gate driver, sinks current
14	SRC	Positive output of gate driver, sources current
15, 16	VDRV	4.8 V output of internal LDO, voltage used for drive. It is required to connect an external capacitor of at least 2 µF from VDRV to VSS. Bias power can be directly applied to this pin to bypass internal LDO.

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to VSS unless otherwise stated in the table.

Table 3 Absolute maximum ratings

Symbol	Definition	Min	Max	Units
V_{DD}	VDD pin to COM	-0.3	17.1	V
	VDD pin to VSS	-0.3	17.1	V
V_{DRV}	VDRV pin	-0.3	6.5	V
V_{IN}	IN+, IN- pins	-6.5	0.3	V
V_{OUT}	SRC, SNK and CLAMP pins to COM	-5		V
	SRC, SNK and CLAMP pins to VSS	-0.3	VDRV+0.3	V
COM	COM to VSS	-5	0.3	V
T_J	Operating junction temperature	-55	150	°C
T_S	Storage temperature	-65	150	°C
T_L	Lead temp (soldering, 10s, 0.063 in (1.6 mm) from case)		300	°C

3.2 ESD ratings

Table 4 ESD ratings

Symbol	Definition	Value	Units
V_{ESDHBM}	ESD Human Body Model (HBM), Class 3A per MIL-STD-883, Method 3015[1]	4	kV
V_{ESDCDM}	ESD Charged device model (CDM)[2]	1	kV

[1] Per ANSI/ESDA/ JEDEC JS-001

[2] Per ANSI/ESDA/JEDEC JS-002

3.3 Thermal characteristics

All ratings are specified under board mounted and still air conditions.

Table 5 Thermal characteristics

Symbol	Definition	Min	Typ	Max	Units
$R_{\Theta JC}$	Thermal resistance, junction to case		17.6		°C/W
$R_{\Theta JA}$	Thermal resistance, junction to ambient		58.2		°C/W

3.4 Recommended operating conditions

For proper operation the device should be used within the recommended operating conditions. All voltage parameters are absolute voltages referenced to VSS unless otherwise stated.

Table 6 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_{DD}	VDD bias voltage to COM	4.75	15	V
	VDD bias voltage to VSS	4.75	13.2	V
V_{DRV}	External voltage on VDRV pin (VDD=VDRV)[1]	4.75	5.25	V
COM	COM to VSS	-3	0	V
CMRS	Common mode voltage range (static DC)[2]	-150	10	V
CMRD	Common mode voltage range (dynamic AC)[2, 3]	-200	10	V
CMSR	Common mode voltage slew rate		100	V/ns
T_A	Operating ambient temperature	-55	125	°C

[1] Connecting pins VDD and VDRV together will bypass internal LDO, allowing for drive voltage to be externally set

[2] Measurement from input signal across resistors to IN+ and IN- pins, meaning negative voltage is positive voltage on switch node in half bridge

[3] Duration of AC voltage transient event must be shorter than specified blanking time

3.5 Electrical characteristics

VDD = 4.75 V to 13.2 V, COM = VSS = 0 V and $T_A = T_J$ = -55 to 125°C unless otherwise stated. All pins with respect to VSS unless otherwise stated. **All parameter ratings apply over a total ionizing dose (TID) of 100 krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s or at a low dose rate (ELDRS) of 10 mrad(Si)/s.**

Table 7 Electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Input power						
I_{INQNL}	VIN operating current unloaded (500 kHz switching frequency)		2.4	3	mA	V_{DD}=4.75 V
			2.4	3	mA	V_{DD}=13.2V
I_{INQ}	VIN operating current loaded (500 kHz switching frequency)	5	6.5	8	mA	V_{DD}=4.75 V, C_L=1.2 nF
		5	6.6	8	mA	V_{DD}=13.2 V, C_L=1.2 nF
I_{INSD}	VIN standby current	1.5	2.1	2.8	mA	V_{DD}=4.75 V
		1.5	2.1	2.8	mA	V_{DD}=13.2 V
$V_{DRVUVLO+}$	VDRV UVLO rising threshold	4.3	4.5	4.6	V	
$V_{DRVUVLO-}$	VDRV UVLO falling threshold	4.2	4.3	4.6	V	
V_{DRVHY}	VDRV UVLO hysteresis		150		mV	
$V_{DDUVLO+}$	VDD UVLO rising threshold	4.45	4.6	4.7	V	
$V_{DDUVLO-}$	VDD UVLO falling threshold	4.35	4.5	4.6	V	
V_{DDVHY}	VDD UVLO hysteresis		100		mV	
V_{LDO}	Internal LDO dropout (VDD-VDRV)		93		mV	V_{DD}=4.75 V, I_{VDRV}=30 mA

Electrical parameters

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
I_{LDO}	VDRV current limit	160	220	300	mA	VDD=13.2 V, VDRV=3V
		120	206	290	mA	VDD=5 V, VDRV=3 V
V_{DRV}	VDRV regulation voltage	4.7	4.8	4.85	V	VDD=4.9 V I_{VDRV} =20 mA
		4.7	4.8	4.85	V	VDD = 5.2 V I_{VDRV} =60 mA
		4.7	4.8	4.85	V	VDD=5.5 V I_{VDRV} =100 mA
Input logic						
V_{IHD}	Differential input logic threshold for turn on (low to high)	1.2	2.0	2.85	V	47 kΩ on IN+, IN- VCMR = 0 V
V_{ILD}	Differential input logic threshold for turn off (high to low)	0.9	1.3	2.2	V	47 kΩ on IN+, IN- VCMR = 0 V
Output						
V_{OH}	Logic “1” output voltage (VDRV-SRC)			50	mV	I_{SRC}=20 mA
V_{OL}	Logic “0” output voltage (SNK-COM)			50	mV	I_{SNK}=20 mA
R_{SRC}	Output high internal resistance		1.4	2	Ω	
R_{SNK}	Output low internal resistance		0.7	1	Ω	
R_{CLAMP}	Miller clamp internal resistance		0.7	1	Ω	
I_{SRC}	Output high short circuit pulsed current[1]		1.5		A	PW ≤ 10 µs
I_{SNK}	Output low short circuit pulsed current[1]		2.5		A	PW ≤ 10 µs
I_{CLAMP}	Miller clamp current[1]		2.5		A	
V_{CLAMP}	Miller clamp voltage threshold	0.7	0.8	0.9	V	
Timing						
t_r	Rise time[1]		4		ns	C_L=1nF
t_f	Fall time[1]		4		ns	C_L=1nF
t_{on}	Turn-on propagation delay[1]		25		ns	C_L=1nF CONFIG3=OPEN CONFIG2=OPEN CONFIG1=OPEN
t_{off}	Turn-off propagation delay [1]		23		ns	
Δt_{LHHL}	Propagation delay matching[1]		1.4	2.9	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		12		ns	
t_{on}	Turn-on propagation delay[1]		45		ns	C_L=1nF CONFIG3=OPEN CONFIG2=OPEN CONFIG1=VSS
t_{off}	Turn-off propagation delay[1]		44		ns	
Δt_{LHHL}	Propagation delay matching[1]		0.9	1.9	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		18.5		ns	
t_{on}	Turn-on propagation delay[1]		63		ns	C_L=1nF

Electrical parameters

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{off}	Turn-off propagation delay[1]		62		ns	CONFIG3=OPEN CONFIG2=VSS CONFIG1=OPEN
Δt_{LHHL}	Propagation delay matching[1]		0.9	1.9	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		36		ns	
t_{on}	Turn-on propagation delay[1]		83		ns	C_L=1nF CONFIG3=OPEN CONFIG2=VSS CONFIG1=VSS
t_{off}	Turn-off propagation delay[1]		82		ns	
Δt_{LHHL}	Propagation delay matching[1]		0.9	2.4	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		54		ns	
t_{on}	Turn-on propagation delay[1]		102		ns	C_L=1nF CONFIG3=VSS CONFIG2=OPEN CONFIG1=OPEN
t_{off}	Turn-off propagation delay[1]		102		ns	
Δt_{LHHL}	Propagation delay matching[1]		0.9	2.4	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		72		ns	
t_{on}	Turn-on propagation delay[1]		122		ns	C_L=1nF CONFIG3=VSS CONFIG2=OPEN CONFIG1=VSS
t_{off}	Turn-off propagation delay[1]		121		ns	
Δt_{LHHL}	Propagation delay matching[1]		0.8	1.8	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		90		ns	
t_{on}	Turn-on propagation delay[1]		141		ns	C_L=1nF CONFIG3=VSS CONFIG2=VSS CONFIG1=OPEN
t_{off}	Turn-off propagation delay[1]		140		ns	
Δt_{LHHL}	Propagation delay matching[1]		0.8	2.2	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		108		ns	
t_{on}	Turn-on propagation delay (maximum blanking) [1]		160		ns	C_L=1nF CONFIG3=VSS CONFIG2= VSS CONFIG1= VSS
t_{off}	Turn-off propagation delay (maximum blanking) [1]		159		ns	
Δt_{LHHL}	Propagation delay matching[1]		0.8	2.4	ns	
t_{PWmin}	Shortest input pulse transferred to the output[1]		126		ns	
Overtemperature protection						
OTP+	Internal overtemperature protection rising threshold[1]	174	178	185	°C	
OTP-	Internal overtemperature protection falling threshold[1]	132		141		

[1] Parameter not subject to production test. Parameter guaranteed by design and characterization.

4 Timing Diagrams

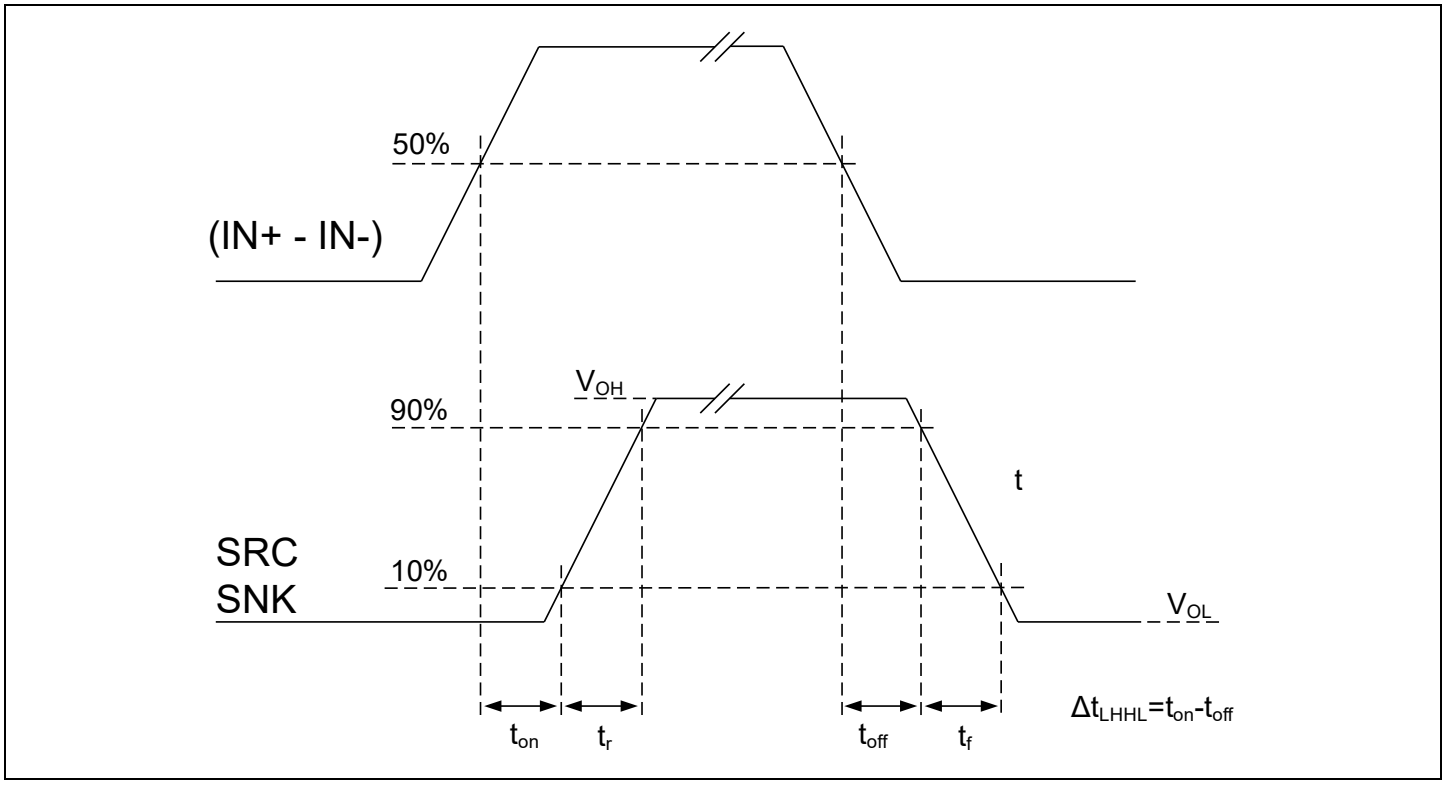
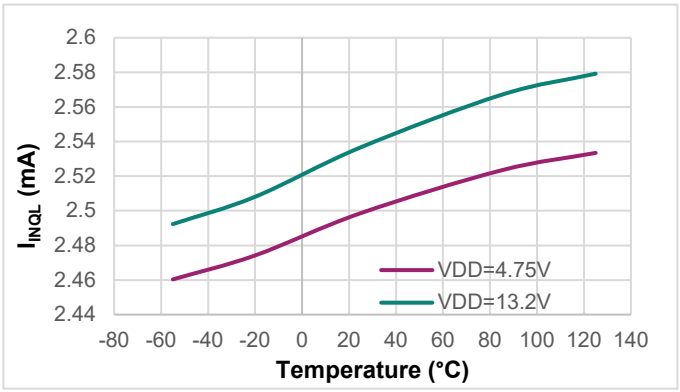


Figure 4 Rise time, fall time, propagation delay and delay matching definition

5 Typical Characteristics



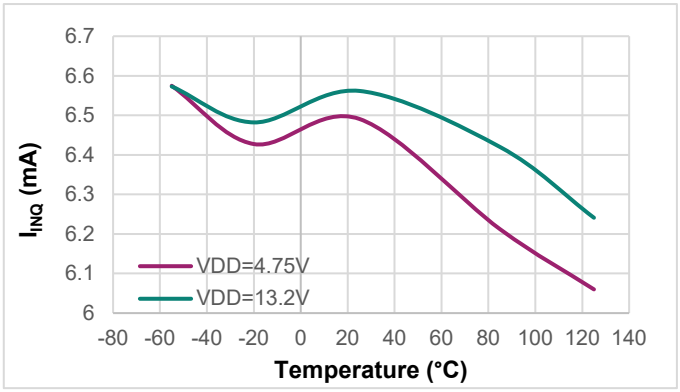


Figure 5 IINQL input current unloaded and IINQ input current with CL=1.2nF

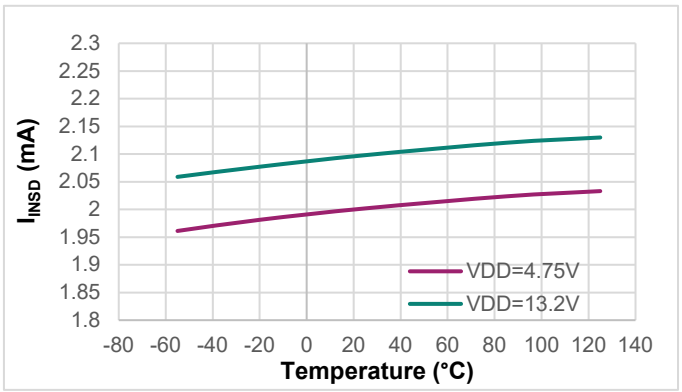
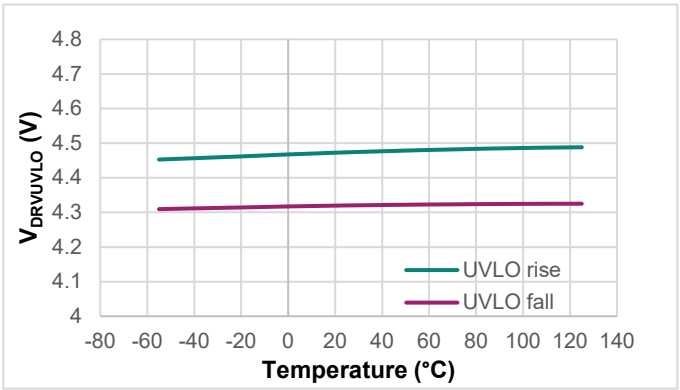


Figure 6 IINSD input standby current



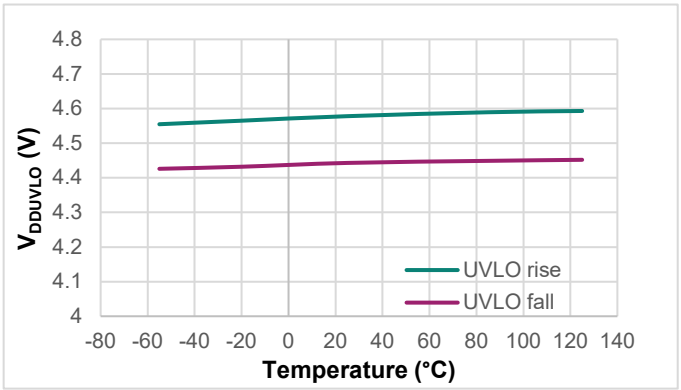
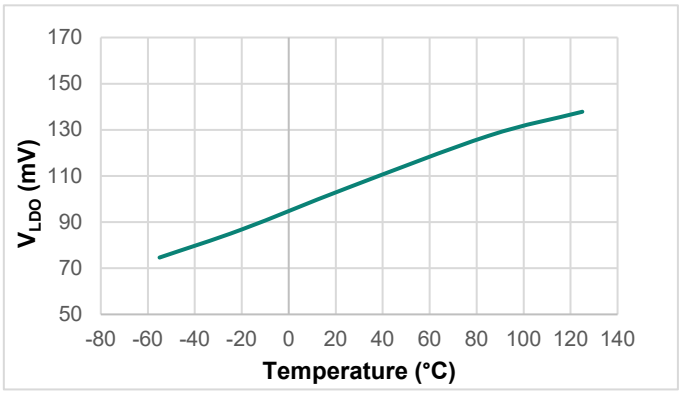


Figure 7 VDD and VDRV UVLO rising and falling thresholds



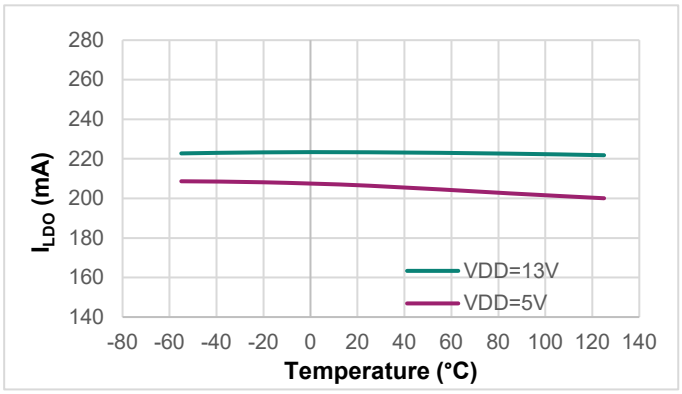


Figure 8 LDO dropout and VDRV current limit

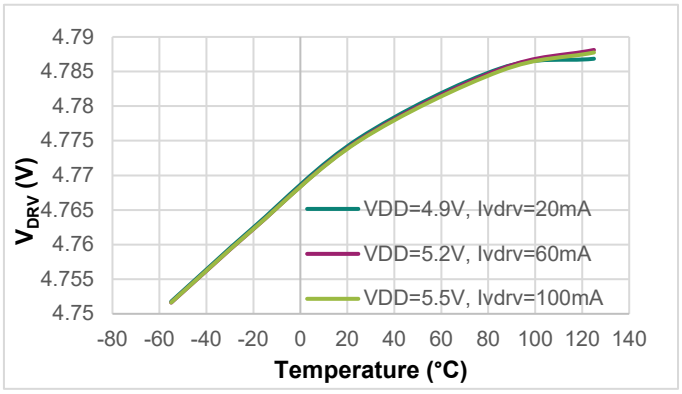
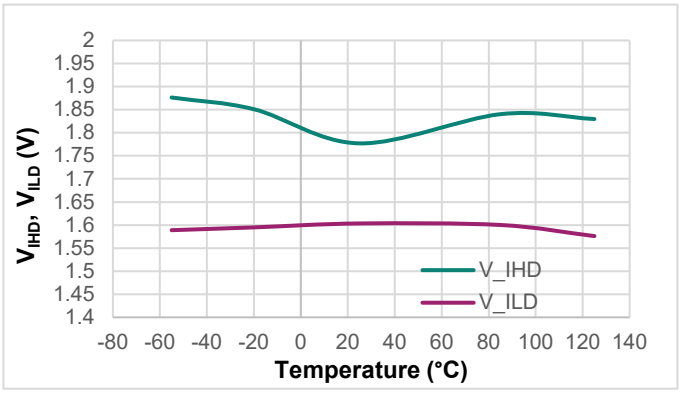


Figure 9 VDRV regulation voltage



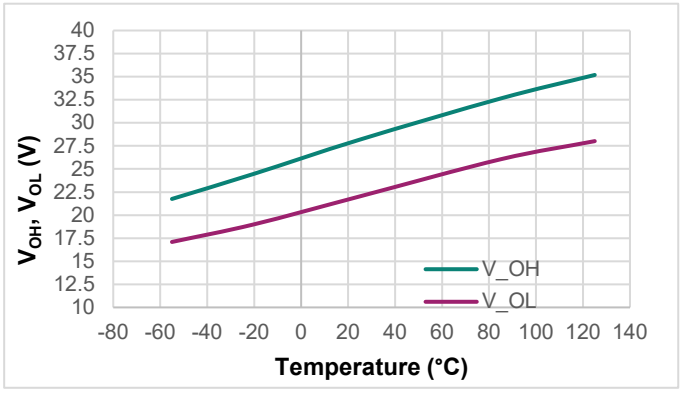


Figure 10 VIHD, VILD Differential input logic for turn on and off
VOH, VOL Logic "1" and logic "0" output voltage

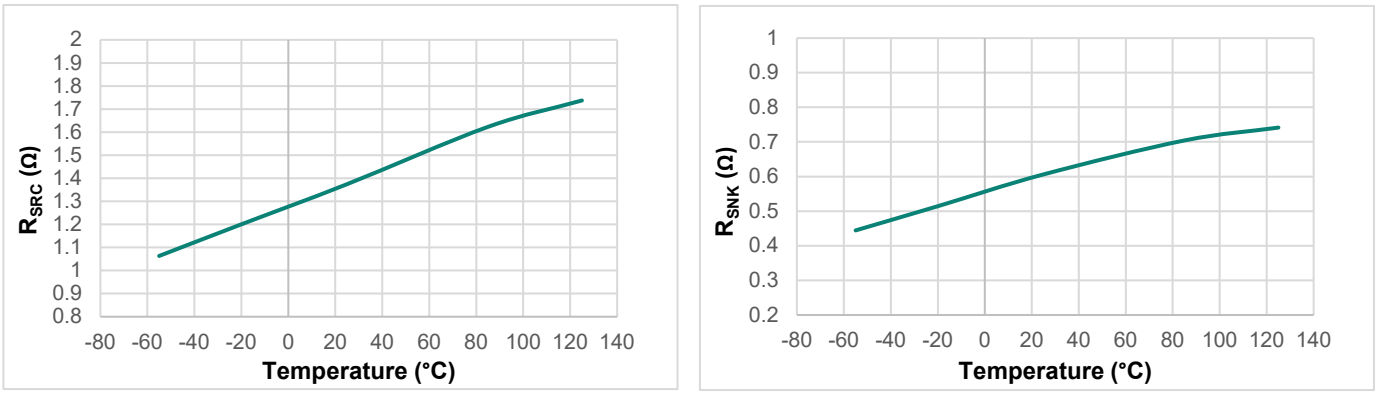


Figure 11 RSRC Output high internal resistance and RSNK output low internal resistance

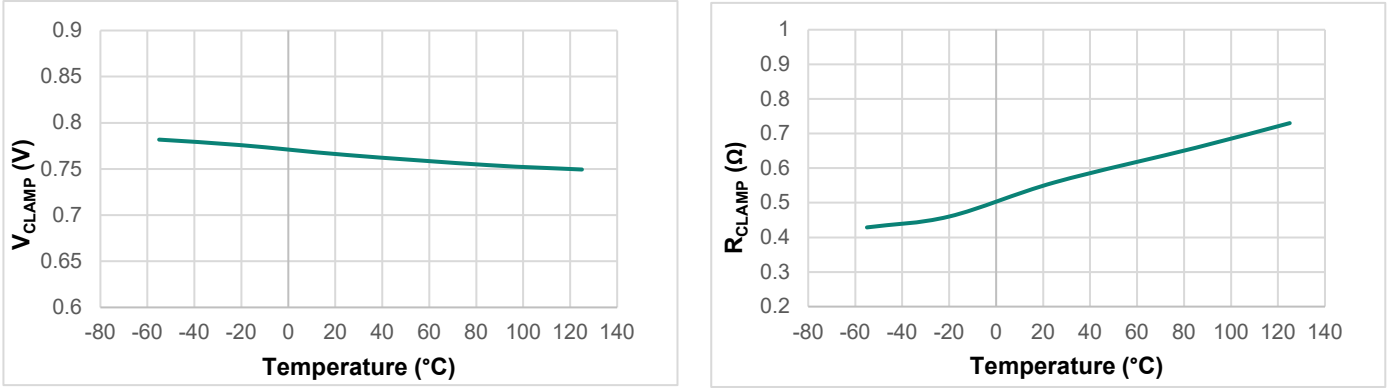


Figure 12 RCLAMP Miller clamp internal resistance and VCLAMP Miller clamp voltage threshold

6 General description

RIC70115 is a single channel gate driver that can work in low or high side applications. It has a logic level output, which makes it well suited to drive GaN Schottky gate (SG) HEMT or logic level Si FETs like the rad hard R8 FET family. RIC70115 will be certified for use in space applications per Defense Logistics Agency (DLA) MIL-PRF-38535 Class V.

6.1 Radiation performance

RIC70115 is designed to work in space and other applications where there is significant ionizing radiation and energetic particles in the environment that can affect microcircuit performance. RIC70115 will be characterized for operation up to a total ionizing dose (TID) of 100 krad(Si), with electrical parameters including limits post-irradiation. It will also be characterized for single event effects (SEE) up to 81.9 MeV·cm^2/mg.

The packaged versions of RIC70115 do not have any electrically floating metal, with all metal internally connected to a known, controlled potential (such as the metal lid). This allows for compliance with system level requirements prohibiting electrically floating metal without the need to add additional wires.

6.1.1 Total ionizing dose (TID)

RIC70115 will be tested over total ionizing dose (TID) to verify robustness to ionizing protons and electrons radiation environments, such as space. The radiation hardness assurance (RHA) program at IR HiRel uses a Cobalt-60 (60 Co) source and heavy ion irradiation. Every wafer will be tested per MIL-STD-883, Method 1019, test condition A “Ionizing Radiation (Total Dose) Test Procedure.” Both pre- and post-irradiation performance are tested to the limits specified in the electrical characteristics.

6.1.2 Single event effects (SEE)

RIC70115 will be characterized in heavy ion environment for single event effects (SEE) up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg. RIC70115 will be immune to destructive events single event burnout (SEB), single event gate rupture (SEGR) and single event latch-up (SEL) over the full operating range of RIC70115 up to an LET of 81.9 MeV·cm^2/mg. RIC70115 will also characterized for single event transient (SET) up to an LET of 81.9 MeV·cm^2/mg.

6.2 Input power and bias

RIC70115 can be powered to provide a drive voltage that is a tightly regulated 4.8 V from an internal LDO or provide a drive voltage from an external voltage source.

6.2.1 Internal LDO

RIC70115 features an internal LDO that steps down an external voltage from VDD to a tightly regulated 4.8 V drive voltage on VDRV. This 4.8 V drive voltage on VDRV is used for gate drive on SRC. Additionally, this internal LDO can power other loads by applying load to VDRV. The internal LDO has a current limit I_{LDO}, after which the LDO will enter constant current mode. When the internal LDO is used to generate VDRV voltage, a ceramic capacitor or similarly low ESR capacitor of at least 2 µF is recommended on VDRV for proper operation.

6.2.2 External bias

RIC70115 can alternately work with other drive voltages, such as 5 V, by externally applying the input voltage on both VDD and VDRV. This will bypass the internal LDO, allowing the drive voltage to be the externally applied voltage.

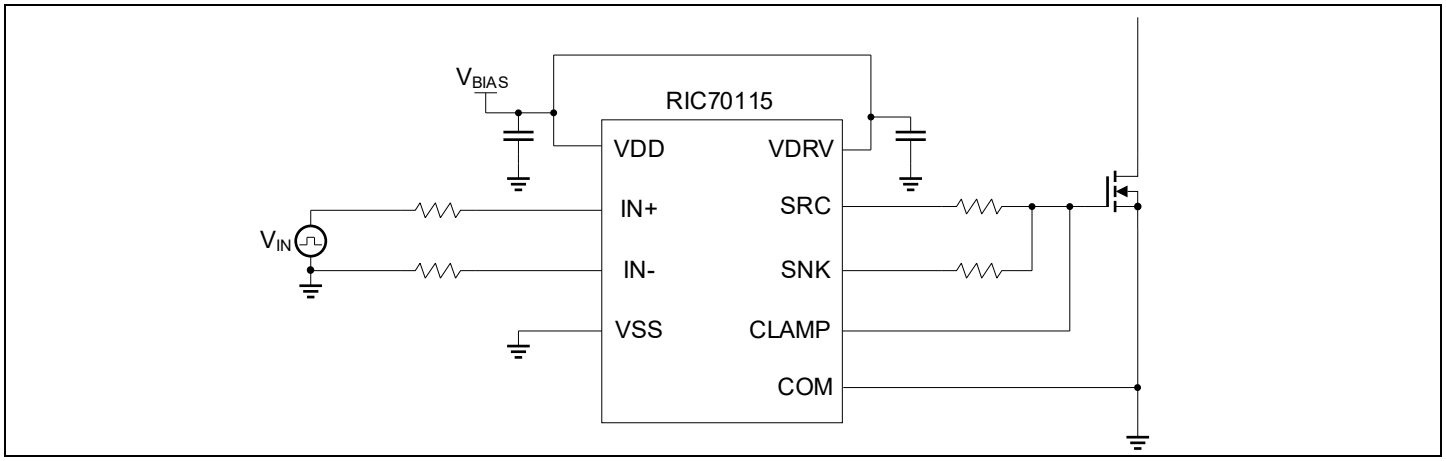


Figure 13 Example external bias where drive voltage is V_{BIAS}

6.2.3 Negative drive

RIC70115 can optionally provide a negative drive voltage if an external negative voltage is applied to the COM pin. This allows for improved robustness against induced turn on but at the expense of increased third quadrant “body diode” forward voltage drop loss.

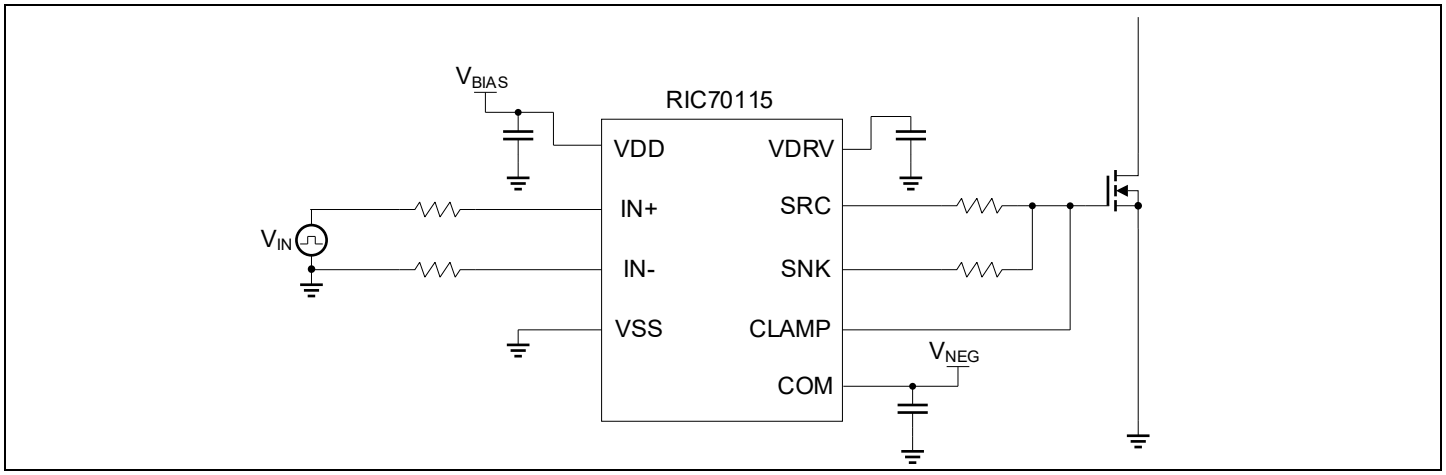


Figure 14 Example configuration with negative turn off V_{NEG}

6.3 Input

RIC70115 features truly differential input (TDI), where the input logic is a differential voltage from IN+ to IN- pins. TDI improves robustness against common mode noise up to 150 V static and 200 V dynamic, enabling both low and high side operation without the need for external level shifting, like a digital isolator. For proper operation an external resistor is required for any input that a voltage is applied on.

6.3.1 Minimum input pulse

To help prevent spurious switching during common-mode transient events, RIC70115 features programmable input blanking time. When enabled, the blanking time will prevent any input pulse that is shorter than the blanking time from propagating to the output. Blanking time is set by connecting CONFIG 3, CONFIG 2 and CONFIG 1 pins to either VSS or open. All CONFIG pins have an internal pull up resistor.

Table 8 Blanking time based on CONFIG pin settings

CONFIG 3	CONFIG 2	CONFIG 1	Blanking time
Open	Open	Open	0 ns
Open	Open	VSS	20 ns
Open	VSS	Open	37 ns
Open	VSS	VSS	58 ns
VSS	Open	Open	77 ns
VSS	Open	VSS	97 ns
VSS	VSS	Open	116 ns
VSS	VSS	VSS	135 ns

6.3.2 Selection of TDI input resistors

RIC70115 requires precise input resistors on the IN+ and IN- pins. These resistors are not optional, even if the application does not require the TDI function. The input logic thresholds at the IN+ and IN- pins are designed to be paired with the specified input resistor values. These input resistors should be selected with a 0.1% tolerance, especially in high-side applications, where the common-mode voltage rating is contingent upon tight matching of input resistors. Extra care should be taken to ensure that these resistors are symmetrical, so that stray capacitance across them is also tightly matched.

In high-side applications, the input resistors must also be rated for the power dissipation expected in the worst-case operating conditions. The common-mode voltage observed by the high side transistor is “blocked” by each input resistor, so that RIC70115 is not exposed to the high voltage. The resistor dissipate power during the intervals where common-mode voltage is high, typically during the high-side transistors’ duty ratio of each switching period. The power rating of the resistors should therefore be selected based on the following equation.

$$P_{Rin+} = P_{Rin-} = \frac{{V_{DC,max}}^2}{R_{in+}} \times D$$

Where,

- P_{Rin+} is the required power rating for the input resistor on the IN+ pin in watts (W)
- P_{Rin-} is the required power rating for the input resistor on the IN- pin in watts (W)
- D is the high side duty ratio
- $V_{DC,max}$ is the maximum expected DC bus voltage, experienced as common mode voltage during the high-side duty ration in volts (V)

It is important to consider that the duty ratio may not be constant, so D should be selected as the duty ratio when operating at the maximum DC bus voltage. The following table lists some examples for selecting the input resistors, based on logic voltage level, expected DC bus voltage and duty ratio. For most applications, the power requirement is quite low, thereby allowing the designer to select very small resistor packages such as 0402 or 0603. In some extreme scenarios with a high DC voltage and high duty ratio simultaneously, larger packages with higher power ratings may be needed.

Table 9 Examples for selected input resistors

Maximum DC bus voltage	Logic voltage	Duty ratio	TDI input resistance	Resistor tolerance	Minimum Rin power rating
60 V	3.3 V	0.25	47 kΩ	0.1%	0.02 W
60 V	5 V	0.25	75 kΩ	0.1%	0.01 W
80 V	3.3 V	0.25	47 kΩ	0.1%	0.10 W
80 V	5 V	0.25	75 kΩ	0.1%	0.06 W

6.3.3 Low side

In low side operation, differential input logic from IN+ to IN- is used to improve immunity to any common mode noise, such as ground bounce.

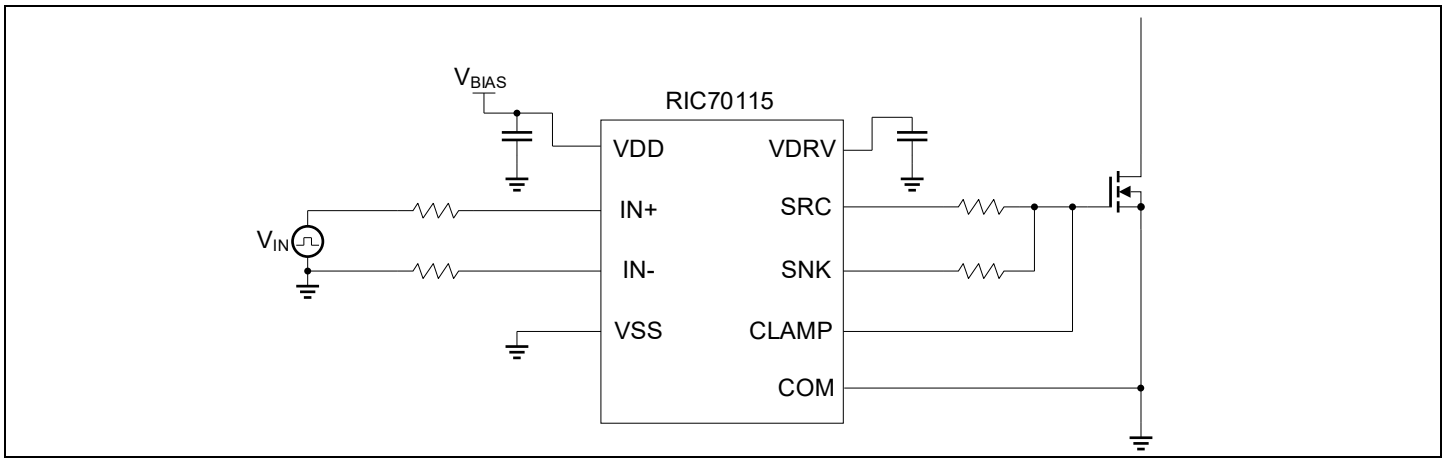


Figure 15 Example configuration for low side drive with differential input

6.3.4 High side

The common mode voltage (V_{CMR}) support of up to 150 V static and 200 V dynamic allows RIC70115 to work in high side applications without the need for any logic level shifting device, such as a digital isolator. The high voltage is “blocked” by external resistors on IN+ and IN-. To prevent any noise from being applied to the input pins due to imbalance on the input (such as tolerance variation between input resistors) or noise during the switching transition, blanking time can be set on RIC70115. The amount of blanking time is adjustable, with fixed values from 0 ns to 135 ns programmable by connecting various CONFIG pins to VSS or leave open, details of which are in Table 8

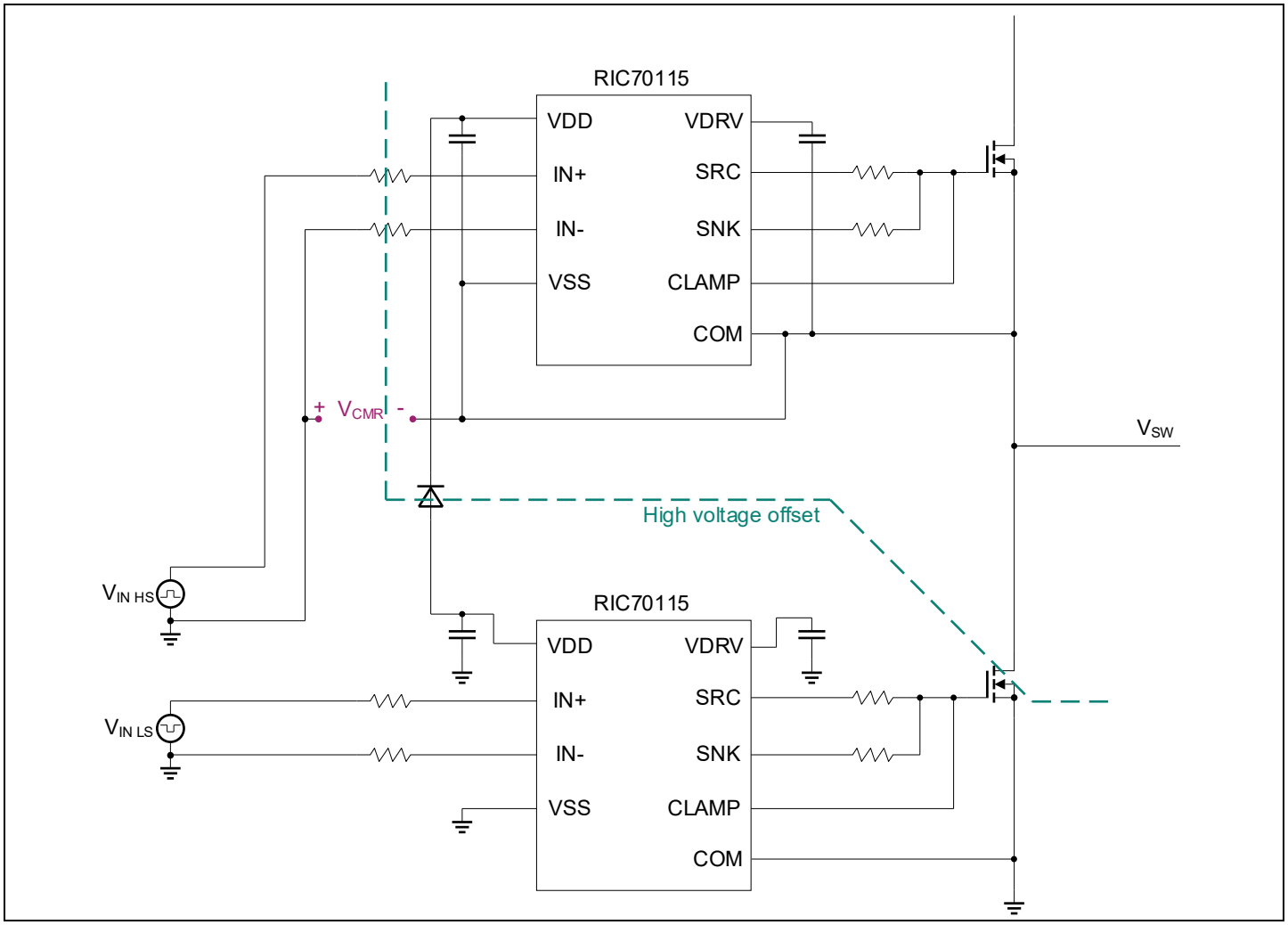


Figure 16 Example configuration for high side drive

6.3.5 Optional additional input filter

To improve performance by reducing single event transient (SET) events, an additional resistor and capacitor filter can be optionally added on the input IN+ and IN- pins. The optional filter capacitance is recommended to be 40 pF, and can be adjusted. The input resistors R_{IN+} and R_{IN-} can be reduced with the following equations for 3.3 V and 5 V input logic. Reducing the input resistors R_{IN+} and R_{IN-} improve SET performance, but cause higher power loss during high side operation and require more drive current from the input logic source (V_{IN})

$$R_{FLT\ 3.3V\ logic} = \frac{R_{IN}}{47k\Omega - R_{IN}} \times 1.5k\Omega$$

$$R_{FLT\ 5V\ logic} = \frac{R_{IN}}{75k\Omega - R_{IN}} \times 1.5k\Omega$$

Where,

- R_{FLT} is the resistance of the optional input filter in ohm (Ω)
- R_{IN} is the resistance of the input resistor R_{IN+} and R_{IN-} in ohm (Ω) and cannot exceed 47 kΩ for 3.3V logic and 75 kΩ for 5V logic

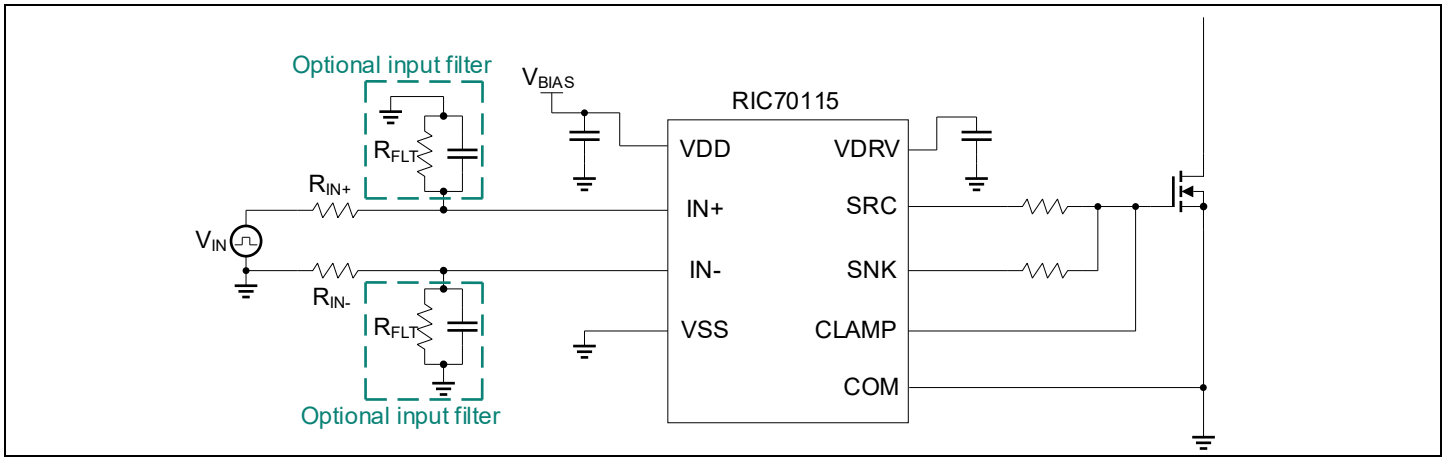


Figure 17 Example configuration for low side drive with differential input

Note that adding this optional input filter will extend matching delay, requiring additional dead time in the low tens of nanoseconds. Additionally, if the device is operating in low side or a lower high side voltage (like a 28 V bus with DC max of 40 V), the external input resistor R_{IN+} and R_{IN-} resistance can be reduced.

6.4 Output

RIC70115 features a 1.5 A peak source and 2.5 A peak sink gate drive strength. The source and sink drive are independent pins, allowing the user to set the desired turn on and off slew rate with external resistors.

6.4.1 Miller clamp

In some applications, such as GaN HEMT where there is a high voltage slew rate on the drain when the GaN HEMT is being held off, an induced voltage can be generated on the gate of the power switch. If not properly accounted for in design, this induced voltage can be high enough to cause the GaN HEMT to improperly turn on.

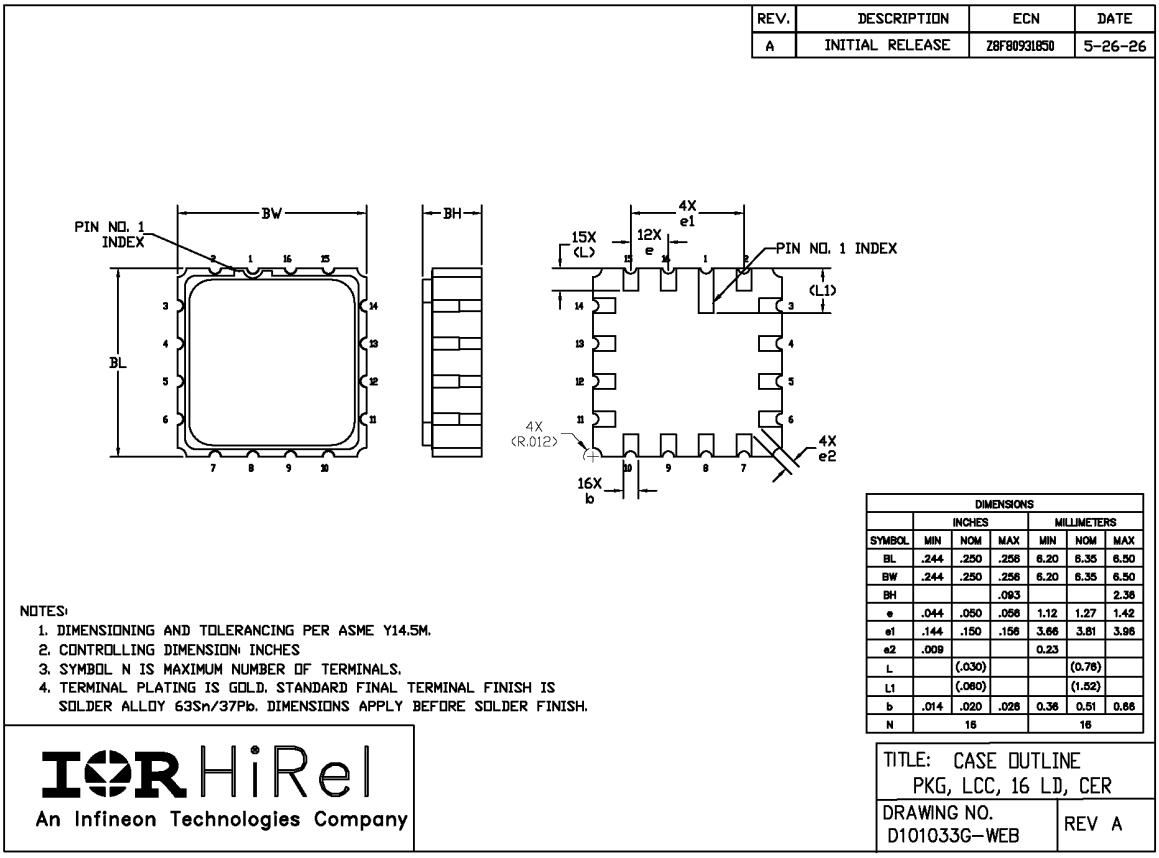
To prevent this, RIC70115 includes an integrated miller clamp on the CLAMP pin. The miller clamp is on a separate pin activates after the switch is fully turned off. This allows the turn off speed, which is determined by SNK and any external resistance on it, to be set at the desired speed for the turn off switching transition. Once off, the miller clamp enables, greatly reducing the impedance between gate to source, preventing induced voltages from rising high enough to causing the switch to improperly turn on.

6.5 Fault protection

RIC70115 features two integrated fault protections, VDD undervoltage lockout (UVLO), VDRV undervoltage lockout (UVLO) and overtemperature protection (OTP). VDRV UVLO prevents RIC70115 from operating unless the VDRV voltage is sufficiently high enough, which protects against an insufficient gate drive voltage from not fully turning on the switch. If the switch is not fully turned on, the $R_{DS(on)}$ and power loss in the switch will be much larger than expected. OTP protects RIC70115 from operating at junction temperatures that greatly exceed 150°C, which is outside of the absolute maximum ratings of the device.

7 Package details

7.1 LCC



DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
BL	.244	.250	.256	6.20	6.35	6.50
BW	.244	.250	.256	6.20	6.35	6.50
BH			.093			2.36
e	.044	.050	.056	1.12	1.27	1.42
e1	.144	.150	.156	3.66	3.81	3.96
e2	.009			0.23		
L		(.030)			(0.76)	
L1		(.060)			(1.52)	
b	.014	.020	.026	0.36	0.51	0.66
N	16			16		

Figure 18 16 pin LCC package outline

Revision history

Document revision	Date	Description of changes

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