Final datasheet

CoolSiC™ 1200 V SiC MOSFET G2 : Silicon Carbide MOSFET with .XT interconnection technology

Features



- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 142 A at T_C = 100°C
- $R_{DS(on)}$ = 7.5 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Overload operation up to T_{vj} = 200°C
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance
- Suitable Infineon gate drivers can be found under https://www.infineon.com/gdfinder

Halogen-free
Green
Lead-free
RoHS

Potential applications

- General purpose drives (GPD)
- Online UPS / Industrial UPS

Product validation

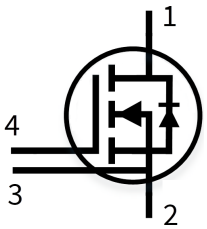
- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

Pin definition:

• Pin 1 – Drain
• Pin 2 – Source
• Pin 3 – Kelvin sense contact
• Pin 4 – Gate

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction



Type	Package	Marking
IMZC120R007M2H	PG-TO247-4-U07	12M2H007

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	Wave soldering only allowed at leads 1.6 mm (0.063 in.) from case for 10 s			260	°C
Mounting torque	M	M3 screw, Maximum of mounting processes: 3			0.6	Nm
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.16	0.21	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	201	A
			$T_c = 100$ °C	142	
Peak drain current, t_p limited by $T_{vj(max)}$ [1)]	I_{DM}	$V_{GS} = 18$ V		710	A
Gate-source voltage, max. transient voltage	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage [2)]	V_{GS}			-7...23	V
Avalanche energy, single pulse	E_{AS}	$I_D = 93$ A, $V_{DD} = 50$ V, $L = 0.24$ mH, $T_{vj(start)} = 25$ °C		1036	mJ
Avalanche energy, repetitive	E_{AR}	$I_D = 93$ A, $V_{DD} = 50$ V, $L = 1.2$ µH, $T_{vj(start)} = 25$ °C		5.18	mJ
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	711	W
			$T_c = 100$ °C	355	

1) Verified by design.
2) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 93 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		7.5		mΩ
			T_{vj} = 150 °C, $V_{GS(on)}$ = 18 V		15.3	20	
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		17.7		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		9.34		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 29.1 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.1	V
			T_{vj} = 175 °C		3.2		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			800	µA
			T_{vj} = 175 °C		13.6		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			120	nA
			V_{GS} = -10 V			-120	
Forward transconductance	g_{fs}	I_D = 93 A, V_{DS} = 20 V			60		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			4.8		Ω
Input capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			6570		pF
Output capacitance	C_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			287		pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			25		pF
C_{oss} stored energy	E_{oss}	Calculated based on C_{oss} = f(V_{DD})			121		µJ
Output charge	Q_{oss}	Calculated based on C_{oss} = f(V_{DD})			449		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on E_{oss}			378		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on Q_{oss}			562		pF
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, turn-on pulse			176		nC

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, turn-on pulse			39		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, turn-on pulse			43		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		32.4		ns
			T_{vj} = 175 °C		24.7		
Rise time	t_r	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		21.5		ns
			T_{vj} = 175 °C		19.1		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		65.2		ns
			T_{vj} = 175 °C		76.3		
Fall time	t_f	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		28.5		ns
			T_{vj} = 175 °C		33.6		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		1670		µJ
			T_{vj} = 175 °C		2270		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		1360		µJ
			T_{vj} = 175 °C		1760		
Total switching energy[1)]	E_{tot}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		3358		µJ
			T_{vj} = 175 °C		4924		

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Turn-on energy at -5 V	E_{on}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		1670		µJ
			T_{vj} = 175 °C		2270		
Turn-off energy at -5 V	E_{off}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		620		µJ
			T_{vj} = 175 °C		700		
Total switching energy at -5 V[1)]	E_{tot}	V_{DD} = 800 V, I_D = 93 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 12 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		2605		µJ
			T_{vj} = 175 °C		4035		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[2)]				200	°C

1) including E_{fr}
2) up to 5000 cycles. Maximum ΔT limited to 100 K.

***Note**: The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.*

Characteristics at T_{vj} = 25°C, unless otherwise specified.

3 Body diode (MOSFET)

Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} ≥ 25 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	137	A
			T_c = 100 °C	75	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	V_{GS} = 0 V		426	A

Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 93 A, V_{GS} = 0 V	T_{vj} = 25 °C		4.2	5.5	V
			T_{vj} = 100 °C		4.11		
			T_{vj} = 175 °C		4.05		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 93 A, V_{GS}=0 V, $R_{GS(on)}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		0.7		µC
			T_{vj} = 175 °C		2.31		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 93 A, V_{GS}=0 V, $R_{GS(on)}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		63.8		A
			T_{vj} = 175 °C		111.5		
MOSFET forward recovery energy	E_{fr}	V_{DD} = 800 V, I_{SD} = 93 A, V_{GS}=0 V, $R_{GS(on)}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		328		µJ
			T_{vj} = 175 °C		894		
MOSFET forward recovery energy at -5 V	E_{fr}	V_{DD} = 800 V, I_{SD} = 93 A, V_{GS} = -5 V, $R_{GS(on)}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		315		µJ
			T_{vj} = 175 °C		1065		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[1)]				200	°C

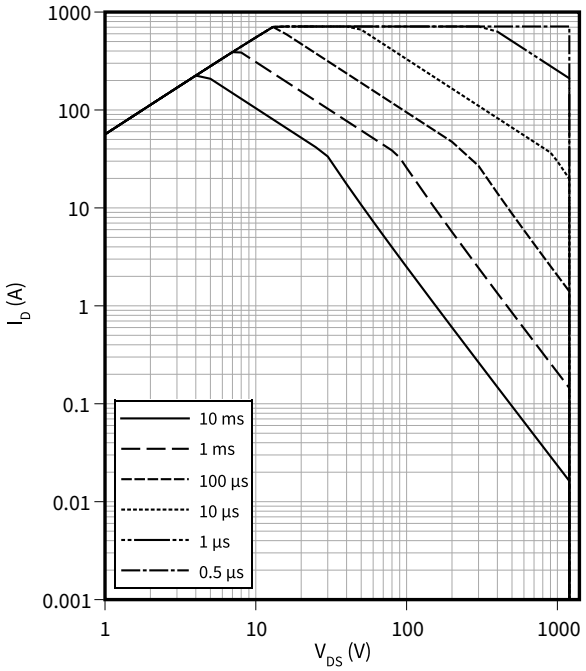
1) up to 5000 cycles. Maximum ΔT limited to 100 K.

4 Characteristics diagrams

Safe operating area (SOA)

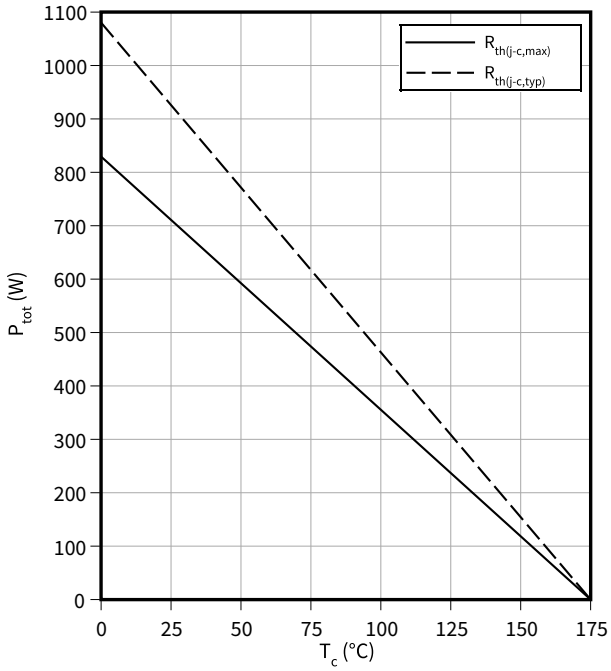
$I_D = f(V_{DS})$

$T_{vj} \leq 175\ °C$, $T_c = 25\ °C$



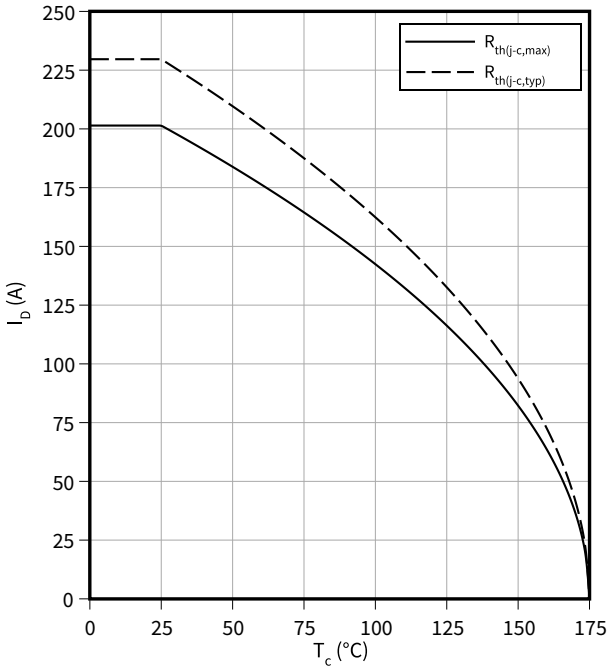
Power dissipation as a function of case temperature

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

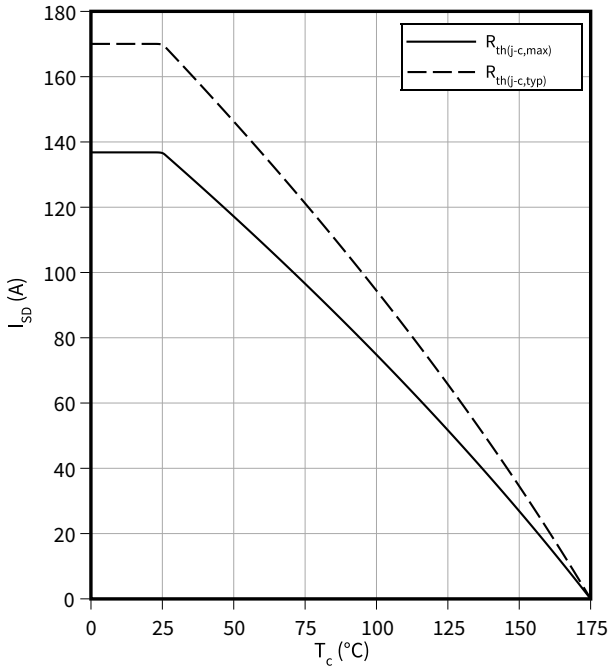
$I_D = f(T_c)$



Maximum source to drain current as a function of case temperature limited by bond wire

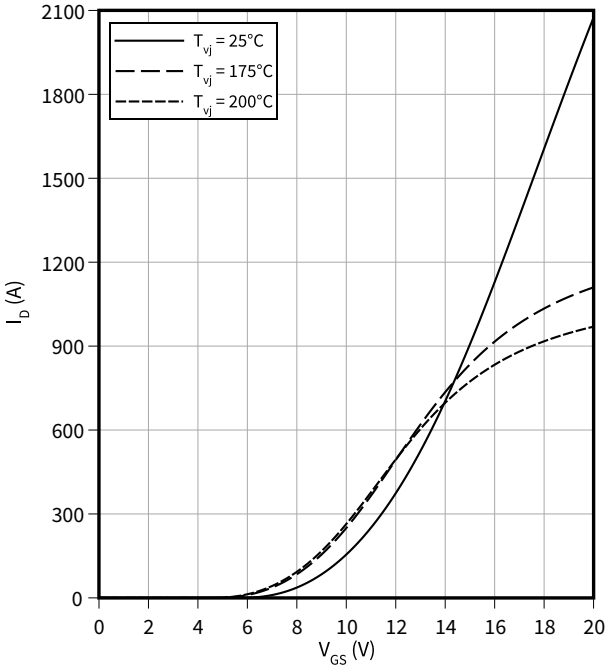
$I_{SD} = f(T_c)$

$V_{GS} = 0\ V$



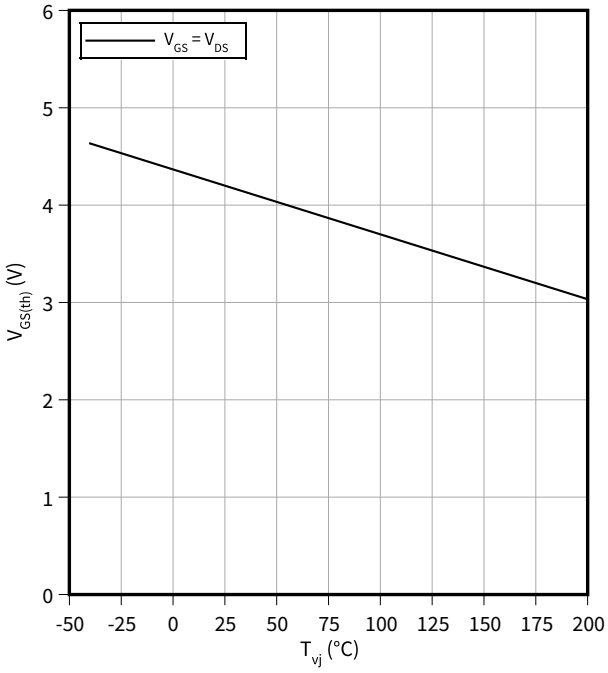
Typical transfer characteristic

$I_D = f(V_{GS})$
V_{DS} = 20 V, t_p = 20 µs



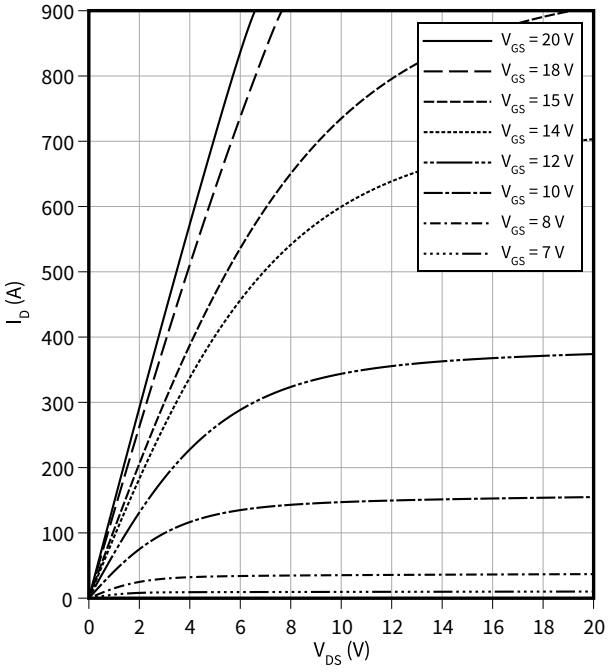
Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$
I_D = 29.1 mA



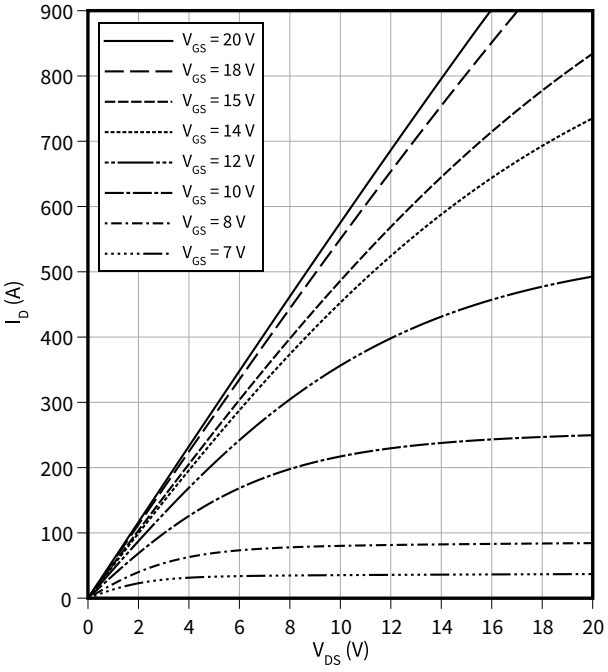
Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$
T_{vj} = 25 °C, t_p = 20 µs



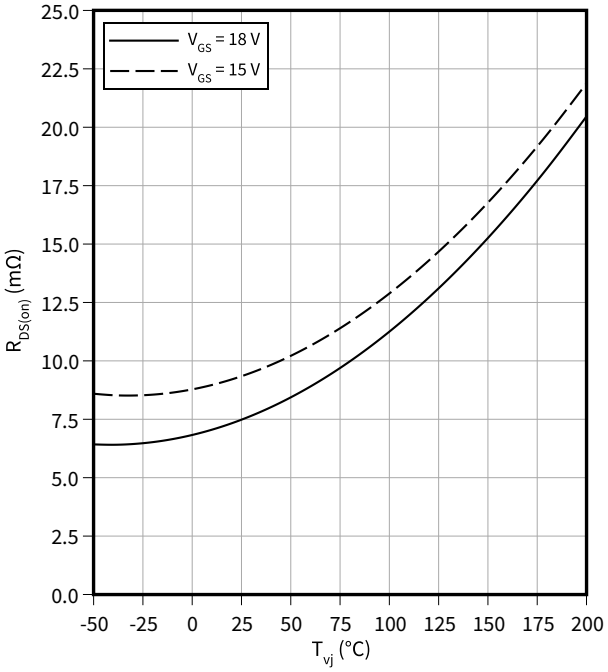
Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$
T_{vj} = 175 °C, t_p = 20 µs



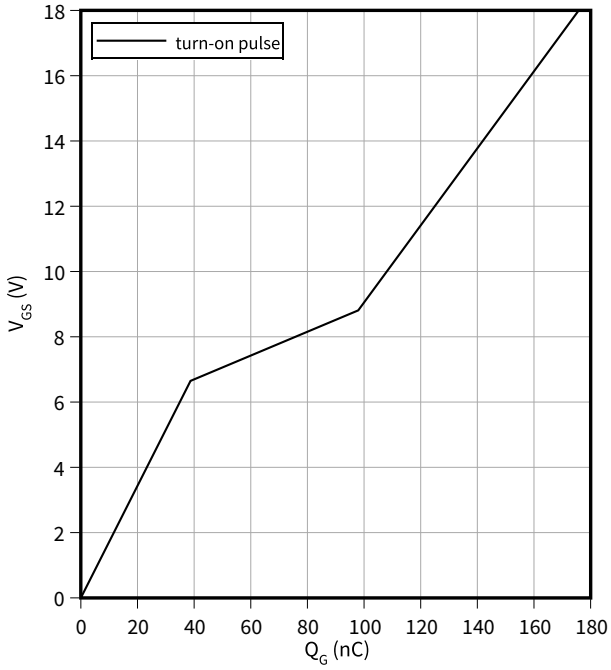
Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$
$I_D = 93$ A



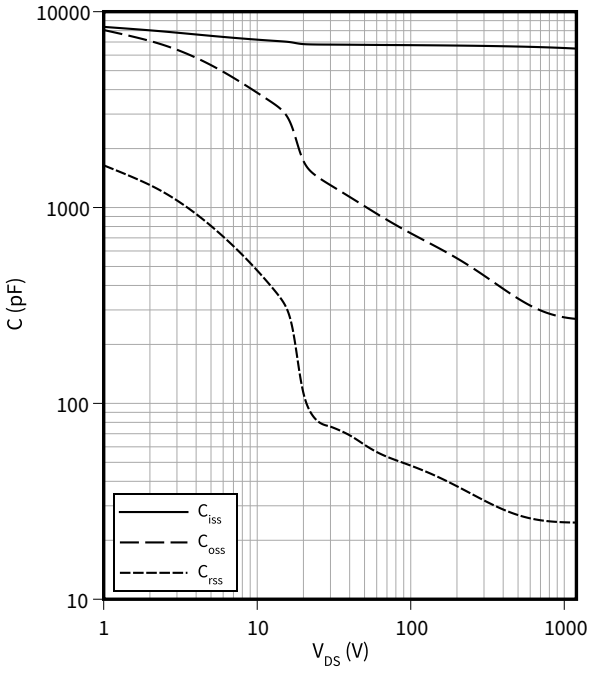
Typical gate charge

$V_{GS} = f(Q_G)$
$I_D = 93$ A, $V_{DS} = 800$ V



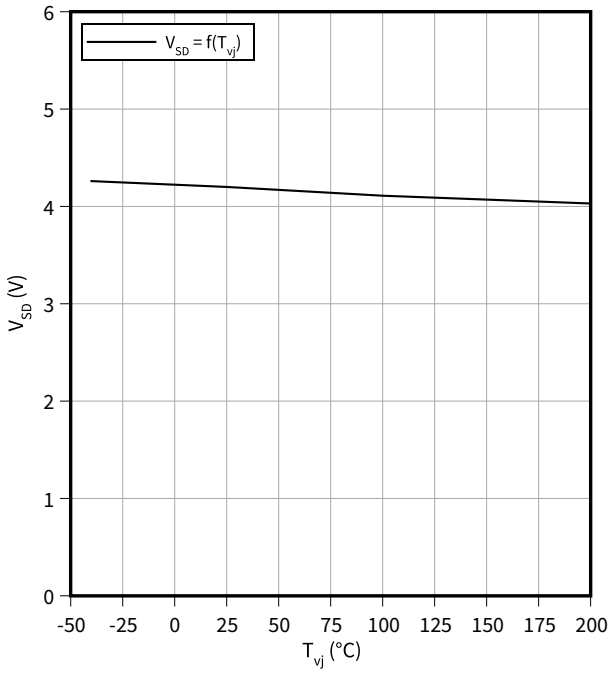
Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$
$f = 100$ kHz, $V_{GS} = 0$ V



Typical reverse drain voltage as a function of junction temperature

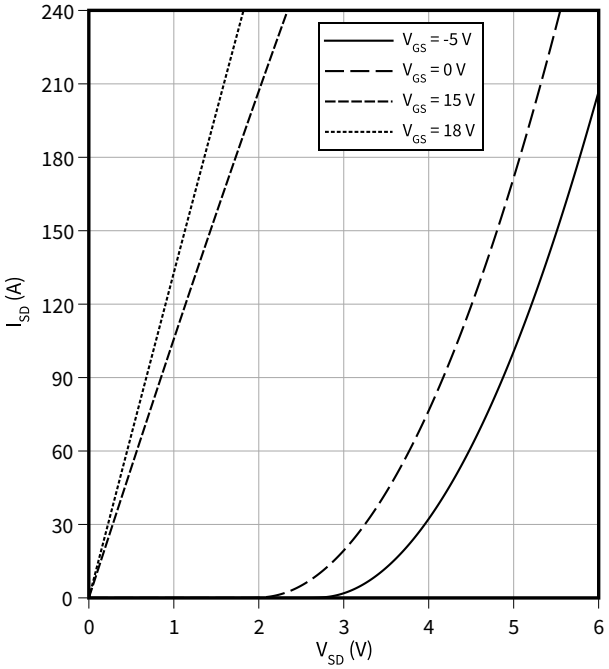
$V_{SD} = f(T_{vj})$
$I_{SD} = 93$ A, $V_{GS} = 0$ V



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

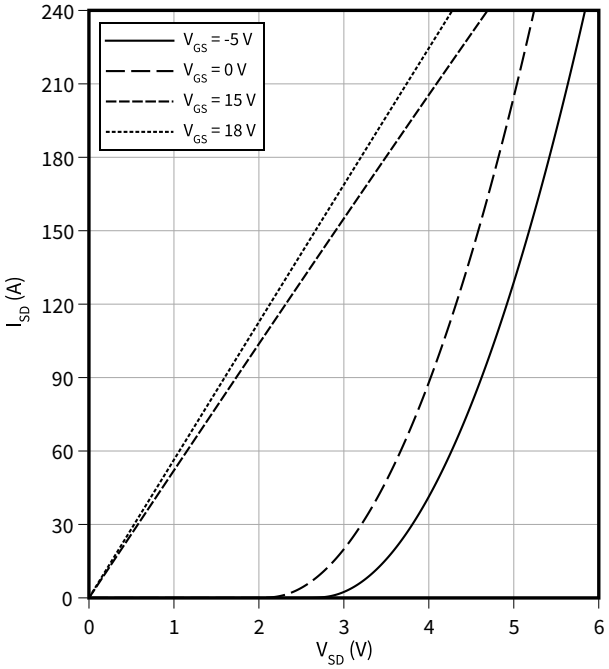
$T_{vj} = 25\ °C$, $t_p = 20\ µs$



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

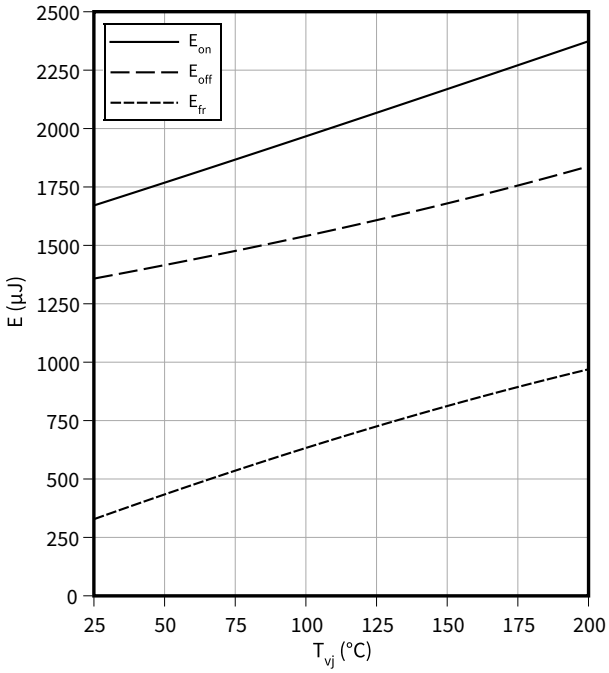
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\ V$

$E = f(T_{vj})$

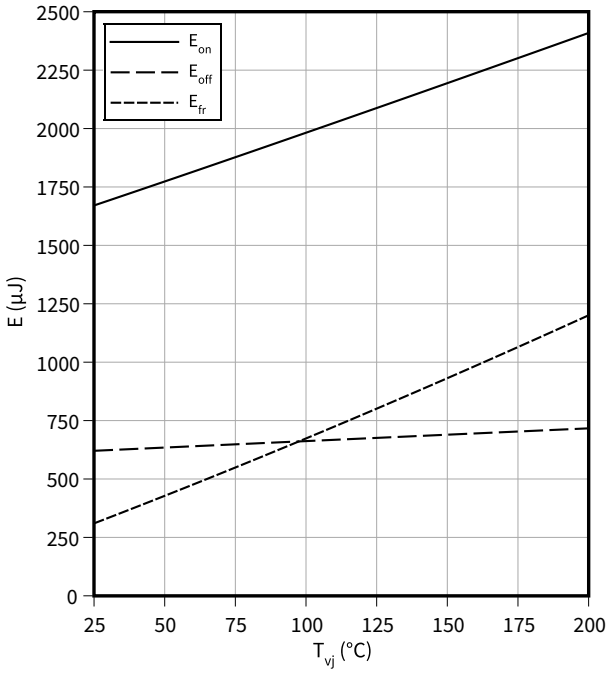
$V_{GS} = 0/18\ V$, $I_D = 93\ A$, $R_{G,ext} = 2.3\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = -5\ V$

$E = f(T_{vj})$

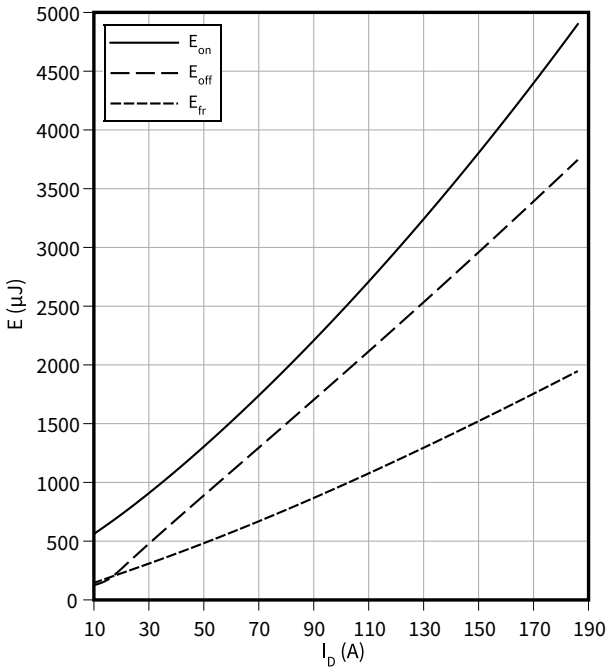
$V_{GS} = -5/18\ V$, $I_D = 93\ A$, $R_{G,ext} = 2.3\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(I_D)$

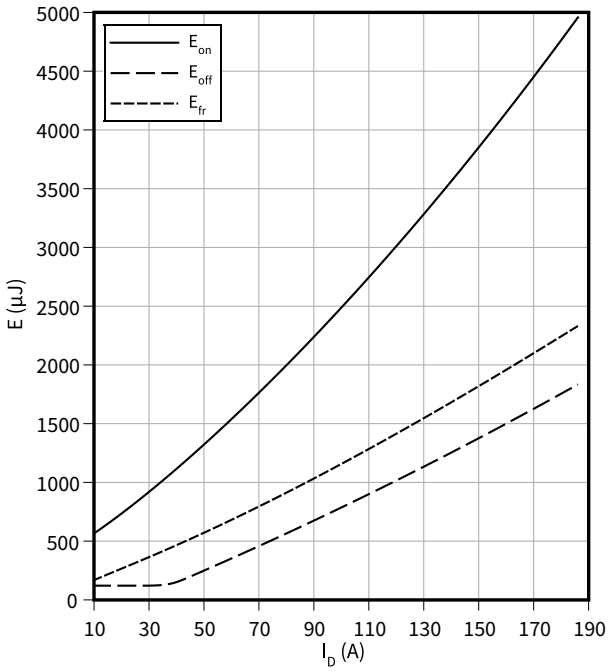
V_{GS} = 0/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(I_D)$

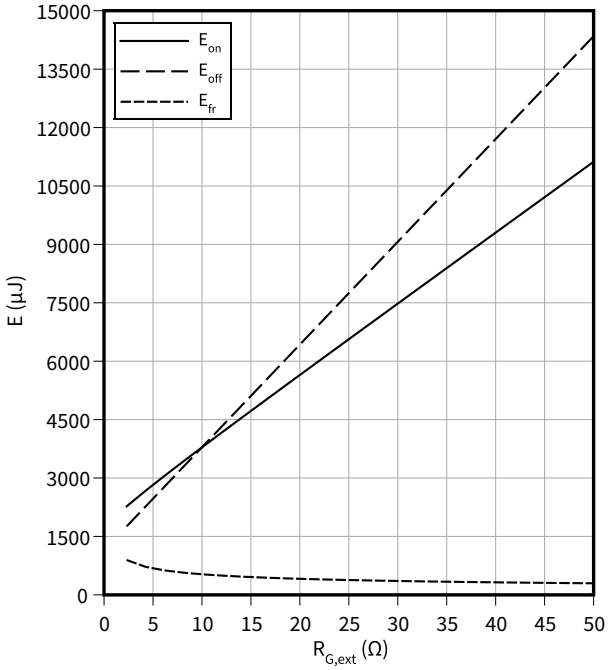
V_{GS} = -5/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

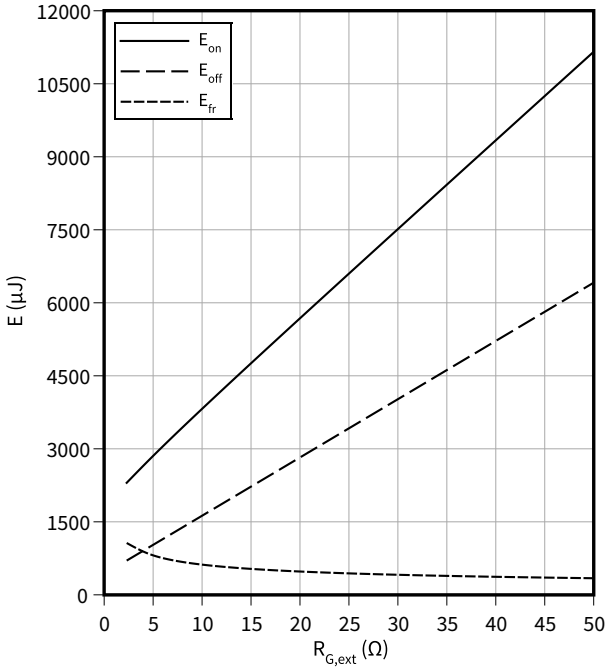
V_{GS} = 0/18 V, I_D = 93 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(R_{G,ext})$

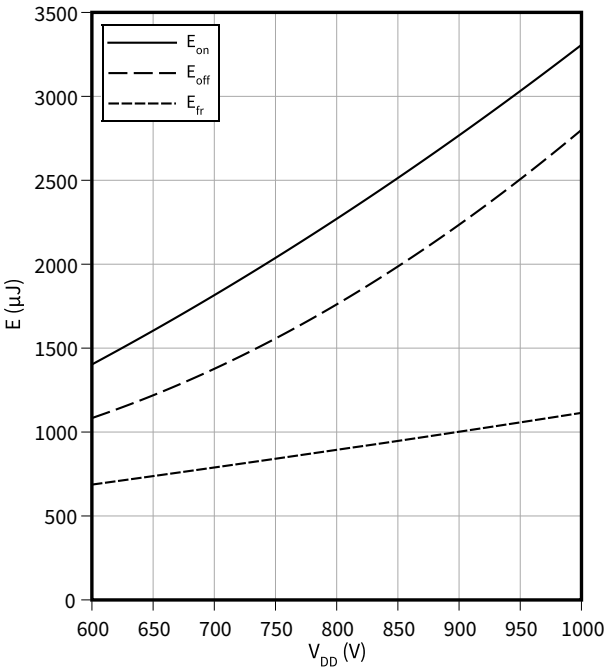
V_{GS} = -5/18 V, I_D = 93 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

E = f(V_{DD})

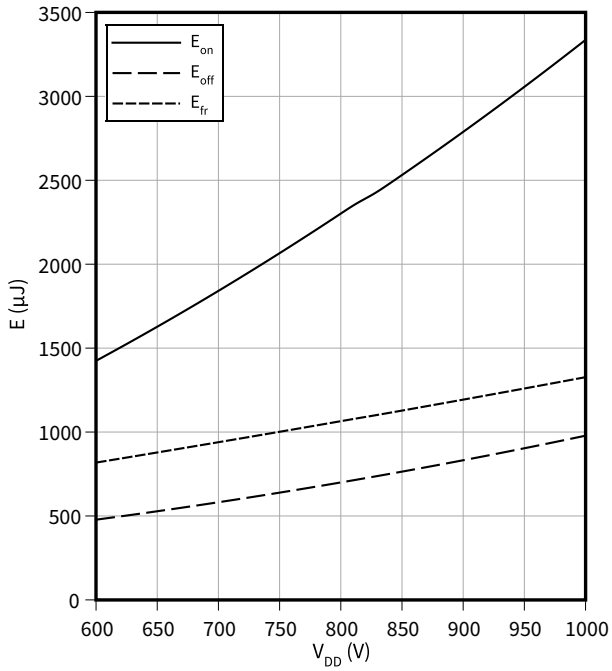
V_{GS} = 0/18 V, I_D = 93 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

E = f(V_{DD})

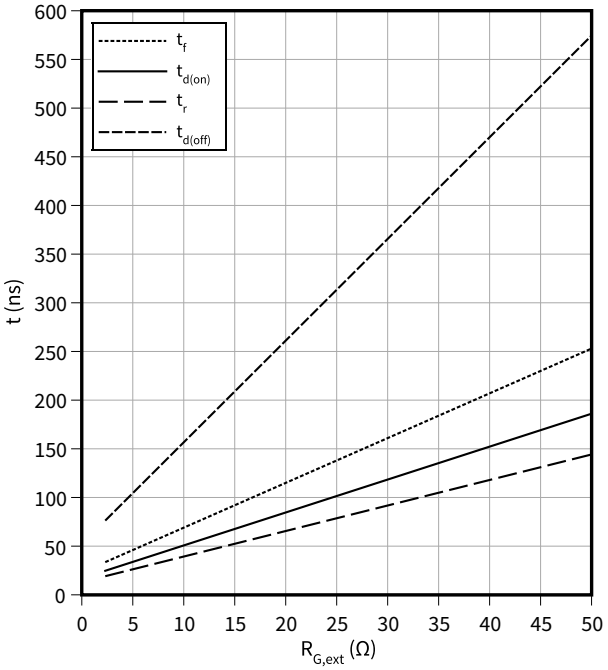
V_{GS} = -5/18 V, I_D = 93 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

t = f($R_{G,ext}$)

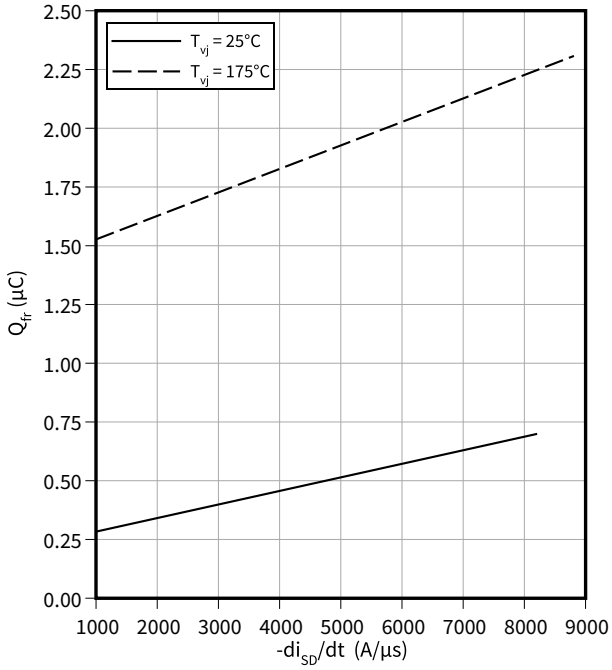
V_{GS} = 0/18 V, I_D = 93 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

Q_{fr} = f(-di_{SD}/dt)

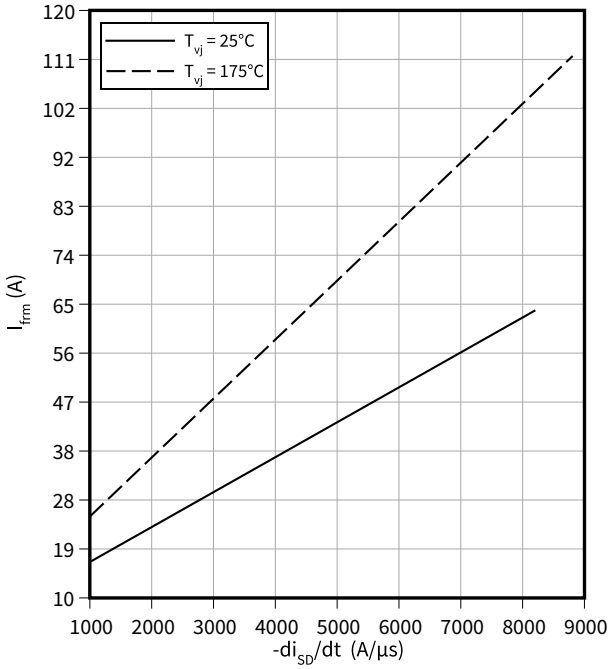
V_{GS} = 0/18 V, I_{SD} = 93 A, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$I_{frm} = f(-di_{SD}/dt)$

V_{GS} = 0/18 V, I_{SD} = 93 A, V_{DD} = 800 V

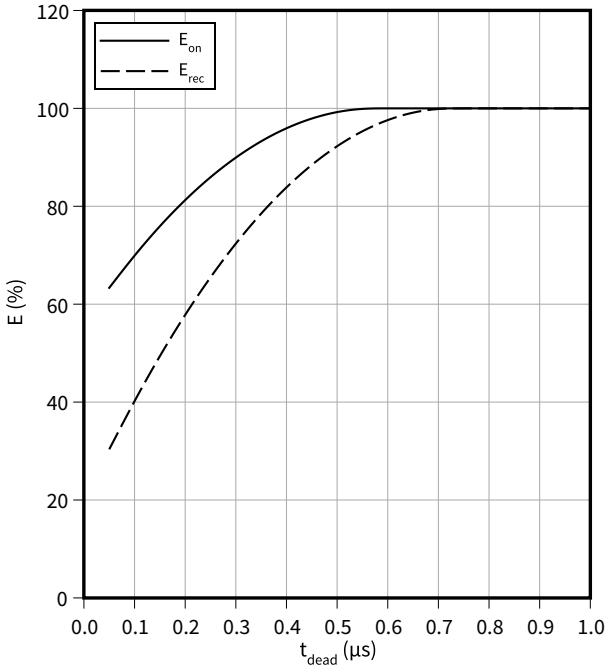


Typical switching energy as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(t_{dead})$

I_D = 93 A, V_{GS} = 0/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω

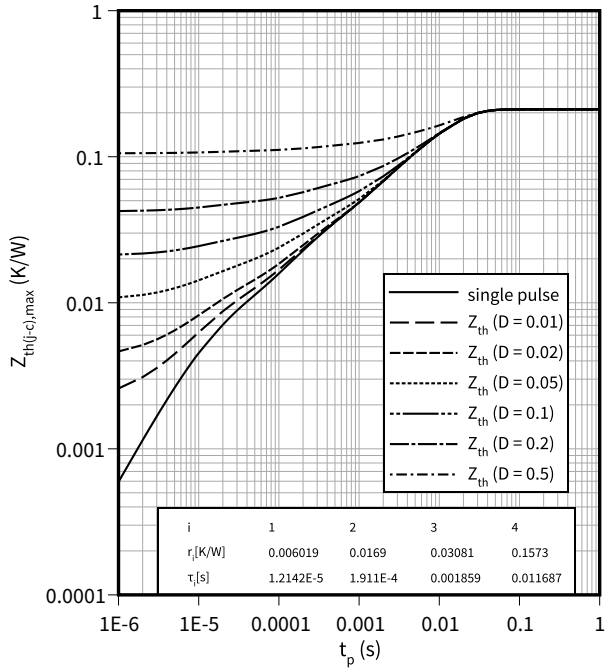
V_{DD} = 800 V



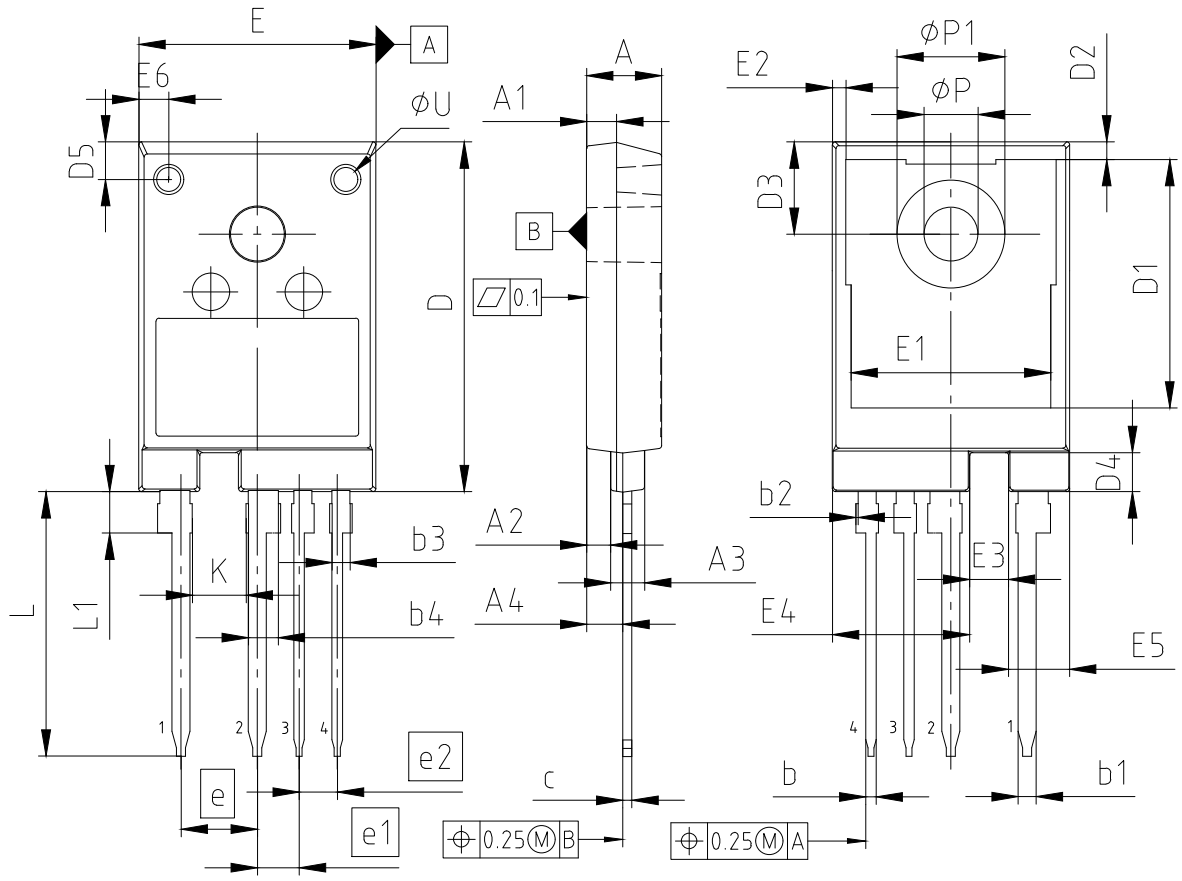
Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO247-4-U07				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	**E**	15.60	16.00
A1	1.90	2.10	**E1**	13.10	13.50
A2	1.50	1.70	**E2**	0.60	1.20
A3	2.16	2.36	**E3**	2.48	2.68
A4	2.31	2.51	**E4**	9.05	9.25
b	0.60	0.80	**E5**	3.97	4.17
b1	1.10	1.30	**E6**	1.80	2.20
b2	---	0.15	**e**	5.08	
b3	1.10	1.30	**e1**	2.79	
b4	1.90	2.10	**e2**	2.54	
c	0.50	0.70	**K**	3.50	---
D	23.10	23.50	**L**	17.50	17.80
D1	16.25	16.85	**L1**	2.61	2.91
D2	0.97	1.37	**N**	4	
D3	6.00	6.30	**ØP1**	7.00	7.40
D4	2.50	2.70	**ØP**	3.50	3.70
D5	2.30	2.70	**ØU**	1.40	1.80

NOTES: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
N IS THE NUMBER OF LEADS

Figure 1

6 Testing conditions

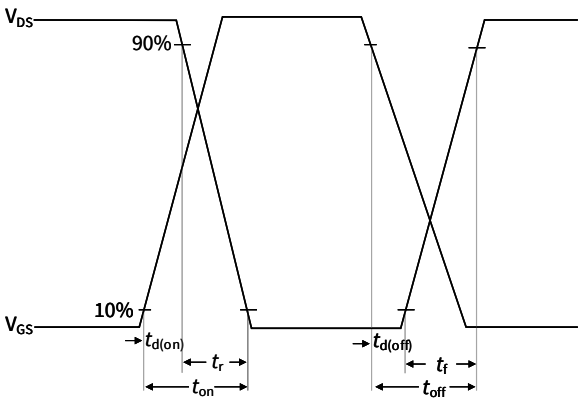


Figure A. **Definition of switching times**

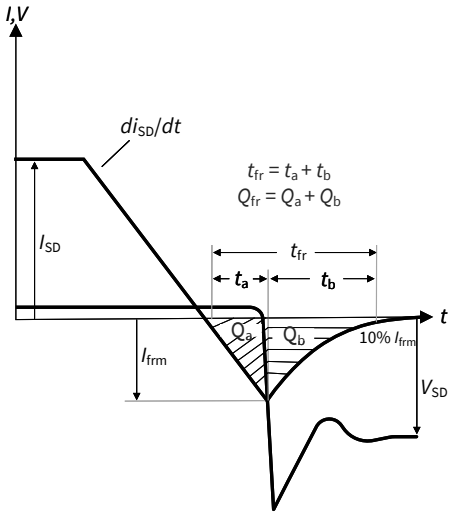


Figure B. **Definition of body diode switching characteristics**

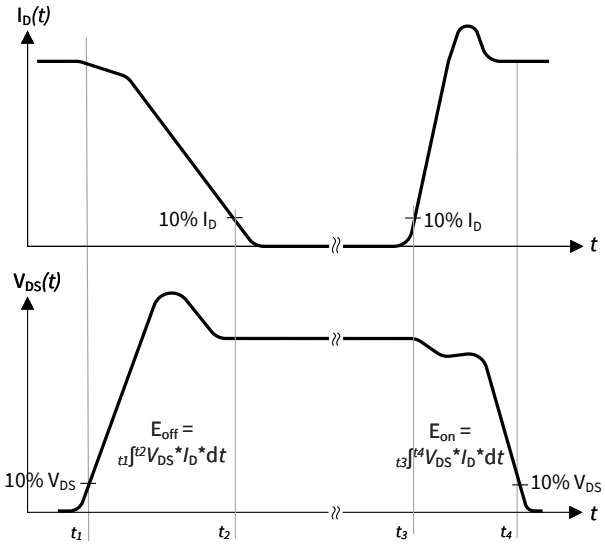


Figure C. **Definition of switching losses**

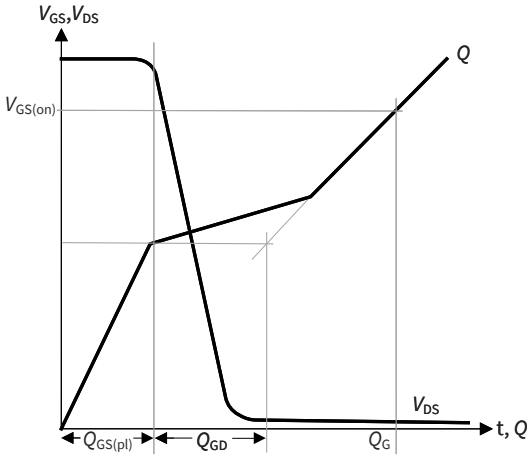


Figure D. **Definition of QGD**

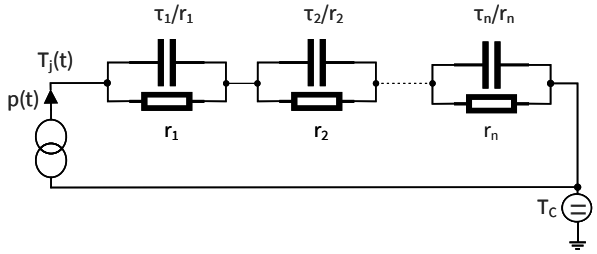


Figure E. **Thermal equivalent circuit**

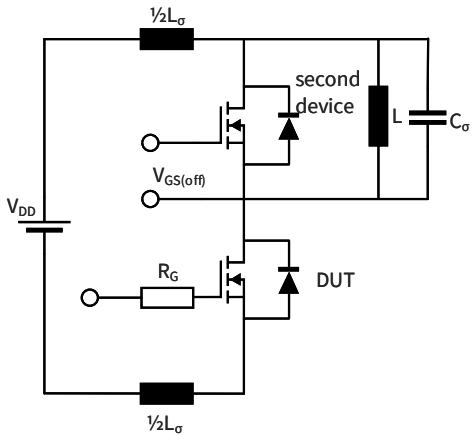


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2025-01-17	Preliminary datasheet
1.00	2025-04-28	Final datasheet
1.10	2025-09-22	Increased I_{DM} in Table 2 Added switching information for V_{GS} = -5/18 V in Table 4 and 6 and corresponding diagrams Added I_{SDC} in Table 5 Added SOA diagram on page 8 Added diagram E = f(V_{DD}) @ V_{GS} = 0/18 V Added diagram E = f(V_{DD}) @ V_{GS} = -5/18 V Editorial changes

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