

## SiC MOSFET

### CoolSiC™ MOSFET 750 V G2

Built on Infineon's robust 2<sup>nd</sup> generation Silicon Carbide trench technology, the 750 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

### Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class  $R_{DS(on)} \times Q_{fr}$
- Excellent  $R_{DS(on)} \times Q_{oss}$  and  $R_{DS(on)} \times Q_G$
- Unique combination of low  $C_{rSS}/C_{iSS}$  and high  $V_{GS(th)}$
- Infineon proprietary die attach technology
- Driver source pin available

### Benefits

- Enhanced robustness and reliability for bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Best-in-class thermal dissipation
- Reduced switching losses through improved gate control

### Potential applications

- EV charging infrastructure
- Solar PV inverters and UPS
- Energy storage and battery formation
- Telecom and Server SMPS
- Solid state relays and circuit breakers

### Product validation

Qualified according to relevant JEDEC tests.

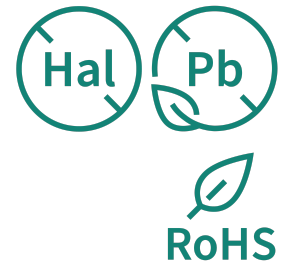
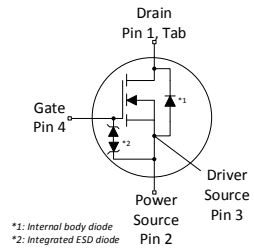
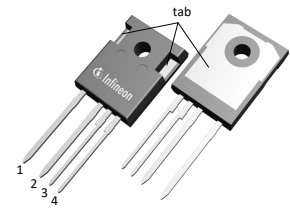
*Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction. When paralleling MOSFETs the placement of the gate resistor is generally recommended to be in series to the Driver Source instead of the Gate.*

**Table 1 Key performance parameters**

Parameter	Value	Unit
$V_{DSS}$ over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	33	mΩ
$R_{DS(on),max}$	41	mΩ
$Q_{G,typ}$	37	nC
$I_{D,pulse}$	179	A
$Q_{oss,typ}$ @ 500 V	79	nC
$E_{oss,typ}$ @ 500 V	13.9	μJ

Part number	Package	Marking	Related links
IMZA75R033M2H	PG-TO247-4	75R033M2	see Appendix A

PG-TO247-4



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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

“Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	$V_{\text{DSS}}$	-	-	750	V	static, $T_j = -55^\circ\text{C}$ to $175^\circ\text{C}$
Continuous DC drain current <sup>1)</sup>	$I_{\text{DDC}}$	-	-	47	A	$T_c = 25^\circ\text{C}$
				33		$T_c = 100^\circ\text{C}$
Peak drain current <sup>2)</sup>	$I_{\text{DM}}$	-	-	179	A	$T_c = 25^\circ\text{C}$ , $V_{\text{GS}} = 18\text{ V}$
Avalanche energy, single pulse	$E_{\text{AS}}$	-	-	169	mJ	$I_{\text{D}} = 6.3\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11
Avalanche energy, repetitive	$E_{\text{AR}}$	-	-	0.87		
Avalanche current, single pulse	$I_{\text{AS}}$	-	-	6.3	A	-
MOSFET $dv/dt$ ruggedness	$dv/dt$	-	-	200	V/ns	$V_{\text{DS}} = 0 \dots 500\text{ V}$
Gate source voltage (static) <sup>3)</sup>	$V_{\text{GS}}$	-7	-	23	V	-
Gate source voltage (transient)	$V_{\text{GS}}$	-11	-	25	V	$t_p \leq 500\text{ ns}$ , duty cycle $\leq 1\%$
Power dissipation	$P_{\text{tot}}$	-	-	164	W	$T_c = 25^\circ\text{C}$
Storage temperature	$T_{\text{stg}}$	-55	-	150	°C	-
Operating junction temperature	$T_j$			175		
Extended operating junction temperature <sup>4)</sup>	$T_j$	-	-	200	°C	$\leq 100\text{ h}$ in the application lifetime
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous reverse drain current <sup>1)</sup>	$I_{\text{SDC}}$	-	-	47	A	$V_{\text{GS}} = 18\text{ V}$ , $T_c = 25^\circ\text{C}$
				37		$V_{\text{GS}} = 0\text{ V}$ , $T_c = 25^\circ\text{C}$
Peak reverse drain current <sup>2)</sup>	$I_{\text{SM}}$	-	-	179	A	$T_c = 25^\circ\text{C}$ , $t_p \leq 250\text{ ns}$
				51		$T_c = 25^\circ\text{C}$
Insulation withstand voltage	$V_{\text{ISO}}$	-	-	n.a.	V	$V_{\text{rms}}$ , $T_c = 25^\circ\text{C}$ , $t = 1\text{ min}$

1) Limited by  $T_{j,\text{max}}$ .

2) Pulse width  $t_{\text{pulse}}$  limited by  $T_{j,\text{max}}$ .

3) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

4) Up to 7500 temperature cycles, where maximum delta  $T$  is limited to 100K.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	0.65	0.91	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063in.) from case for 10s

### 3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-		

## 4 Electrical characteristics

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 5 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage <sup>5)</sup>	$V_{(BR)DSS}$	840	-	-	V	$V_{GS} = 0\text{ V}, I_D = 0.59\text{ mA}$
Gate threshold voltage <sup>6)</sup>	$V_{GS(th)}$	3.5	4.5	5.6	V	$V_{DS} = V_{GS}, I_D = 5.9\text{ mA}, T_j = 25^\circ\text{C}$
		-	3.3	-		$V_{DS} = V_{GS}, I_D = 5.9\text{ mA}, T_j = 175^\circ\text{C}$
Zero gate voltage drain current	$I_{DSS}$	-	1	75	$\mu\text{A}$	$V_{DS} = 750\text{ V}, V_{GS} = 0\text{ V}, T_j = 25^\circ\text{C}$
			10	-		$V_{DS} = 750\text{ V}, V_{GS} = 0\text{ V}, T_j = 175^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	1	$\mu\text{A}$	$V_{GS} = 23\text{ V}, V_{DS} = 0\text{ V}, T_j = 25^\circ\text{C}$
				-1		$V_{GS} = -7\text{ V}, V_{DS} = 0\text{ V}, T_j = 25^\circ\text{C}$
Forward transconductance	$g_{fs}$	-	16.0	-	S	$I_D = 27.0\text{ A}, V_{DS} = 20\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	43.0	-	$\text{m}\Omega$	$V_{GS} = 15\text{ V}, I_D = 27.0\text{ A}, T_j = 25^\circ\text{C}$
			33.0	41.3		$V_{GS} = 18\text{ V}, I_D = 27.0\text{ A}, T_j = 25^\circ\text{C}$
			30.0	-		$V_{GS} = 20\text{ V}, I_D = 27.0\text{ A}, T_j = 25^\circ\text{C}$
Drain-source on-state resistance <sup>7)</sup>	$R_{DS(on)}$	-	52.5	65.6	$\text{m}\Omega$	$V_{GS} = 18\text{ V}, I_D = 27.0\text{ A}, T_j = 150^\circ\text{C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	59.0	-	$\text{m}\Omega$	$V_{GS} = 18\text{ V}, I_D = 27.0\text{ A}, T_j = 175^\circ\text{C}$
Internal gate resistance	$R_{G,int}$	-	2.5	-	$\Omega$	$f = 1\text{ MHz}$

<sup>5)</sup> Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

<sup>6)</sup> Tested after pre-conditioning pulse at  $V_{GS} = +20\text{ V}$ . "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

<sup>7)</sup> Specified by design, not subject to production test.

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1294	-	$\text{pF}$	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, f = 250\text{ kHz}$
Reverse transfer capacitance	$C_{rss}$		6.7	-		
Output capacitance <sup>8)</sup>	$C_{oss}$		89	115		
Output charge <sup>8)</sup>	$Q_{oss}$	-	79	102	nC	calculation based on $C_{oss}$
Effective output capacitance, energy related <sup>9)</sup>	$C_{o(er)}$	-	111	-	$\text{pF}$	$V_{GS} = 0\text{ V}, V_{DS} = 0 \dots 500\text{ V}$
Effective output capacitance, time related <sup>10)</sup>	$C_{o(tr)}$	-	158	-	$\text{pF}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0 \dots 500\text{ V}$

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.  
 Stray inductances and coupling capacitances must be minimized.  
 For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD} = 500\text{ V}$ , $V_{GS} = 0/18\text{ V}$ , $I_D = 27.0\text{ A}$ , $R_{G,ext} = 1.8\ \Omega$ , $L_{stray} = 15\text{ nH}$ ; see table 10
Rise time	$t_r$	-	8	-	ns	
Turn-off delay time	$t_{d(off)}$	-	17	-	ns	
Fall time	$t_f$	-	7	-	ns	
Turn-ON switching losses <sup>11)</sup>	$E_{on}$	-	47	-	$\mu\text{J}$	
Turn-OFF switching losses <sup>11)</sup>	$E_{off}$	-	24	-	$\mu\text{J}$	
Total switching losses <sup>11)</sup>	$E_{tot}$	-	71	-	$\mu\text{J}$	

<sup>8)</sup> Maximum specification is defined by calculated six sigma upper confidence bound.

<sup>9)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 500 V.

<sup>10)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 500 V.

<sup>11)</sup> MOSFET used in half-bridge configuration without external diode. Parameter verified by characterization according to IEC 60747-8.

**Table 7 Gate charge characteristics**

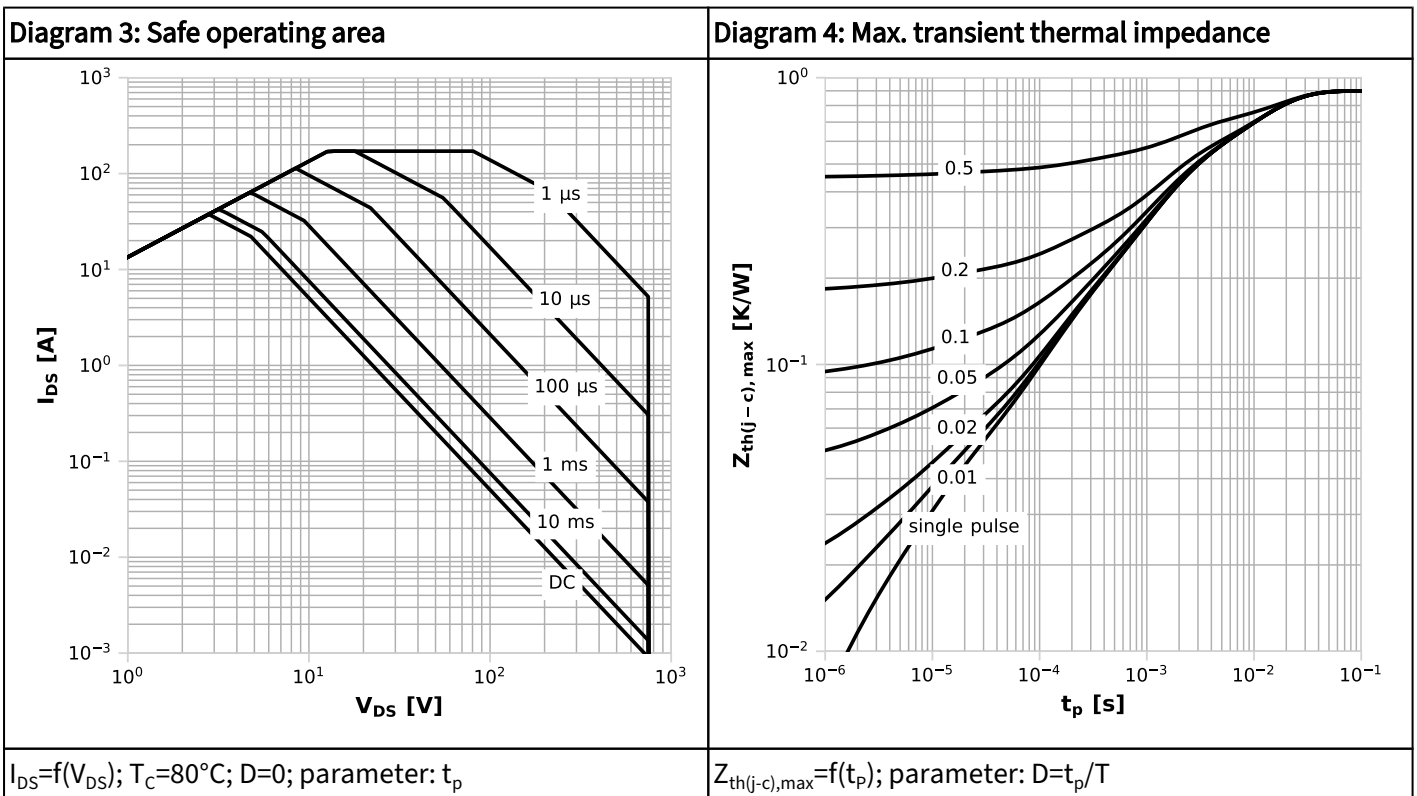
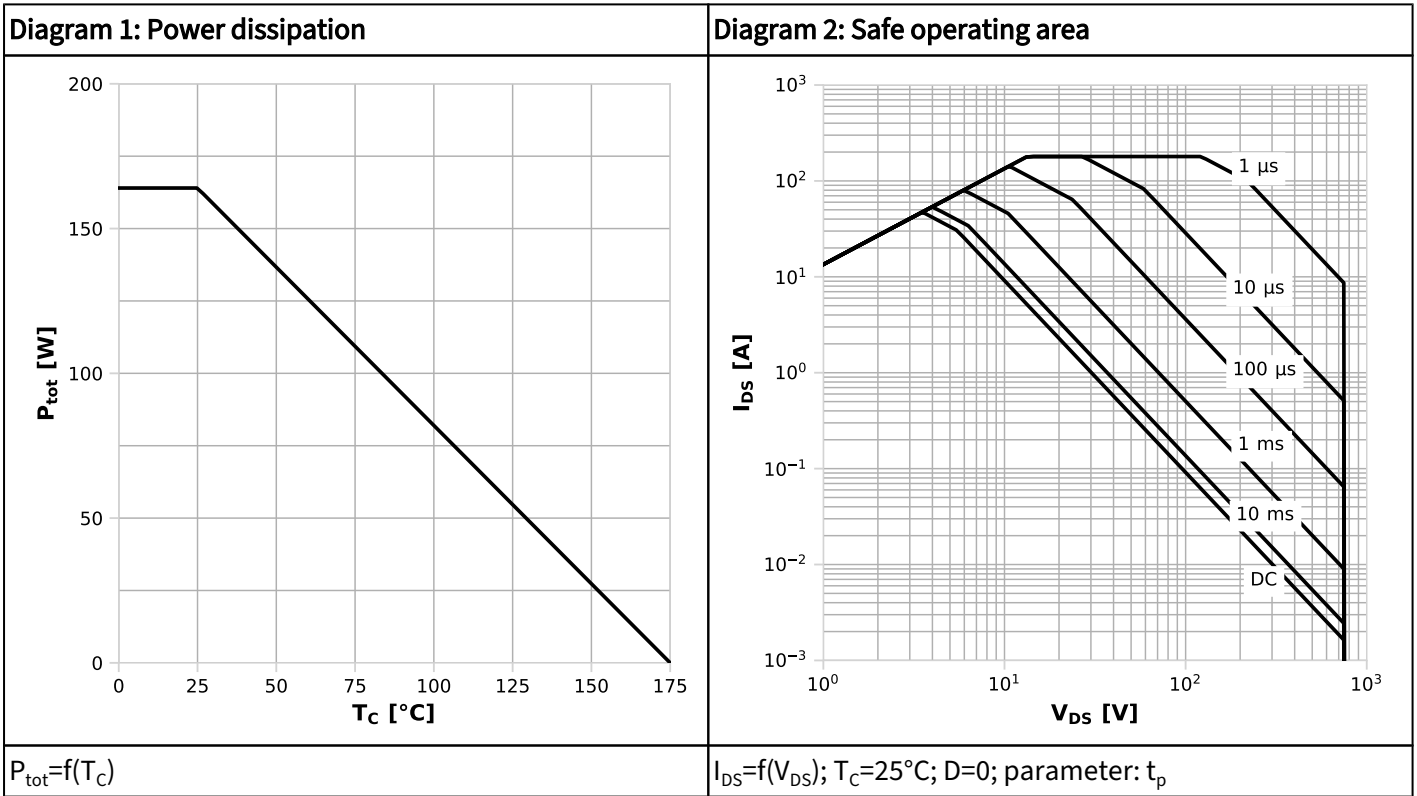
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	9.4	-	nC	$V_{DD} = 500\text{ V}$ , $I_D = 27.0\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	$Q_{GD}$	-	7.9	-		
Total gate charge	$Q_G$	-	37	-		

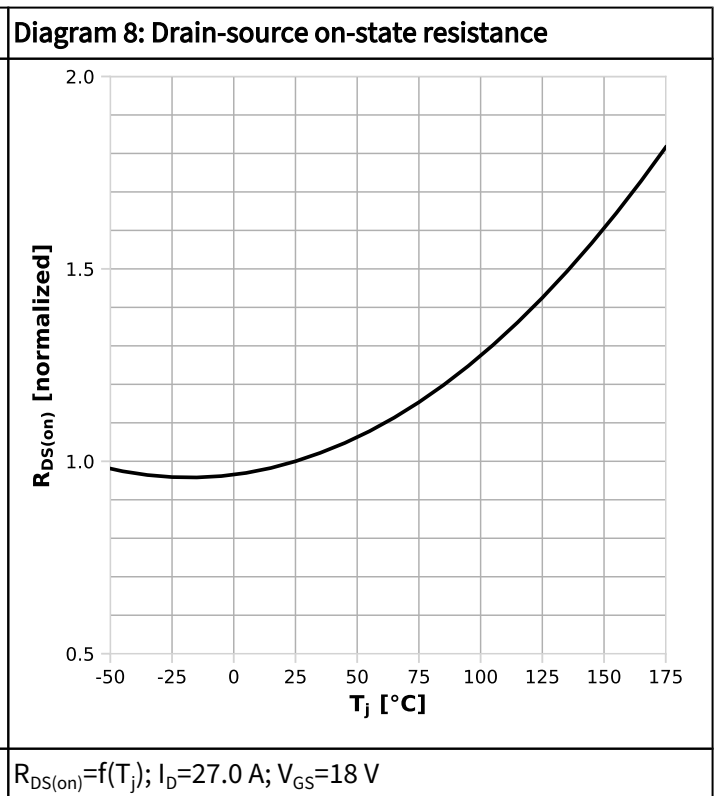
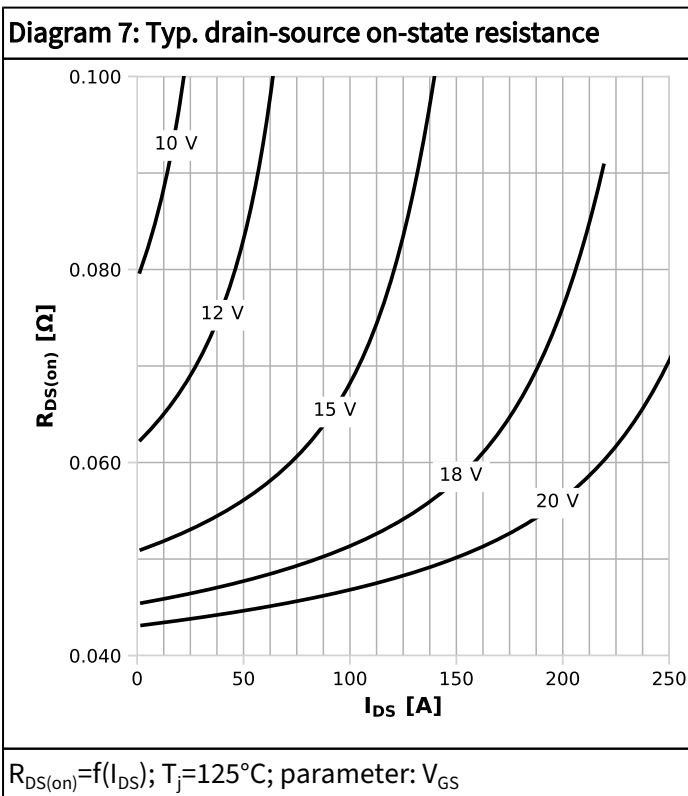
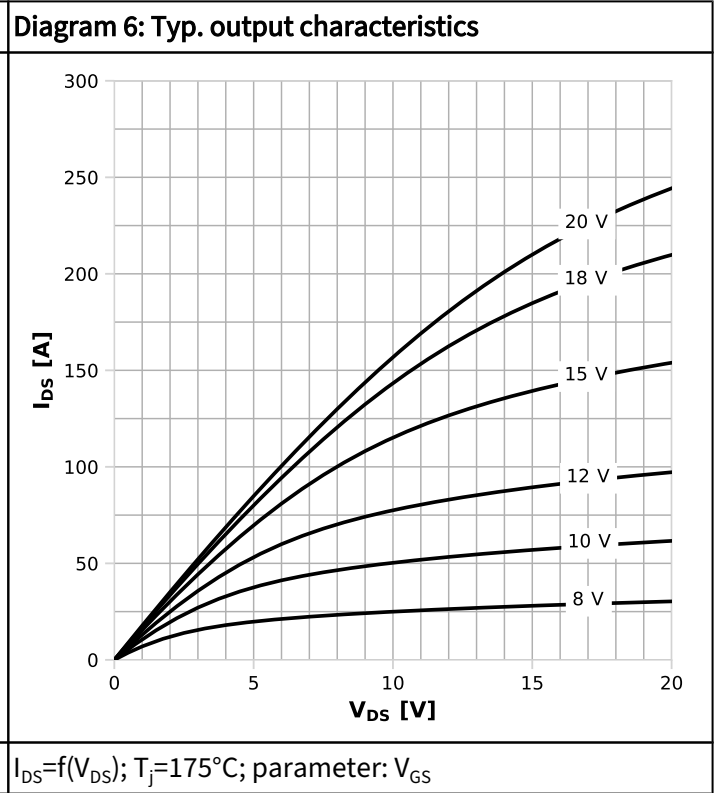
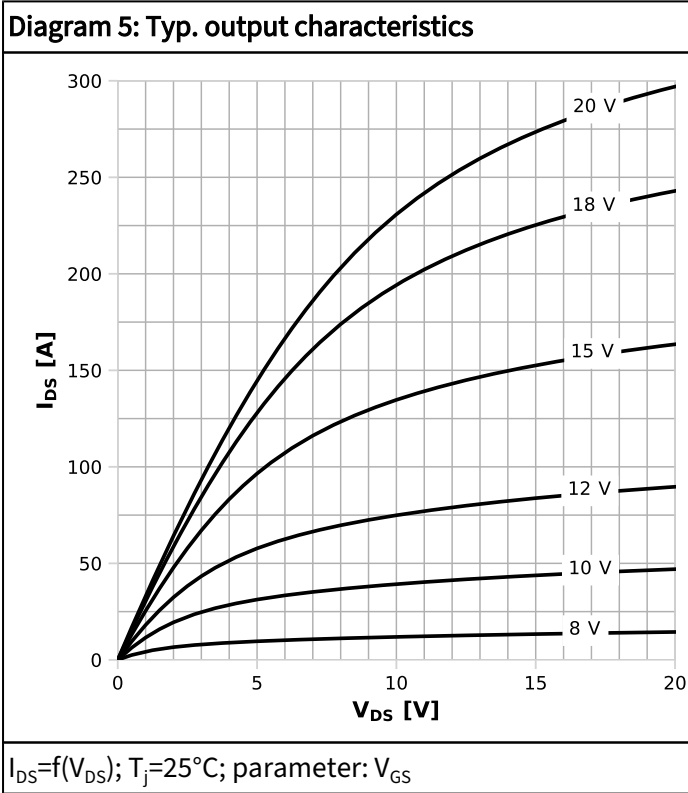
**Table 8 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	$V_{SD}$	-	4.1	5.0	V	$V_{GS} = 0\text{ V}$ , $I_S = 27.0\text{ A}$ , $T_j = 25^\circ\text{C}$
			3.8	-		$V_{GS} = 0\text{ V}$ , $I_S = 27.0\text{ A}$ , $T_j = 175^\circ\text{C}$
MOSFET forward recovery time	$t_{fr}$	-	8	-	ns	$V_{DD} = 500\text{ V}$ , $I_S = 27.0\text{ A}$ , $di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET forward recovery charge <sup>12)</sup>	$Q_{fr}$	-	89	-	nC	
MOSFET peak forward recovery current	$I_{frm}$	-	23	-	A	

<sup>12)</sup>  $Q_{fr}$  includes  $Q_{oss}$

## 5 Electrical characteristics diagrams





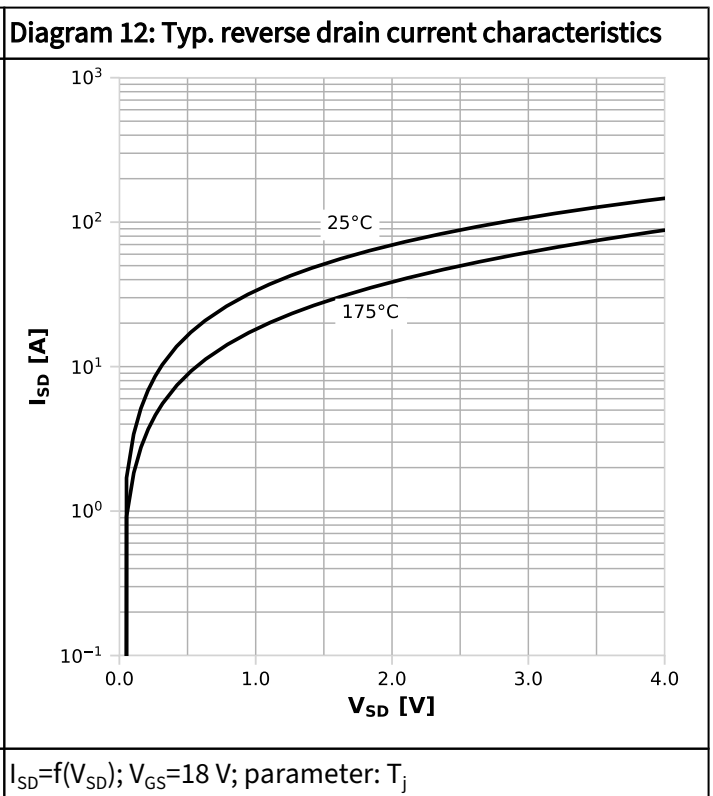
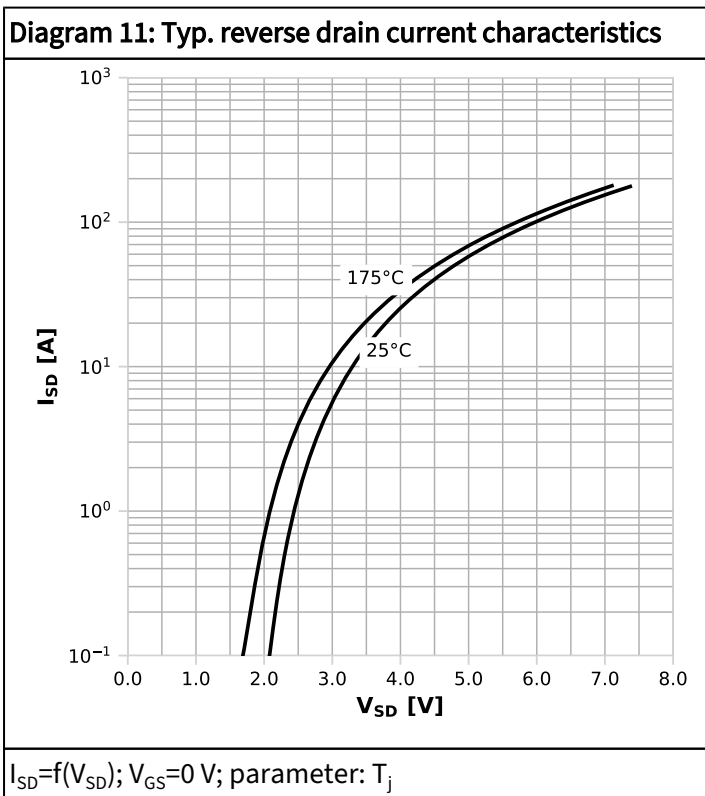
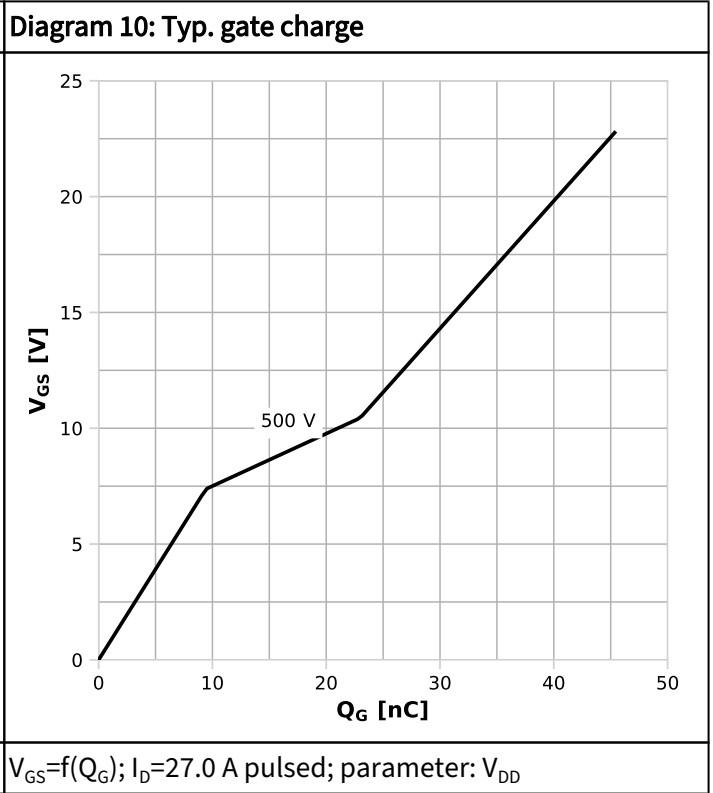
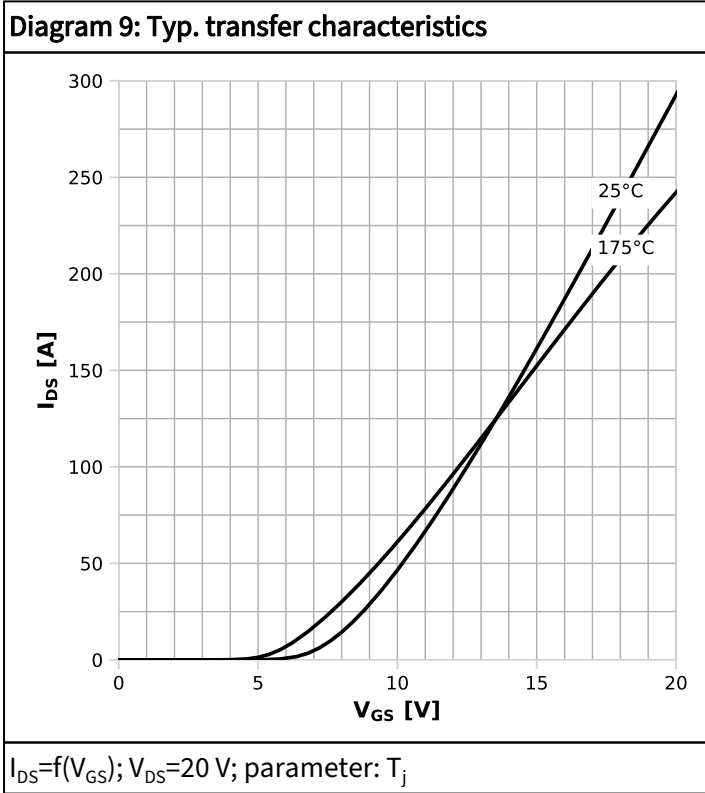
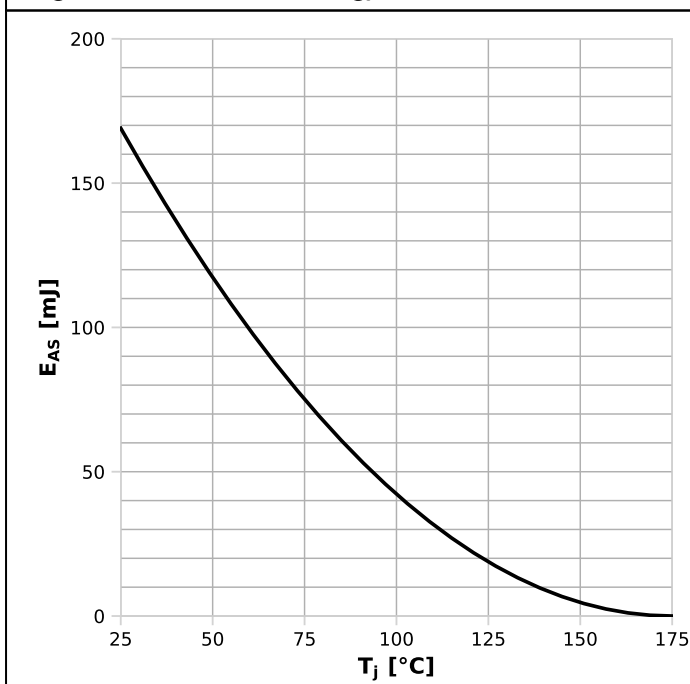
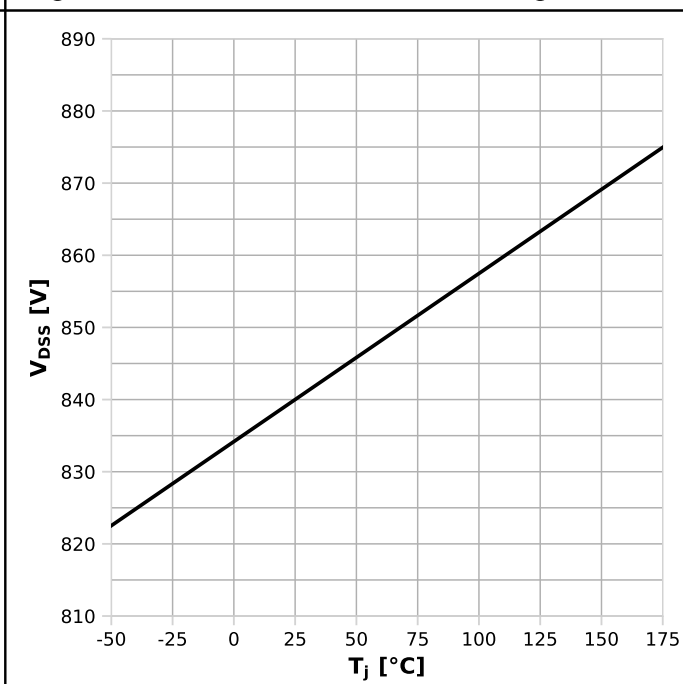


Diagram 13: Avalanche energy



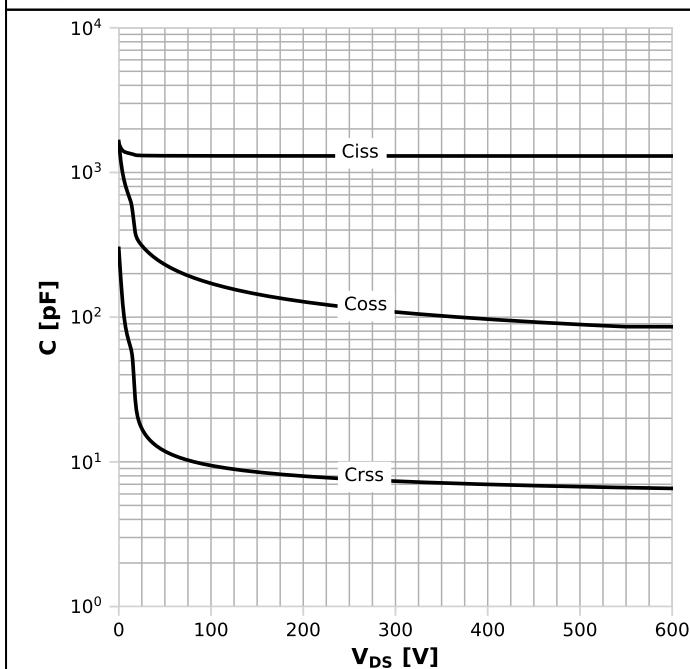
$E_{AS}=f(T_j); I_D=6.3\text{ A}; V_{DD}=50\text{ V}$

Diagram 14: Drain-source breakdown voltage



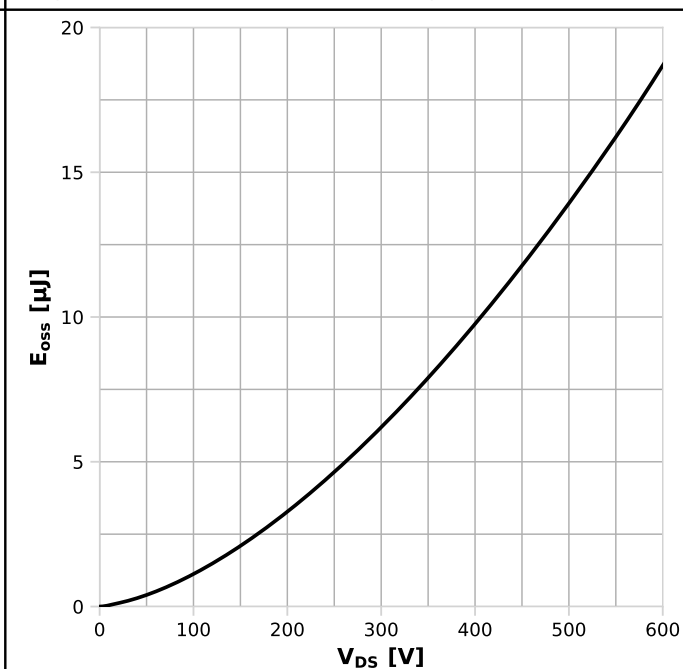
$V_{DSS}=f(T_j); I_D=0.59\text{ mA}$

Diagram 15: Typ. capacitances



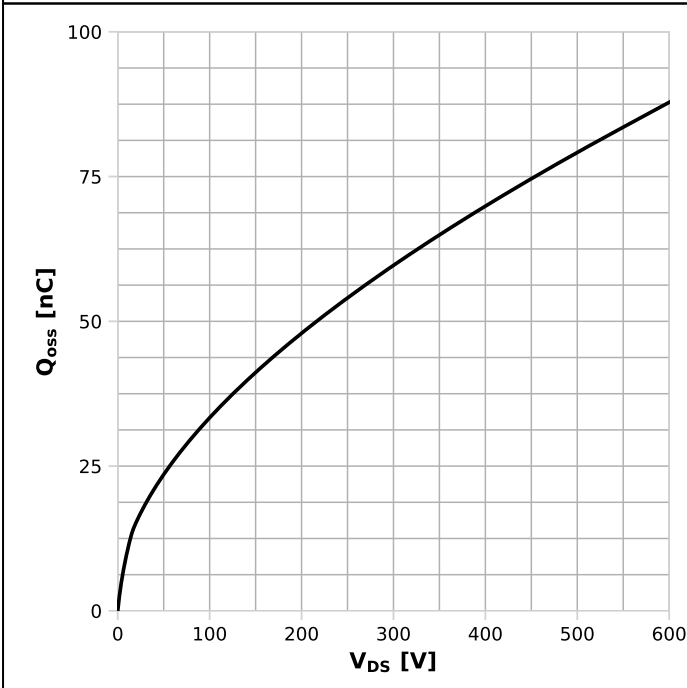
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 16: Typ. Coss stored energy



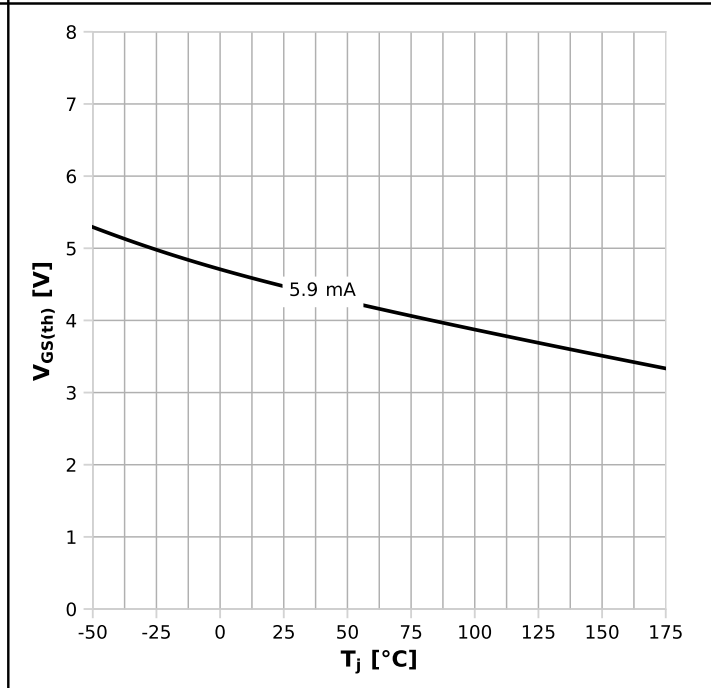
$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



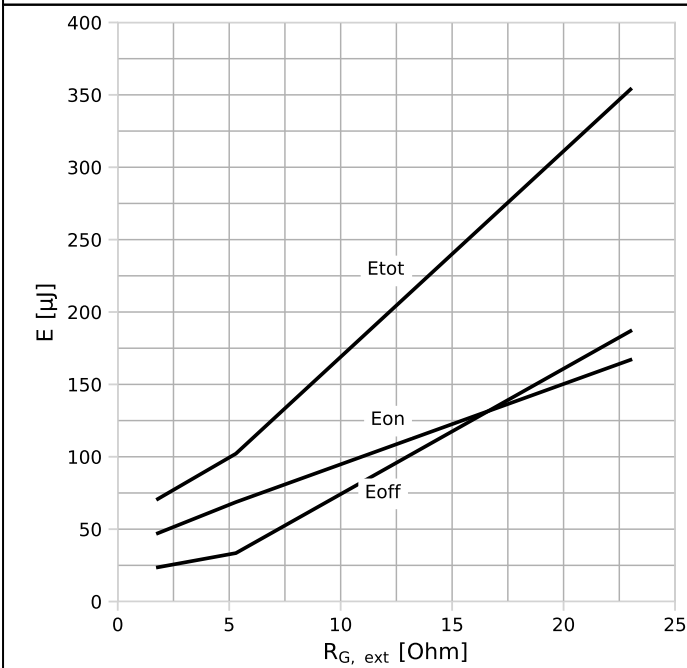
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. gate threshold voltage



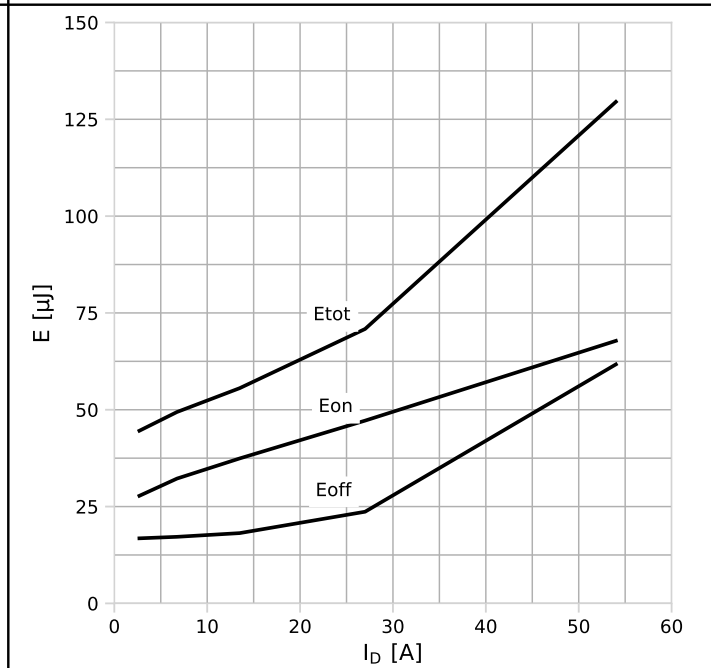
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS};$  parameter:  $I_D$

Diagram 19: Typ. Switching Losses vs R<sub>G,ext</sub>

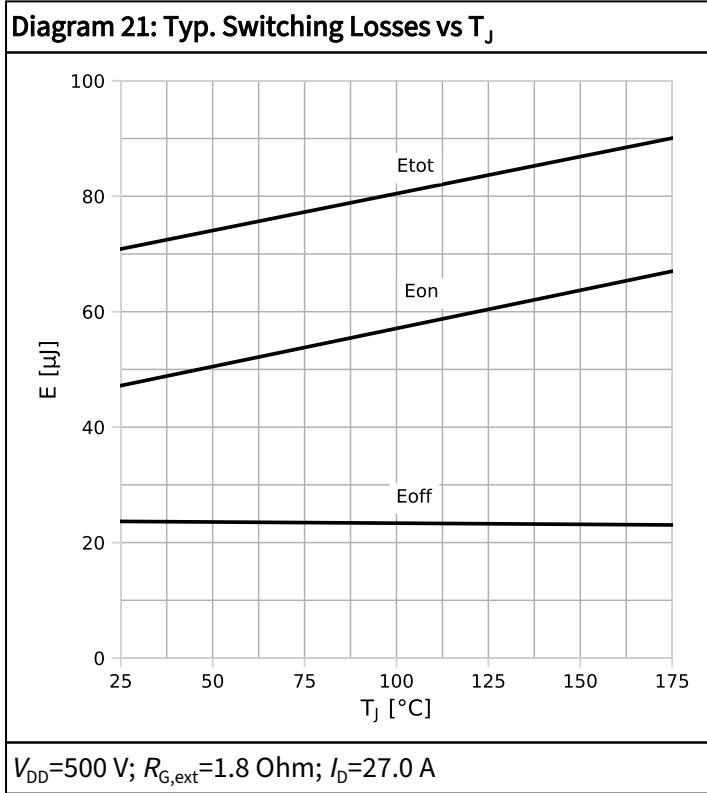


$V_{DD}=500\text{ V}; I_D=27.0\text{ A}; T_J=25^\circ\text{C}$

Diagram 20: Typ. Switching Losses vs switching current

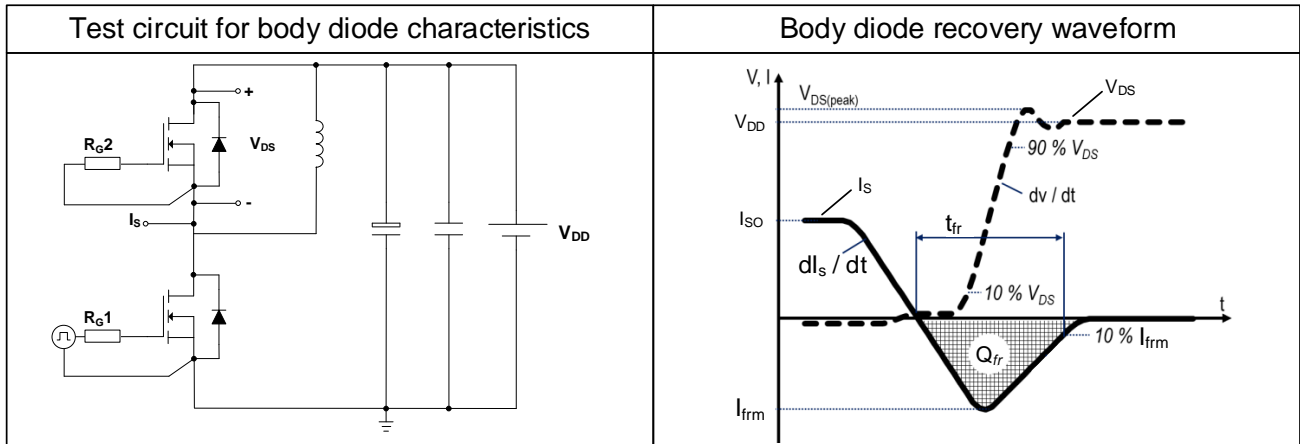


$V_{DD}=500\text{ V}; R_{G,ext}=1.8\text{ Ohm}; T_J=25^\circ\text{C}$

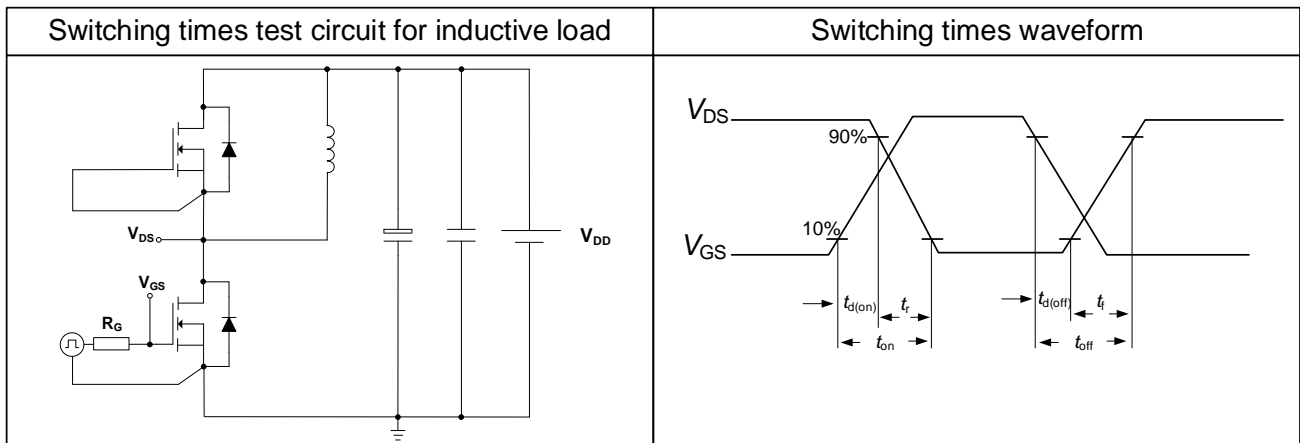


## 6 Test circuits

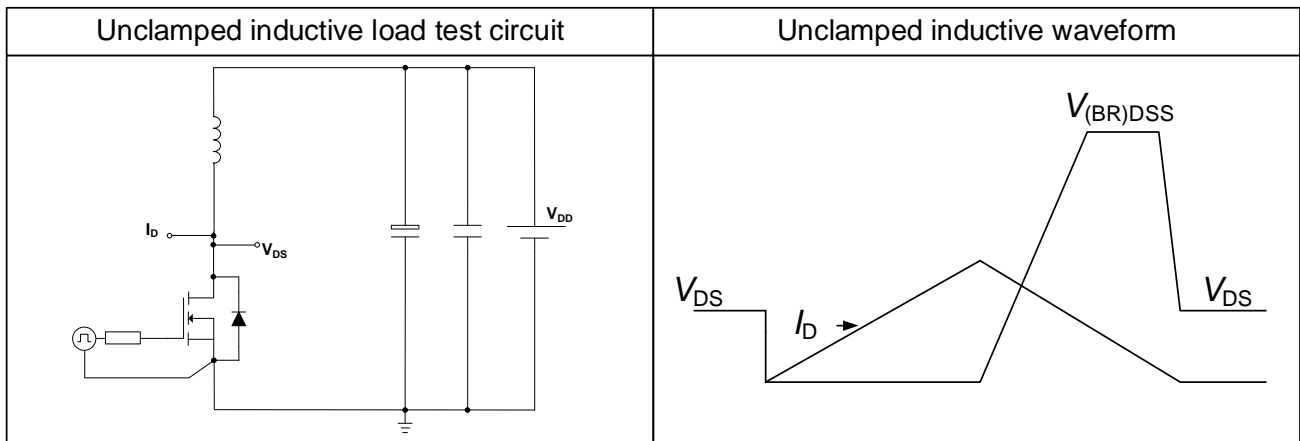
**Table 9 Body diode characteristics**



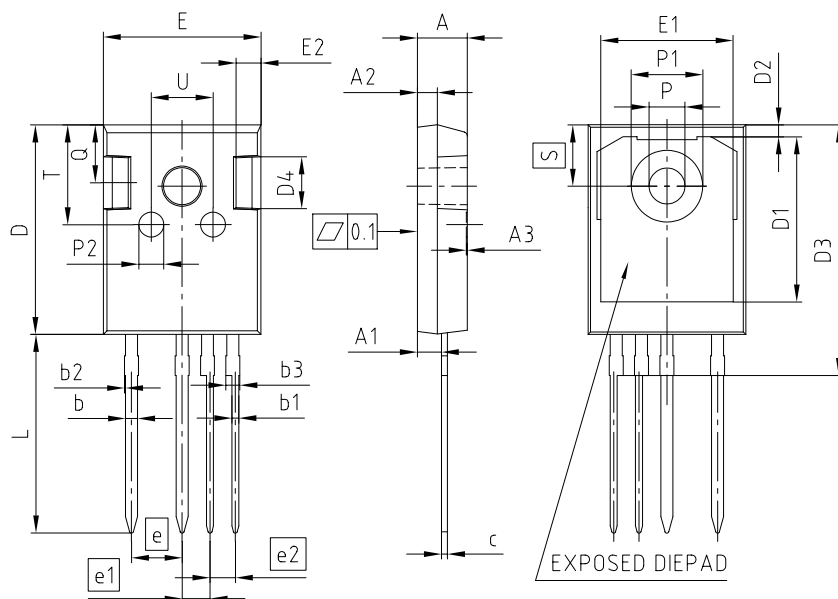
**Table 10 Switching times**



**Table 11 Unclamped inductive load**



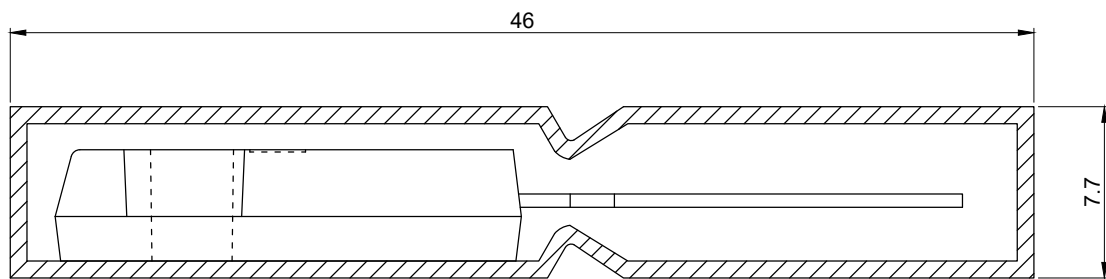
## 7 Package outlines




NOTES:  
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER: PG-TO247-4-U02					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	E	15.70	15.90
A1	2.31	2.51	E1	13.10	13.50
A2	1.90	2.10	E2	2.40	2.60
A3	0.05	0.25	e	5.08	
b	1.10	1.30	e1	2.79	
b1	0.65	0.79	e2	2.54	
b2	---	0.20	N	4	
b3	1.34	1.44	L	19.80	20.10
c	0.58	0.66	øP	3.50	3.70
D	20.90	21.10	øP1	7.40	
D1	16.25	16.85	øP2	2.40	2.60
D2	1.05	1.35	Q	5.60	6.00
D3	24.97	25.27	S	6.15	
D4	4.90	5.10	T	9.80	10.20
			U	6.00	6.40

Figure 1 Outline PG-TO247-4, dimensions in mm



All dimensions are in units mm  
The drawing is in compliance with ISO 128-30, Projection Method 1 [  ]

**Figure 2** Packaging variant PG-TO247-4, dimensions in mm

## 8 Appendix A

Table 12 Related links

- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Simulation Model](#)
- [IFX Design tools](#)

## Revision history

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IMZA75R033M2H

### Revision 2025-12-19, Rev. 1.0

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Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-12-19	Release of final version

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