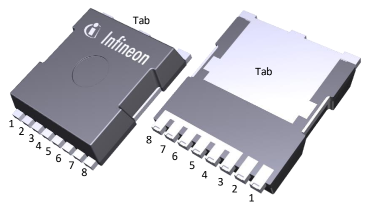
CoolSiC™

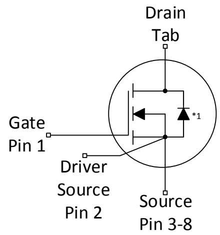
440V CoolSiC™ G2 MOSFET with extended V_{DS}

TOLL



Features

- Ideal for high frequency switching and synchronous rectification
- Commutation robust fast body diode with low Q_{fr}
- Low $R_{DS(on)}$ dependency on temperature
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5 V
- Recommended gate driving voltage 0 V to 18 V
- .XT interconnection technology for best-in-class thermal performance
- 100% avalanche tested
- Fully tested in production to guarantee extended $V_{(BR)DSS}$



*1: Internal body diode

Potential applications

- Application specific MOSFET designed to power AI
- High Power SMPS for server, datacenter and telecom rectifiers

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	440	V
$V_{DS,tr}$	455	V
$R_{DS(on),typ}$	11.3	mΩ
I_D	144	A
Q_{oss}	138	nC
E_{oss}	9.9	µJ
Q_G	85	nC

Part number	Package	Marking	Related links
IMT44R011M2H	PG-HSOF-8	44R011M2	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	144	A	V_{GS}=18 V, T_C=25 °C
				102		V_{GS}=18 V, T_C=100 °C
				13.4		V_{GS}=18 V, T_A=25 °C, R_{THJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	432	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	220	mJ	I_D=37.1 A, R_{GS}=25 Ω
Avalanche energy, repetitive	E_{AR}			1.1		
Gate source voltage (static)	$V_{GS,DC}$	-7	-	23	V	-
Gate source voltage (transient)	$V_{GS,AC}$	-10	-	25	V	t_{pulse}≤500 ns, duty cycle≤1%
Power dissipation	P_{tot}	-	-	429	W	T_C=25 °C
				3.8		T_A=25 °C, R_{THJA}=40 °C/W [2]
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information.

[4] See Diagram 19 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.35	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5)]	R_{thJA}	-	-	40	°C/W	-

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

4 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	440	-	-	V	V_{GS}=0 V, I_D=1.33 mA
Transient drain-source breakdown voltage [6]	$V_{(BR)DSS,tr}$	455	-	-	V	V_{GS}=0 V, I_D=13.3 mA, t_{pulse}≤10 ms, duty cycle≤50%
Gate threshold voltage [7]	$V_{GS(th)}$	3.5	4.5	5.6	V	V_{DS}=V_{GS}, I_D=13.3 mA
Zero gate voltage drain current	I_{DSS}	-	1	75	µA	V_{DS}=400 V, V_{GS}=0 V, T_j=25 °C
			2	-		V_{DS}=400 V, V_{GS}=0 V, T_j=175 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	11.3	14.4	mΩ	V_{GS}=18 V, I_D=37.1 A, T_j=25 °C
			16.3	-		V_{GS}=18 V, I_D=37.1 A, T_j=175 °C
			13.7	-		V_{GS}=15 V, I_D=37.1 A, T_j=25 °C
Gate resistance	R_G	-	2.3	3.5	Ω	-

6) Guaranteed by design, rated for transient startup overvoltages to comply with IPC-9592B derating guidelines.

7) Tested after 1ms pulse at V_{GS} = +20V.

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2900	3770	pF	V_{GS}=0 V, V_{DS}=200 V, f=1 MHz
Output capacitance	C_{oss}		410	-		
Reverse transfer capacitance	C_{rss}		33	-		
Effective output capacitance, energy related [8]	$C_{o(er)}$	-	494	-	pF	V_{GS}=0 V, V_{DS}=0...200 V
Effective output capacitance, time related [9]	$C_{o(tr)}$	-	690	-	pF	I_D=constant, V_{GS}=0 V, V_{DS}=0...200 V
Turn-on delay time	$t_{d(on)}$	-	15.8	-	ns	V_{DD}=200 V, V_{GS}=0...18 V, I_D=37.1 A, $R_{G,ext}$=1.8 Ω
Rise time	t_r		18.3			
Turn-off delay time	$t_{d(off)}$	-	29.8	-	ns	V_{DD}=200 V, V_{GS}=18...0 V, I_D=37.1 A, $R_{G,ext}$=1.8 Ω
Fall time	t_f		9.3			

8) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 200 V.

9) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 200 V.

Table 7 Gate Charge Characteristics [10)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	23	-	nC	V_{DD}=200 V, I_D=37.1 A, V_{GS}=0 to 18 V
Gate to drain charge	Q_{gd}		17.5			
Gate charge total	Q_g		85			
Gate charge total, sync. FET	$Q_{g(sync)}$	-	79	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 18 V
Output charge	Q_{oss}	-	138	-	nC	V_{DS}=200 V, V_{GS}=0 V
Output Energy	E_{oss}		9.9		µJ	

10) As per JEP192, Guidelines for Gate Charge (Q_G) Test Method for SiC MOSFET.

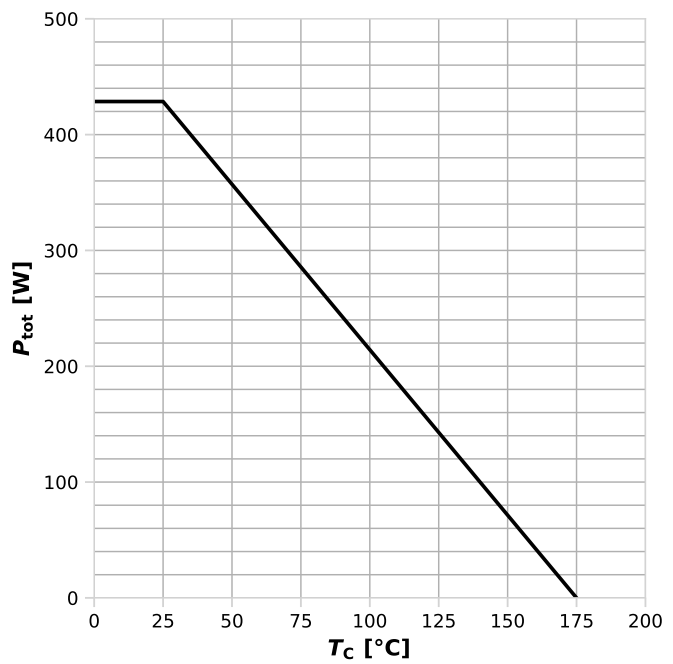
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	67	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	432	A	T_C=25 °C, t_{pulse}≤250 ns
Diode forward voltage	V_{SD}	-	3.5	4.3	V	V_{GS}=0 V, I_S=37.1 A, T_j=25 °C
MOSFET forward recovery time	t_{fr}	-	18.2	-	ns	V_R=200 V, I_S=37.1 A, di_S/dt=1000 A/µs
			12.8			V_R=200 V, I_S=37.1 A, di_S/dt=4000 A/µs
MOSFET forward recovery charge [11)]	Q_{fr}	-	86	-	nC	V_R=200 V, I_S=37.1 A, di_S/dt=1000 A/µs
			220			V_R=200 V, I_S=37.1 A, di_S/dt=4000 A/µs

11) Q_{fr} includes Q_{oss}. Refer to Table 10 for test setup.

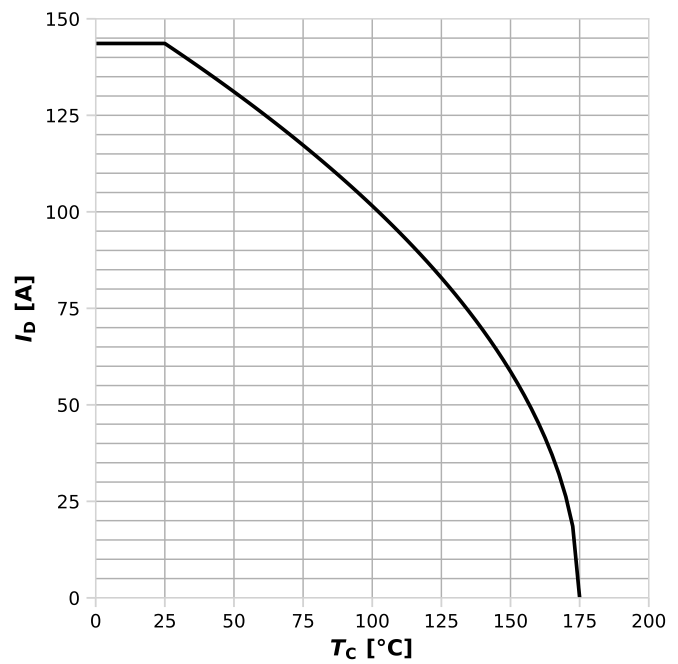
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



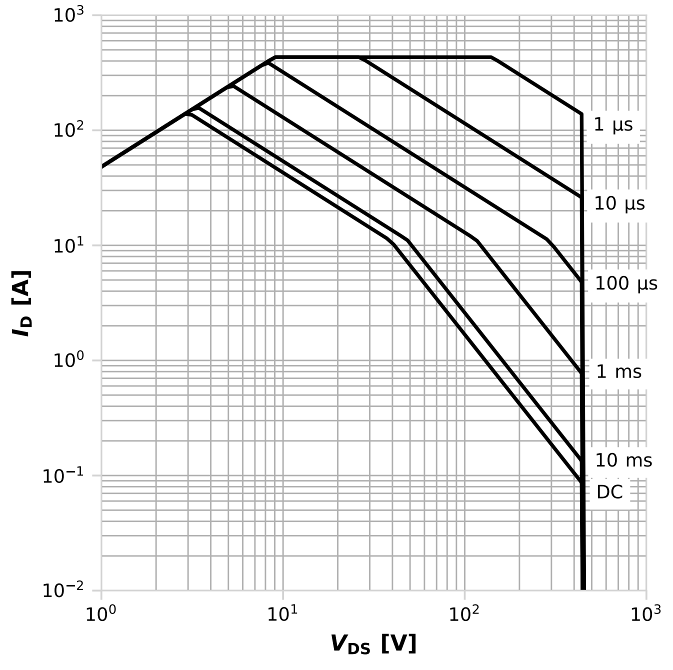
P_{tot}=f(T_C)

Diagram 2: Drain current



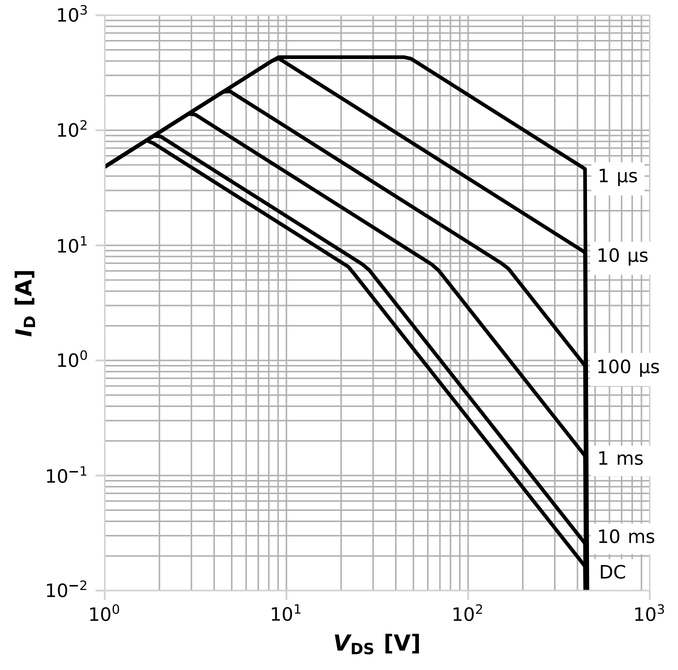
I_D=f(T_C); V_{GS}≥18 V

Diagram 3: Safe operating area



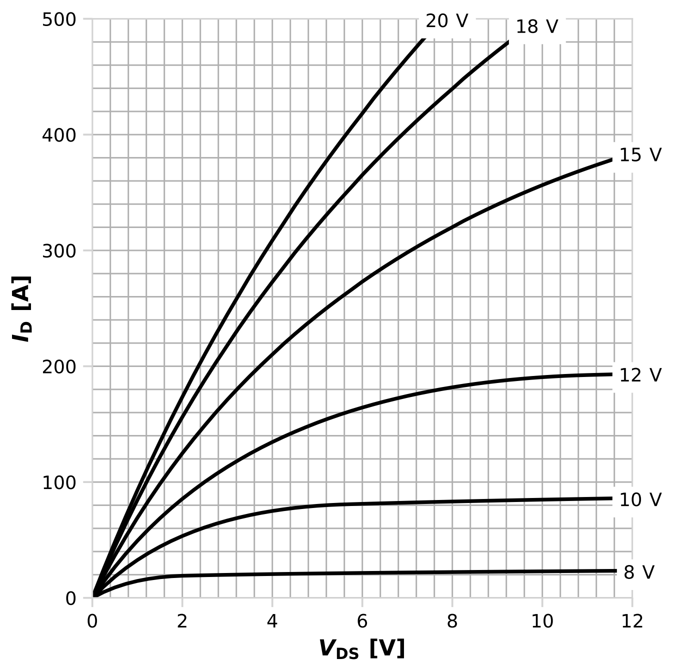
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Safe operating area



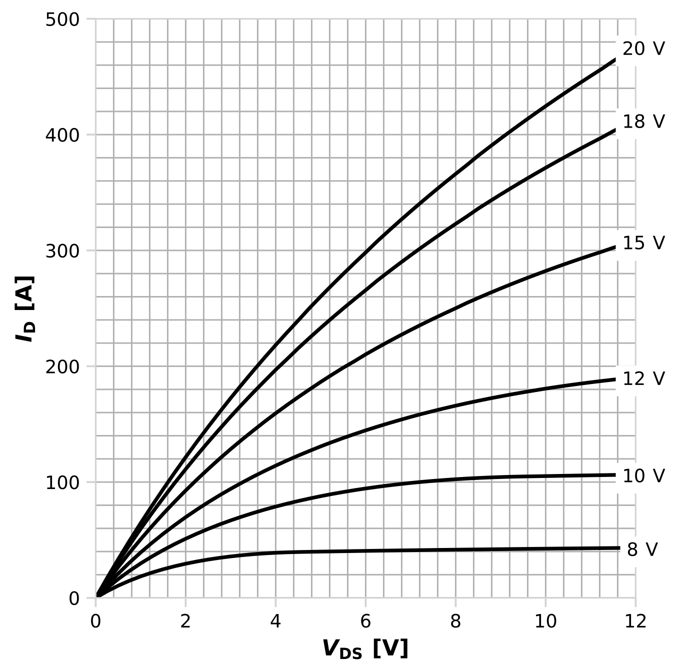
I_D=f(V_{DS}); T_C=125 °C; D=0; parameter: t_p

Diagram 5: Typ. output characteristics



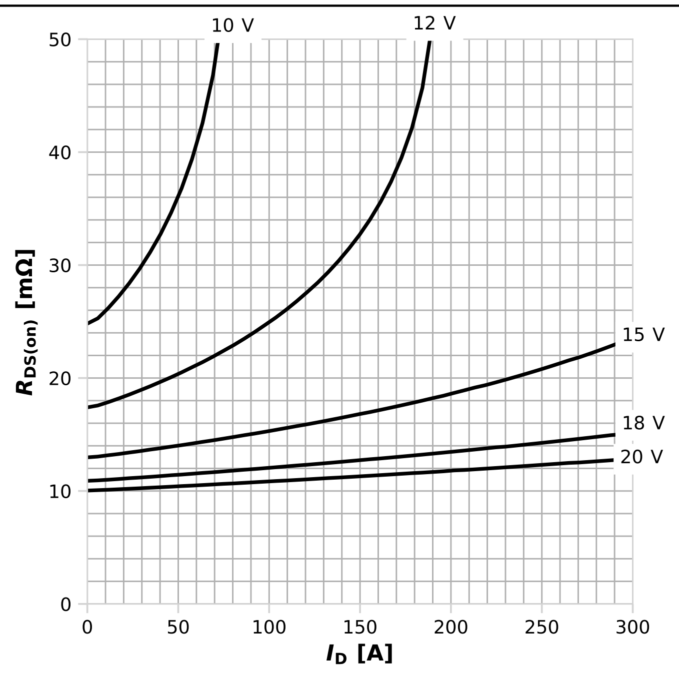
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



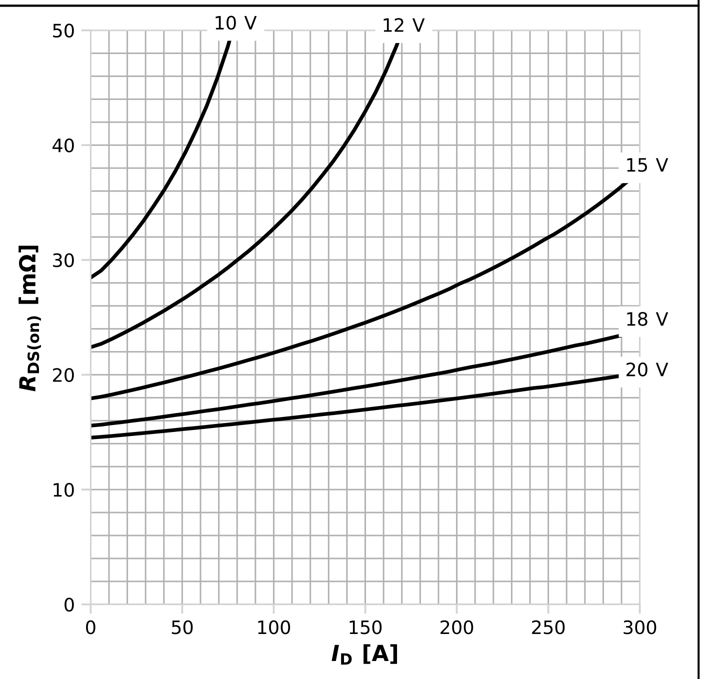
I_D=f(V_{DS}), T_j=175 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on resistance



$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(I_D), T_j=175 °C; parameter: V_{GS}

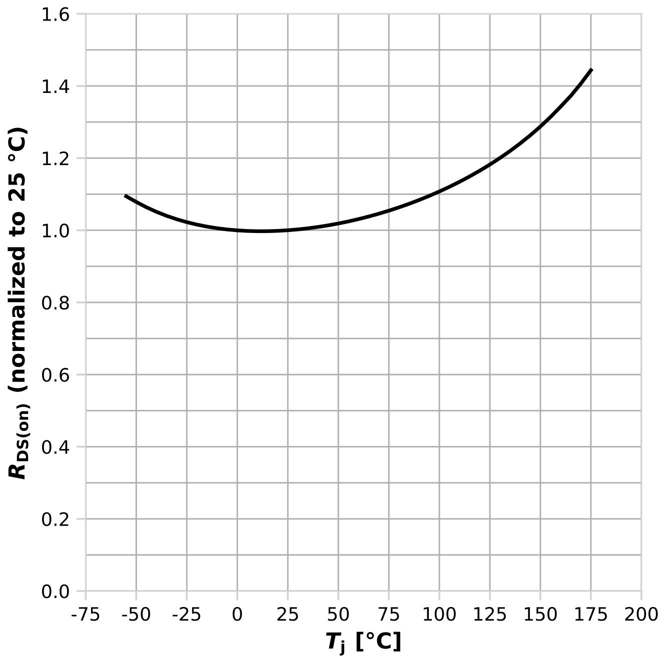
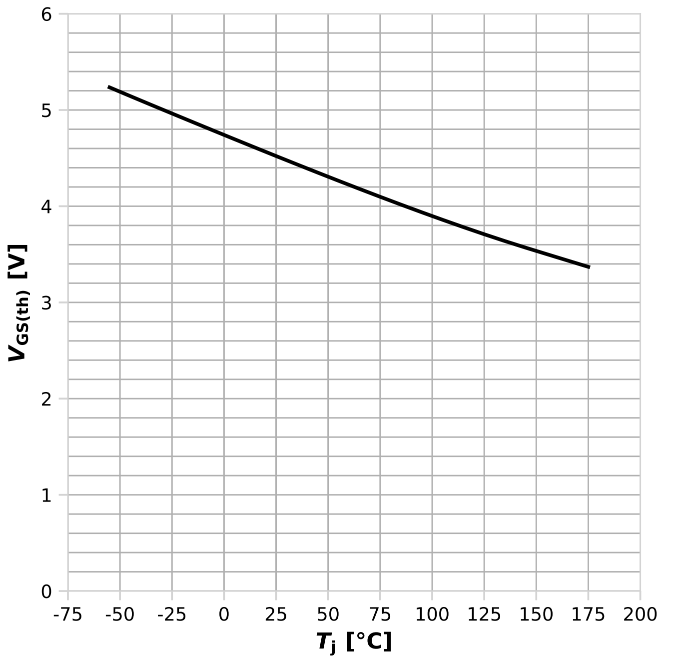
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=37.1 A, V_{GS}=18 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}, I_D=13.3 mA

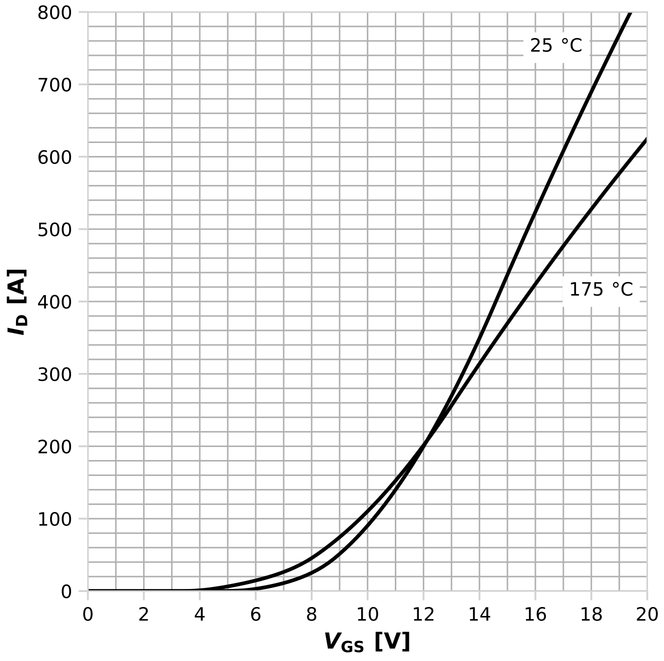
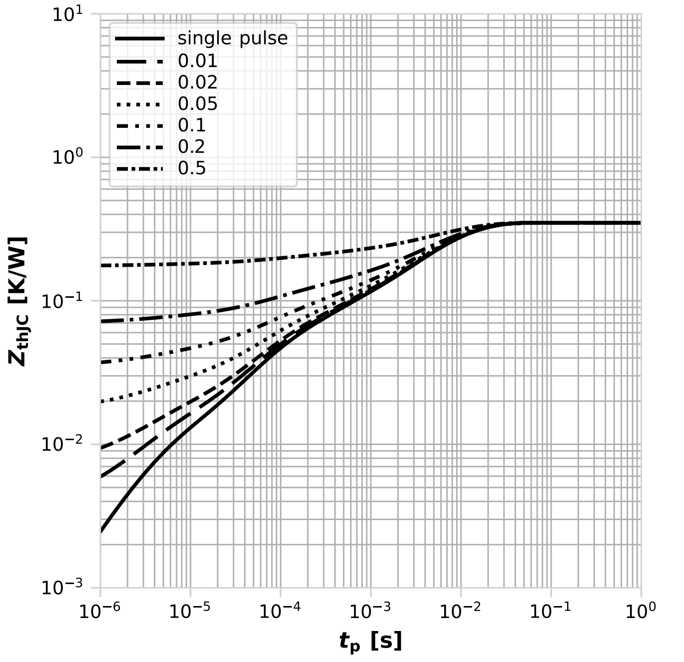
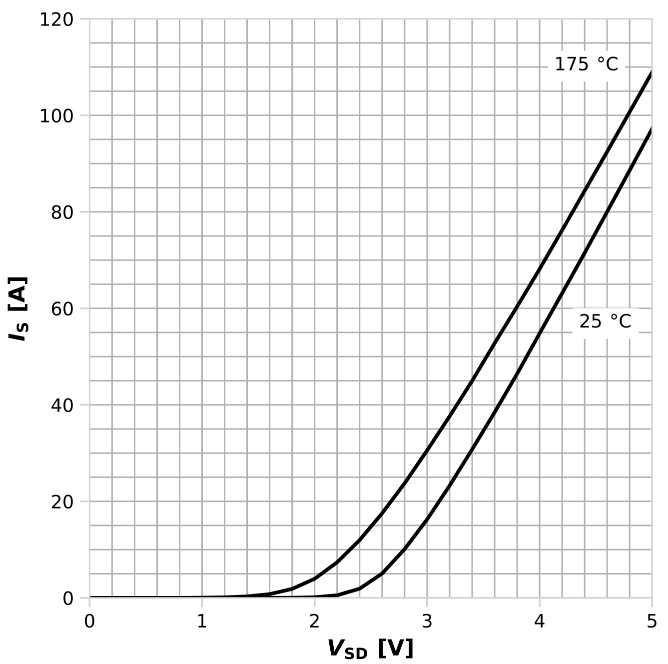
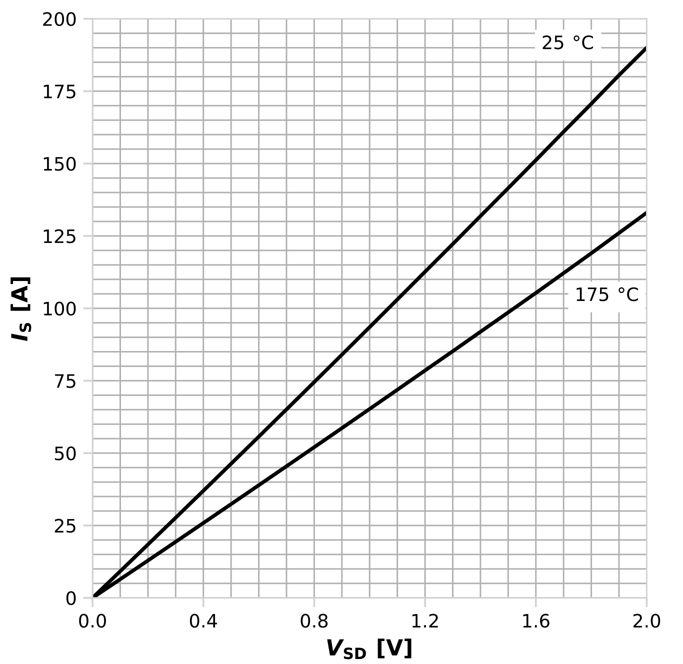
Diagram 11: Typ. transfer characteristics	Diagram 12: Max. transient thermal impedance
	
I_D=f(V_{GS}), $\lvert V_{DS}\rvert$>2$\lvert I_D\rvert R_{DS(on)max}$; parameter: T_j	Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 13: Reverse output characteristics



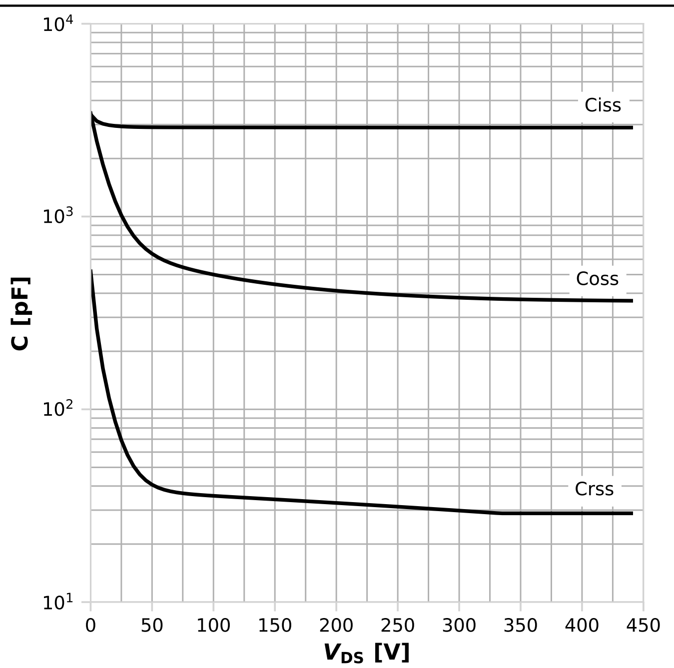
I_F=f(V_{SD}), V_{GS}=0 V; parameter: T_j

Diagram 14: Reverse output characteristics



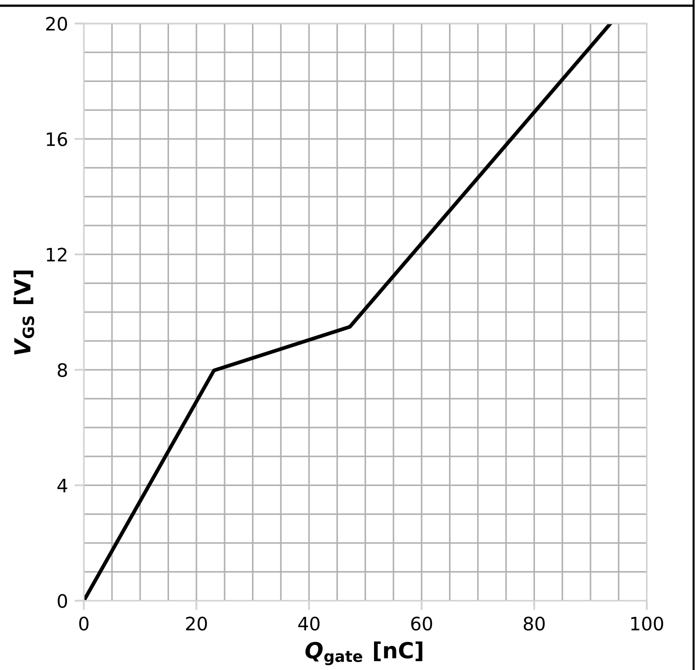
I_F=f(V_{SD}), V_{GS}=18 V; parameter: T_j

Diagram 15: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 16: Typ. gate charge



V_{GS}=f(Q_{gate}), V_{DD}=200 V, I_D=37.1 A pulsed, T_j=25 °C

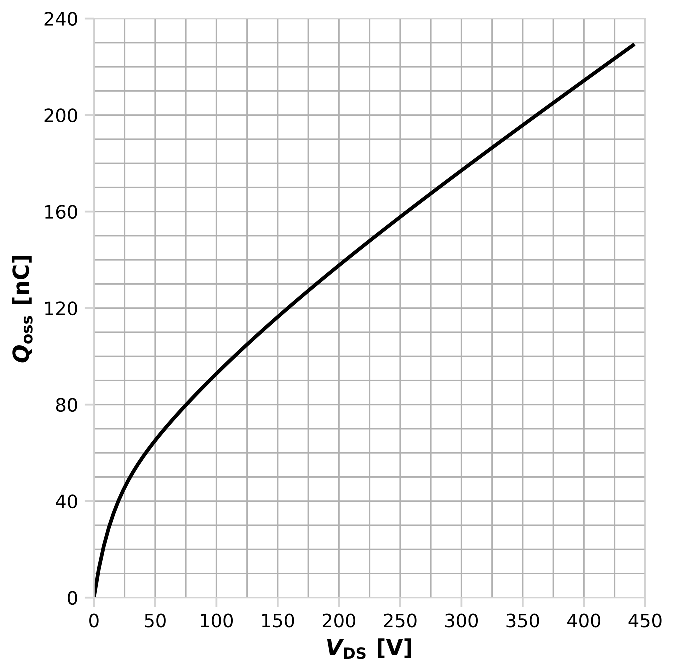
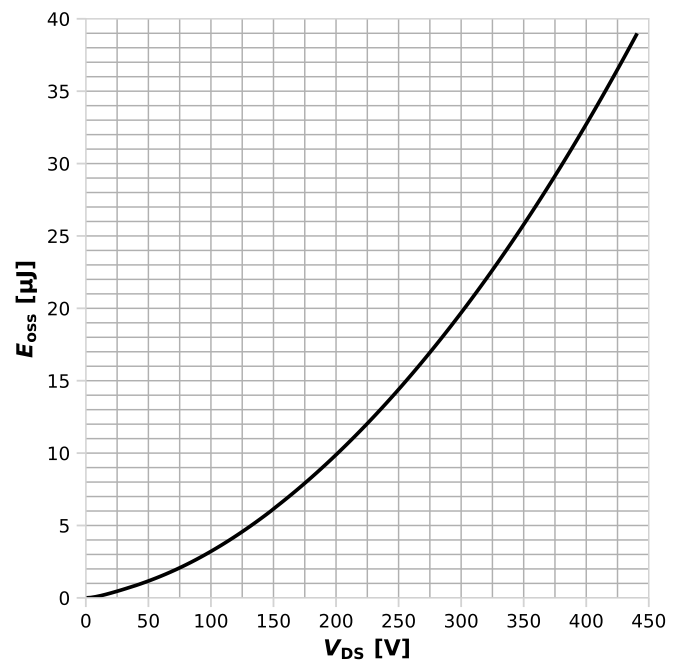
Diagram 17: Typ. output charge	Diagram 18: Typ. output energy
	
Q_{oss}=f(V_{DS}), V_{GS}=0 V	E_{oss}=f(V_{DS}), V_{GS}=0 V

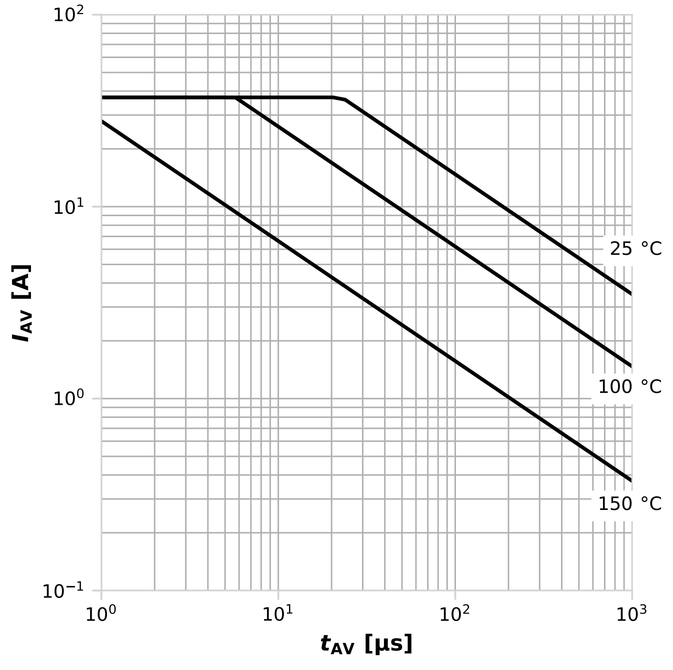
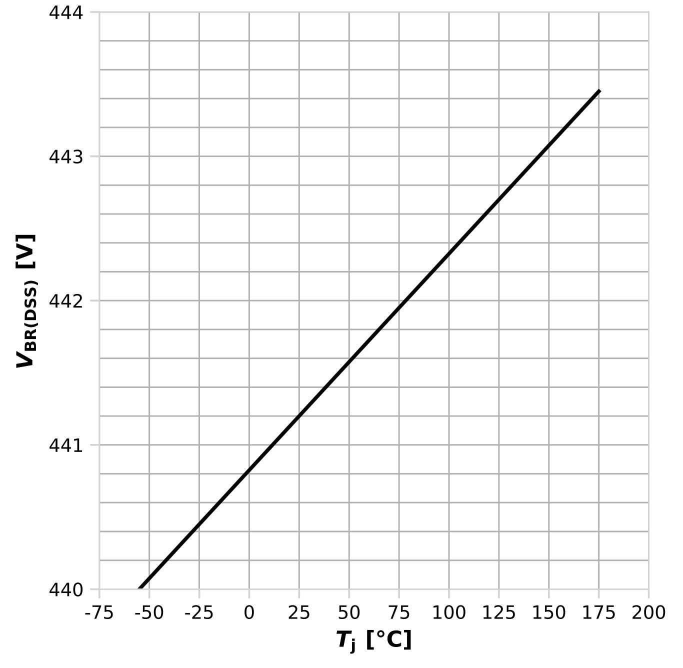
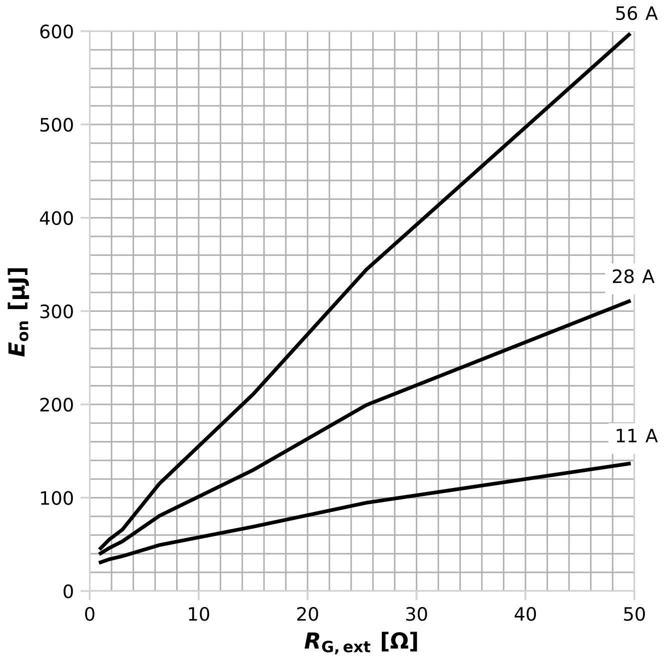
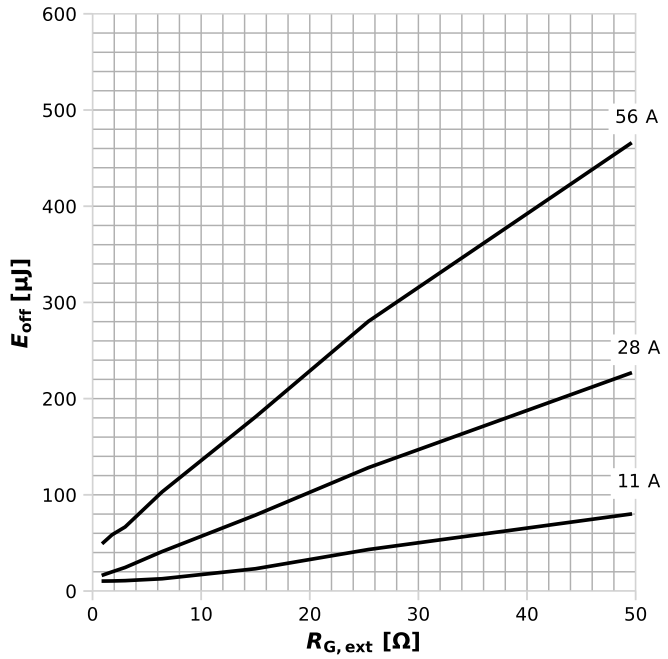
Diagram 19: Avalanche characteristics	Diagram 20: Min. drain-source breakdown voltage
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	$V_{BR(DSS)}$=f(T_j); I_D=1.33 mA

Diagram 21: Typ. turn-on switching losses



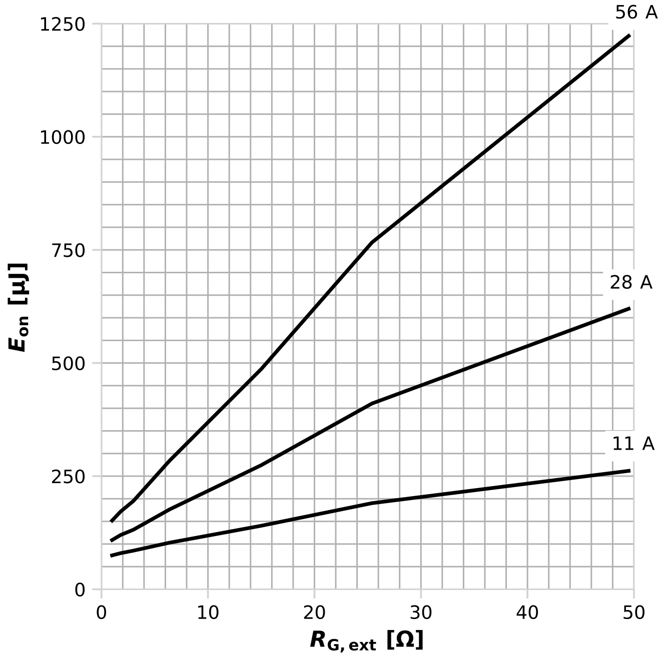
E_{on}=f($R_{g,ext}$), V_{DD}=200 V, V_G=0...18 V; parameter: I_D

Diagram 22: Typ. turn-off switching losses



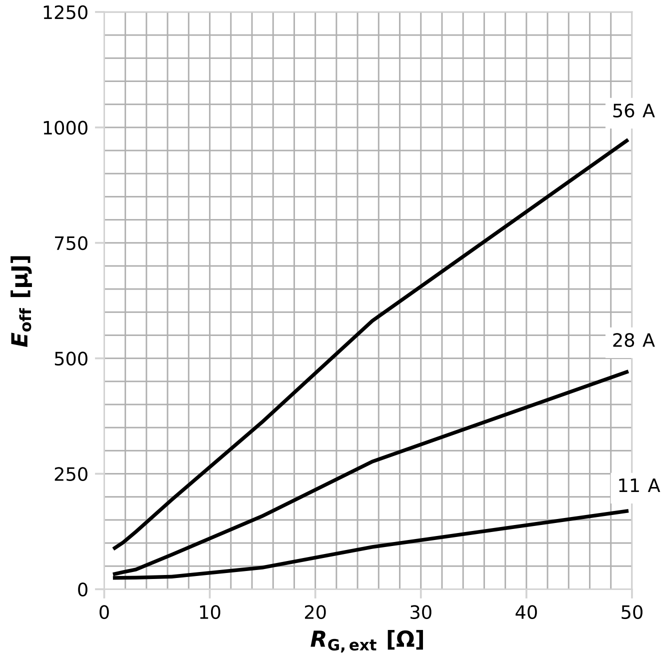
E_{off}=f($R_{g,ext}$), V_{DD}=200 V, V_G=18...0 V; parameter: I_D

Diagram 23: Typ. turn-on switching losses



E_{on}=f($R_{g,ext}$), V_{DD}=320 V, V_G=0...18 V; parameter: I_D

Diagram 24: Typ. turn-off switching losses



E_{off}=f($R_{g,ext}$), V_{DD}=320 V, V_G=18...0 V; parameter: I_D

6 Test circuits

Table 9 Switching times

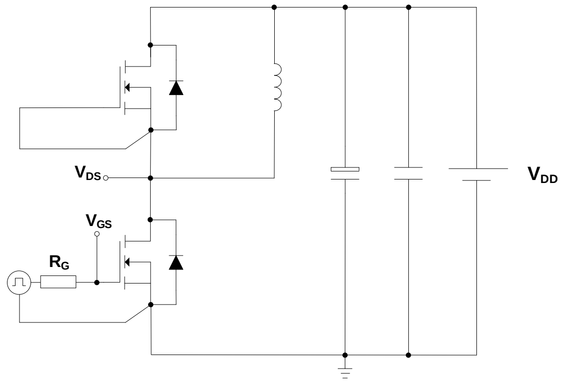
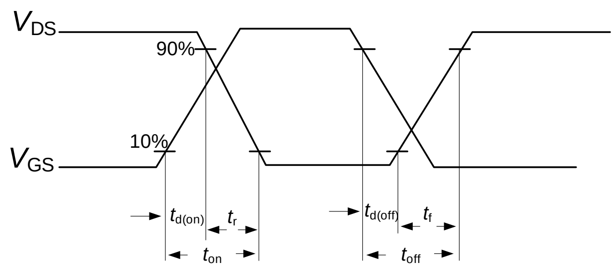
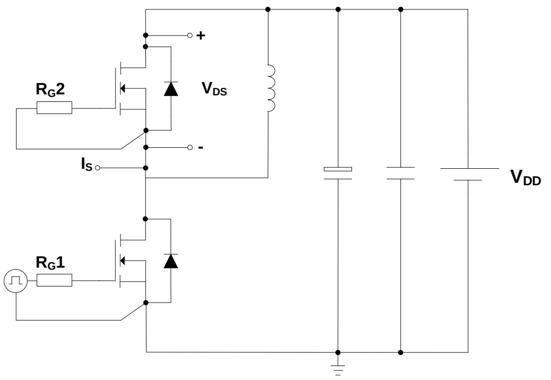
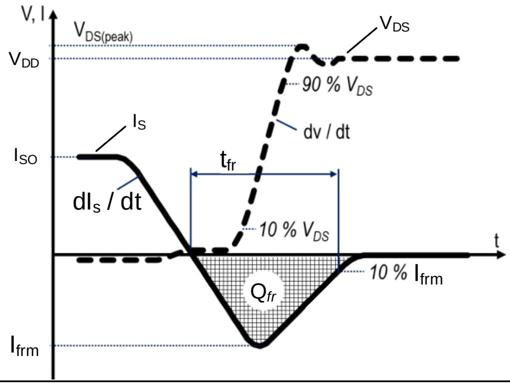
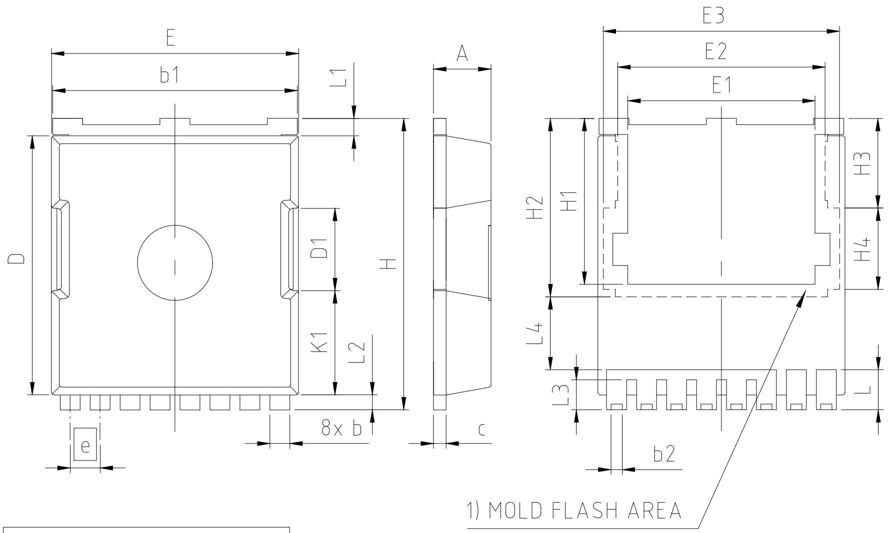
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Body diode characteristics

Test circuit for body diode characteristics	Body diode recovery waveform
	

7 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

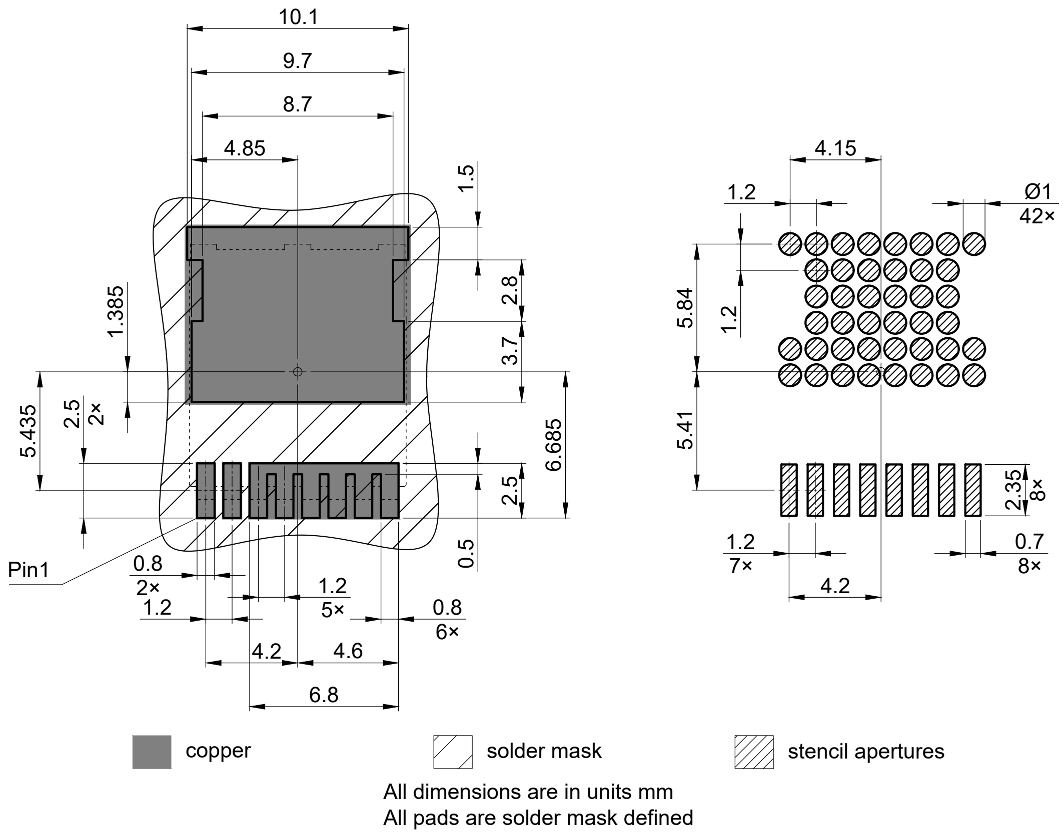
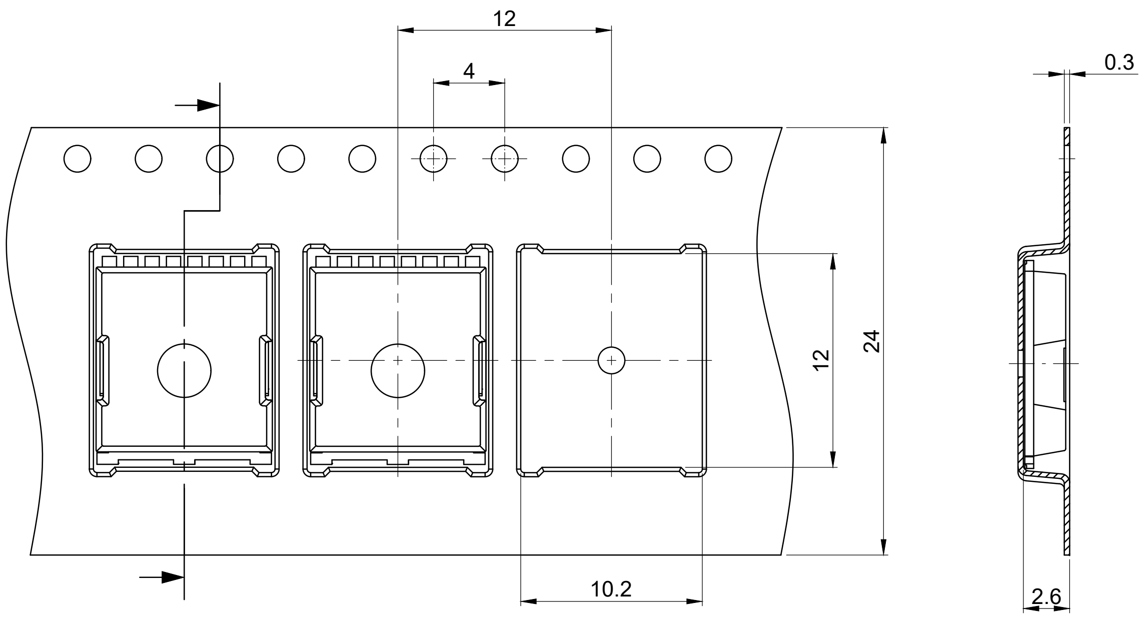


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

Revision history

IMT44R011M2H

Revision 2025-05-27, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-05-27	Release of final datasheet

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