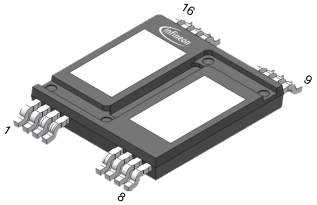
Final datasheet

CoolSiC™ 1200 V SiC MOSFET G2 : Silicon Carbide MOSFET with top side cooling and .XT technology

Features



- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 40 A at T_c = 25°C
- $R_{DS(on)}$ = 40 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Internal layout optimized for fast switching
- Very low switching losses
- Overload operation up to T_{vj} = 200°C
- Short circuit withstand time 2 µs
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance
- Suitable Infineon gate drivers can be found under https://www.infineon.com/gdfinder

Halogen-free

Green

Lead-free

RoHS

Potential applications

- General purpose drives (GPD)
- EV Charging
- Online UPS / Industrial UPS
- String inverter
- Servo drives

Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

Pin definition:

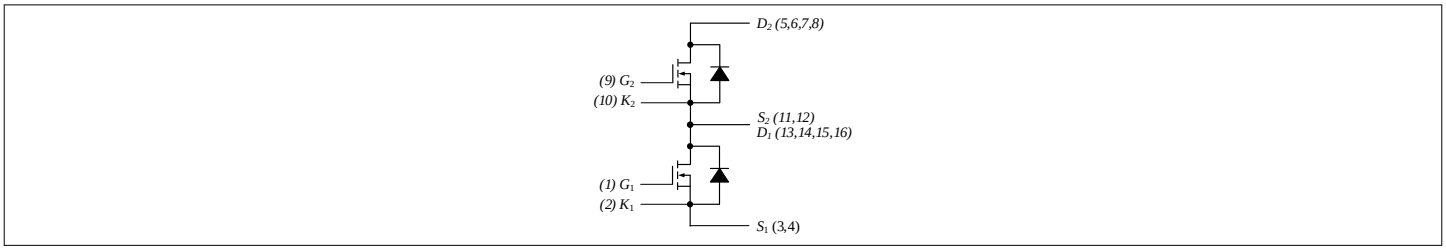
• 13-16 (5-8) & Case 1(2) – Drain D1(D2)

• 3,4 (11,12) – Source S1(S2)

• 2(10) – Kelvin sense K1(K2)

• 1(9) – Gate G1(G2)

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction



Type	Package	Marking
IMSQ120R040M2HH	PG-HDSOP-16-U03	12M2H040

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	Reflow soldering (MSL2 according to JEDEC J-STD-020)			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.4	0.52	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	V_{GS}=18 V	T_c = 25 °C	57	A
			T_c = 100 °C	40	
Peak drain current, t_p limited by $T_{vj(max)}$ [1)]	I_{DM}	V_{GS}=18 V		120	A
Gate-source voltage, max. transient voltage [2)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage	V_{GS}			-7...23	V
Avalanche energy, single pulse	E_{AS}	I_D = 18 A, V_{DD} = 50 V, L = 1.4 mH, $T_{vj(start)}$ = 25 °C		220	mJ
Avalanche energy, repetitive	E_{AR}	I_D = 18 A, V_{DD} = 50 V, L = 7.2 µH, $T_{vj(start)}$ = 25 °C		1.1	mJ
Short-circuit withstand time	t_{SC}	$V_{DD} \leq 800$ V, $V_{DS,peak} < 1200$ V, $V_{GS(on)}$ = 15 V, $T_{vj(start)}$ = 25 °C		2	µs
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		T_c = 25 °C	290	W
			T_c = 100 °C	140	

1) Verified by the design/characterization.
2) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 18 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		40		mΩ
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		49.4		
			T_{vj} = 150 °C, $V_{GS(on)}$ = 18 V		81	107	
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		94		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 5.5 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.1	V
			T_{vj} = 175 °C		3.2		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			20	µA
			T_{vj} = 175 °C		2.6		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = -10 V			-120	nA
			V_{GS} = 23 V			120	
Forward transconductance	g_{fs}	I_D = 18 A, V_{DS} = 20 V			12		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			6.5		Ω
Input capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			1310		pF
Output capacitance	C_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			55		pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			5		pF
C_{oss} stored energy	E_{oss}	Calculated based on C_{oss} = f(V_{DD})			23		µJ
Output charge	Q_{oss}	Calculated based on C_{oss} = f(V_{DD})			85.2		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on E_{oss}			72		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on Q_{oss}			106		pF
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, turn-on pulse			36		nC

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, turn-on pulse			8.2		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, turn-on pulse			8.8		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		8		ns
			T_{vj} = 175 °C		5.9		
Rise time	t_r	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		5		ns
			T_{vj} = 175 °C		4.4		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		15.7		ns
			T_{vj} = 175 °C		18.3		
Fall time	t_f	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		6.6		ns
			T_{vj} = 175 °C		7.8		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		140		µJ
			T_{vj} = 175 °C		270		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		45		µJ
			T_{vj} = 175 °C		61		
Total switching energy[1)]	E_{tot}	V_{DD} = 800 V, I_D = 18 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 9 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		231		µJ
			T_{vj} = 175 °C		462		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[2)]				200	°C

1) Including E_{fr}
2) Up to 5000 cycles. Maximum ΔT limited to 100 K.

***Note**: The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.*

Characteristics at T_{vj} = 25°C, unless otherwise specified.

3 Body diode (MOSFET)

Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} ≥ 25 °C		1200	V
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	V_{GS} = 0 V		120	A

Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 18 A, V_{GS} = 0 V	T_{vj} = 25 °C		4.2	5.5	V
			T_{vj} = 100 °C		4.11		
			T_{vj} = 175 °C		4.05		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 18 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		120		nC
			T_{vj} = 175 °C		480		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 18 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		18.9		A
			T_{vj} = 175 °C		33.4		
MOSFET forward recovery energy	E_{fr}	V_{DD} = 800 V, I_{SD} = 18 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		46		µJ
			T_{vj} = 175 °C		131		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[1)]				200	°C

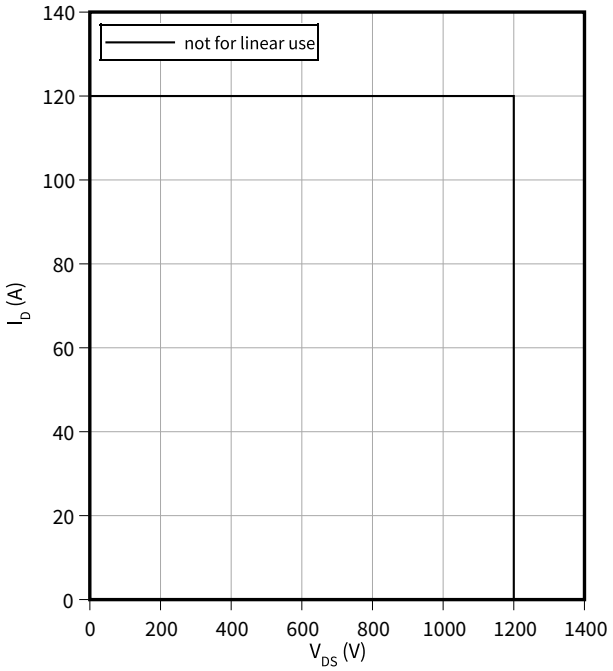
1) Up to 5000 cycles. Maximum ΔT limited to 100 K.

4 Characteristics diagrams

Reverse bias safe operating area (RBSOA)

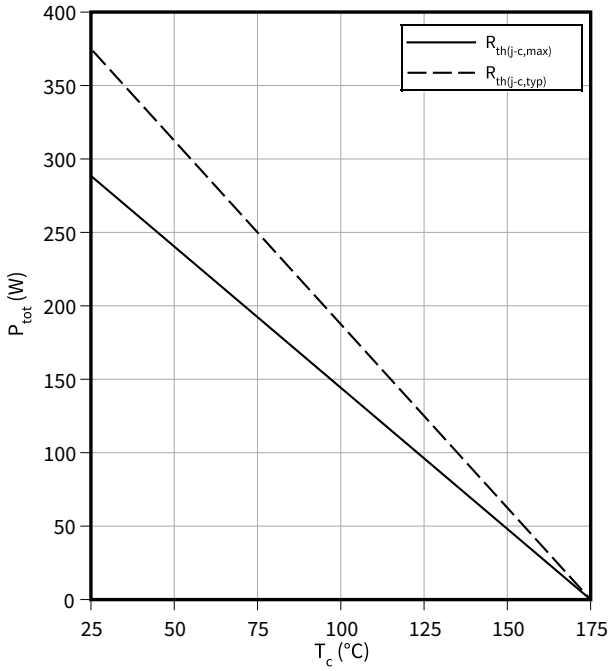
$I_D = f(V_{DS})$

V_{GS} = 0/18 V, T_c = 25 °C, $T_{vj} \leq$ 200 °C



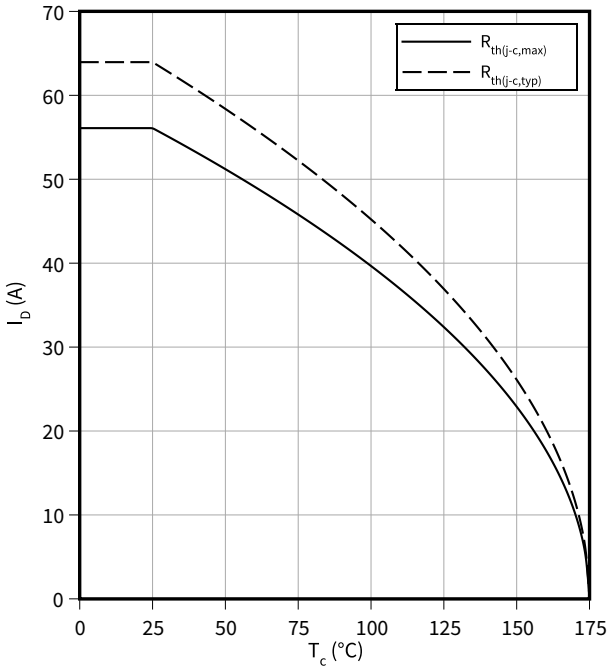
Power dissipation as a function of case temperature

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

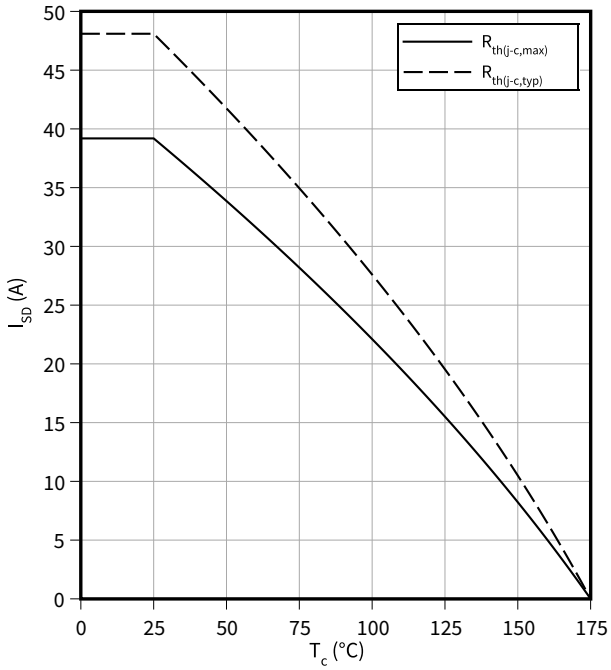
$I_D = f(T_c)$



Maximum source to drain current as a function of case temperature limited by bond wire

$I_{SD} = f(T_c)$

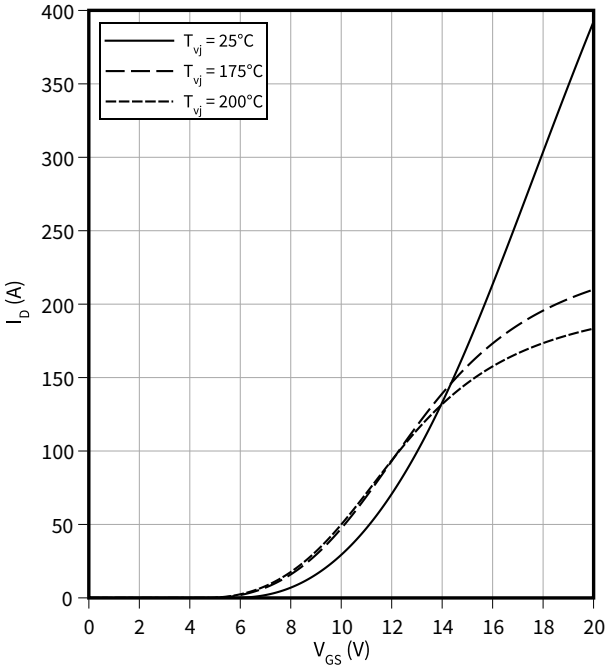
V_{GS} = 0 V



Typical transfer characteristic

$I_D = f(V_{GS})$

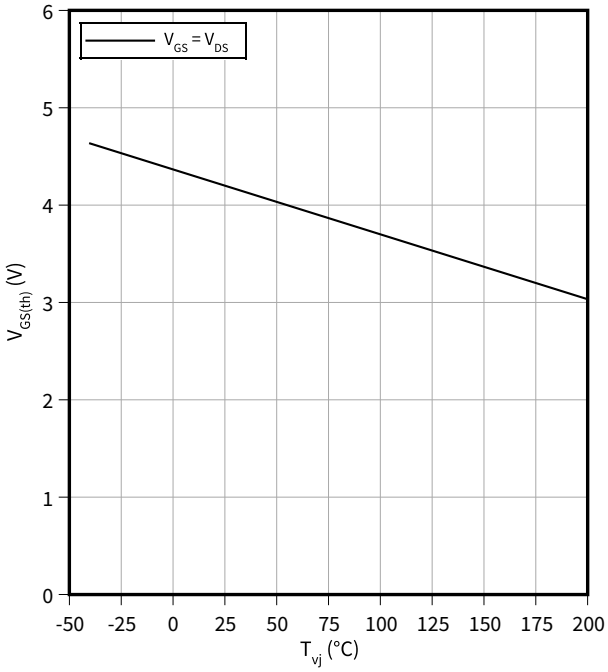
V_{DS} = 20 V, t_p = 20 µs



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

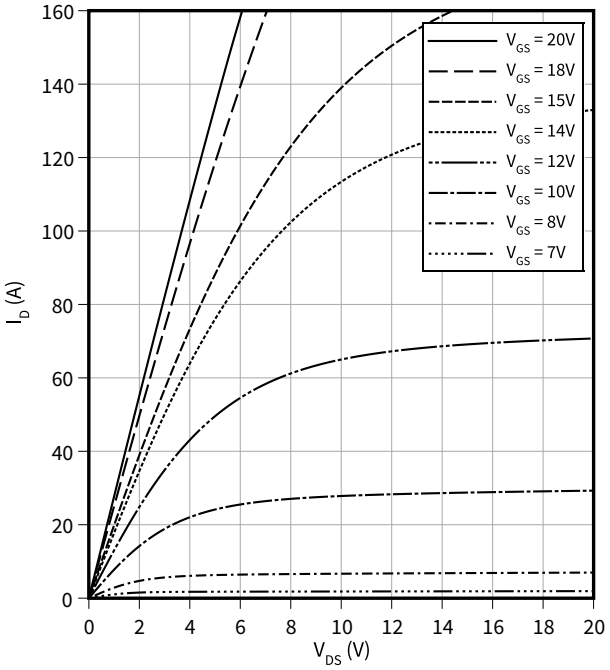
I_D = 5.5 mA



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

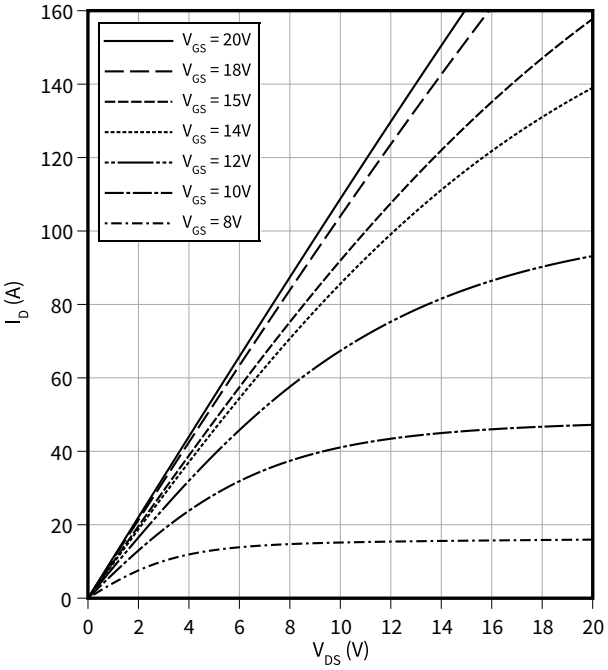
T_{vj} = 25 °C, t_p = 20 µs



Typical output characteristic, V_{GS} as a parameter

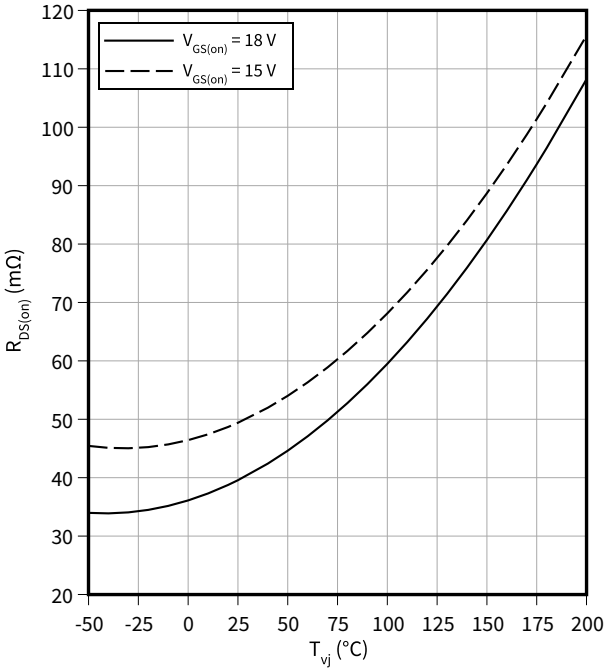
$I_D = f(V_{DS})$

T_{vj} = 175 °C, t_p = 20 µs



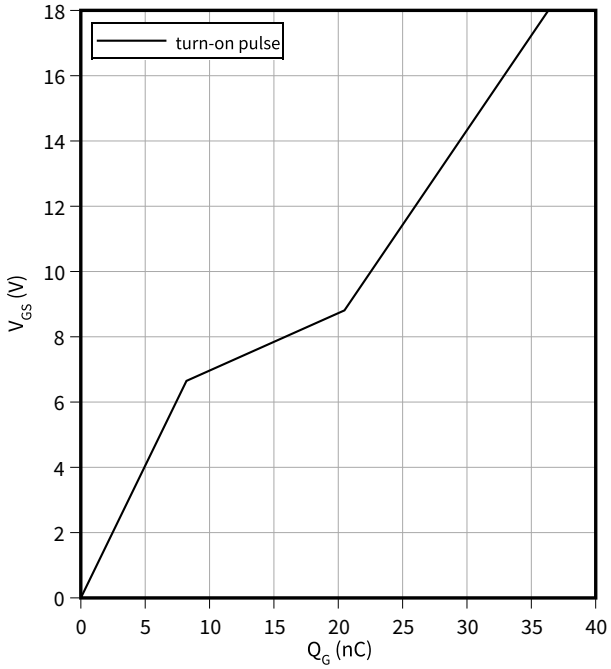
Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$
$I_D = 18$ A



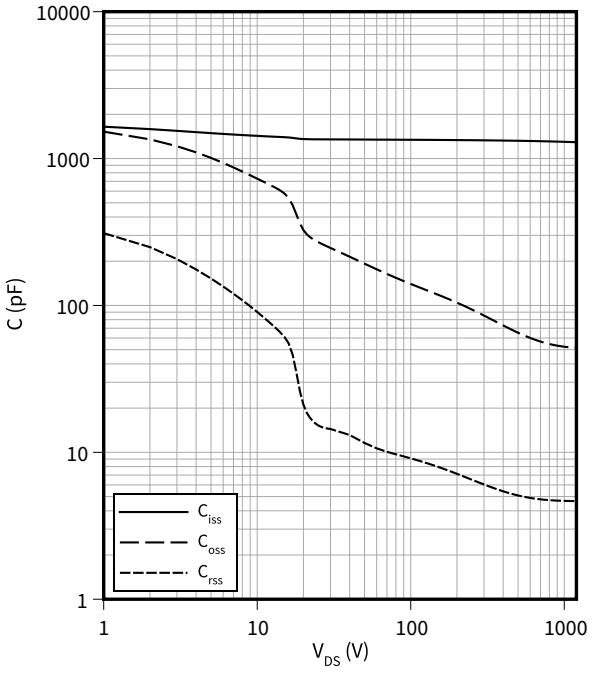
Typical gate charge

$V_{GS} = f(Q_G)$
$I_D = 18$ A, $V_{DS} = 800$ V



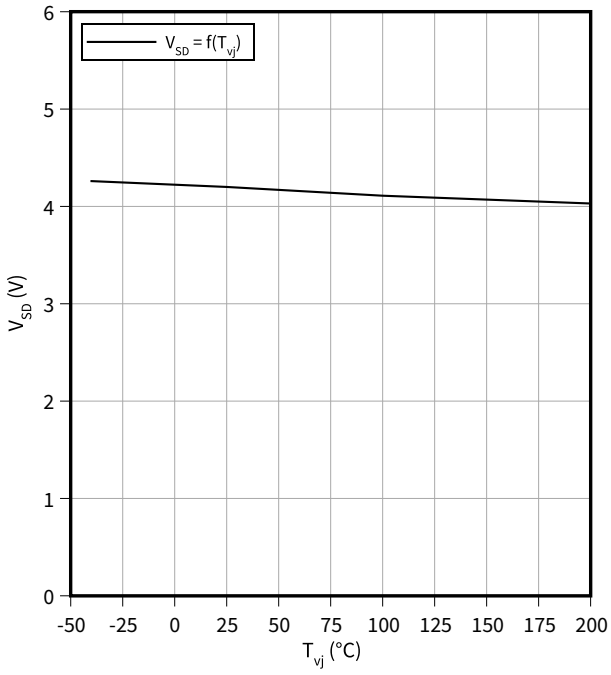
Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$
$f = 100$ kHz, $V_{GS} = 0$ V



Typical reverse drain voltage as a function of junction temperature

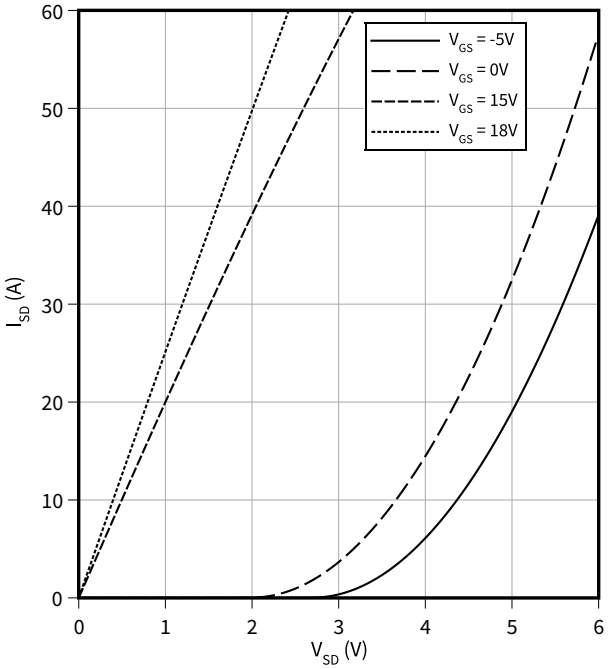
$V_{SD} = f(T_{vj})$
$I_{SD} = 18$ A, $V_{GS} = 0$ V



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

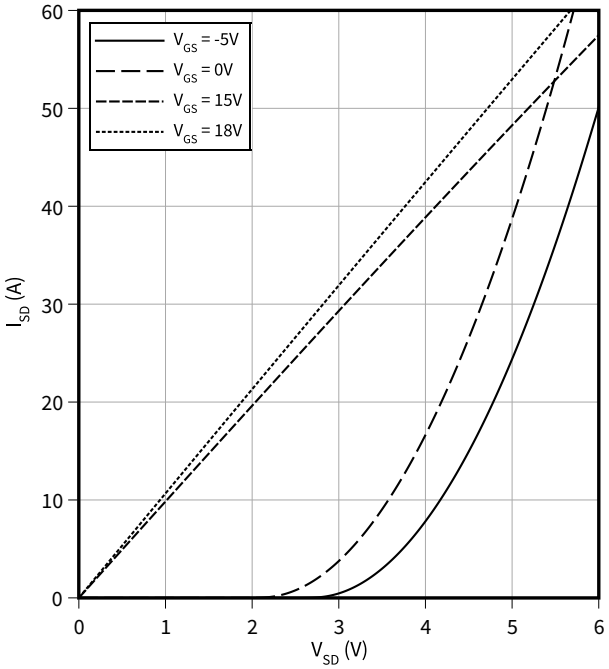
$T_{vj} = 25\ °C$, $t_p = 20\ µs$



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

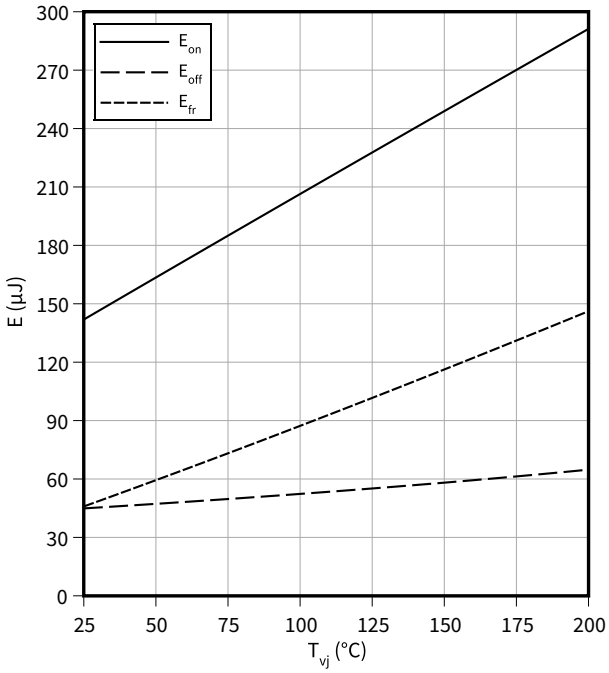
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\ V$

$E = f(T_{vj})$

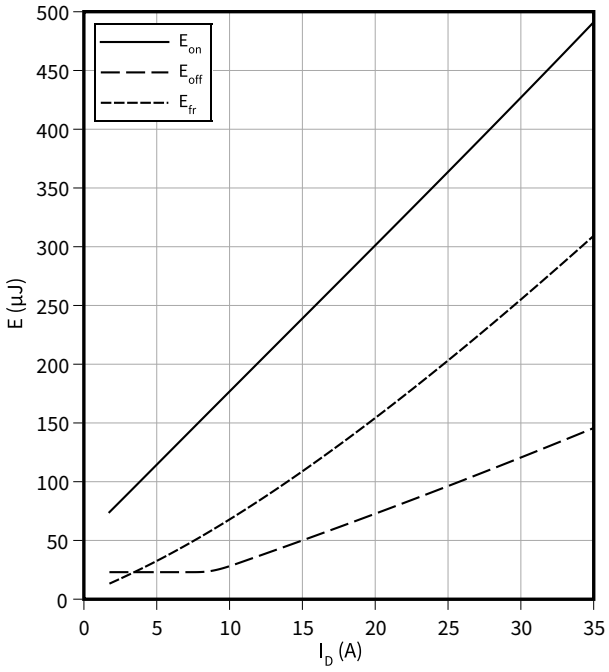
$V_{GS} = 0/18\ V$, $I_D = 18\ A$, $R_{G,ext} = 2.3\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\ V$

$E = f(I_D)$

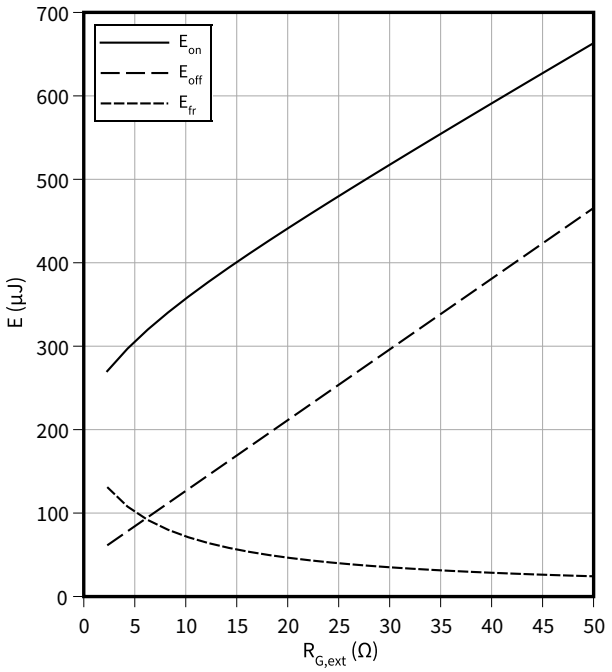
$V_{GS} = 0/18\ V$, $T_{vj} = 175\ °C$, $R_{G,ext} = 2.3\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

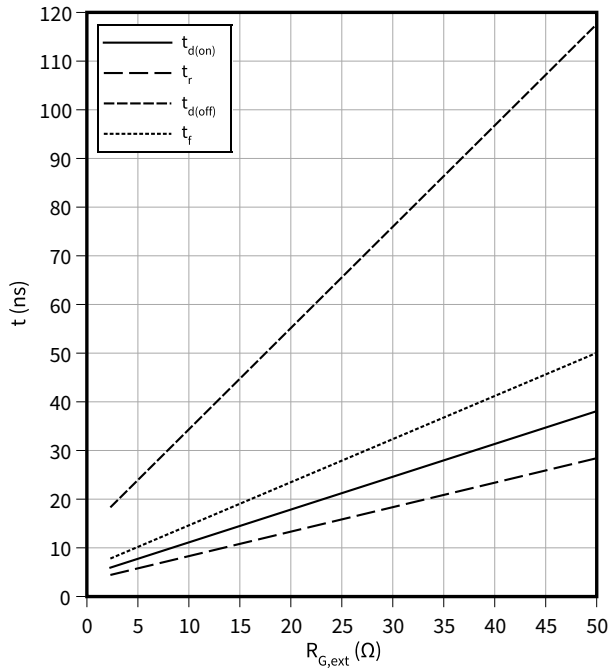
V_{GS} = 0/18 V, I_D = 18 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$t = f(R_{G,ext})$

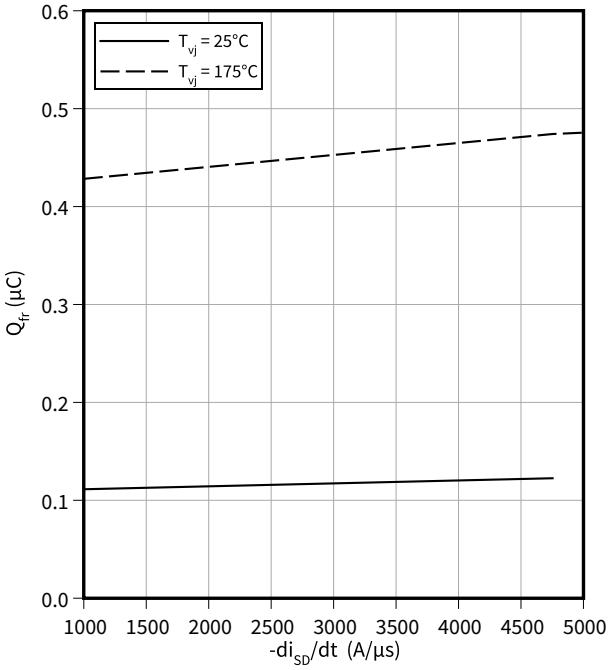
V_{GS} = 0/18 V, I_D = 18 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of revere drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$Q_{fr} = f(-di_{SD}/dt)$

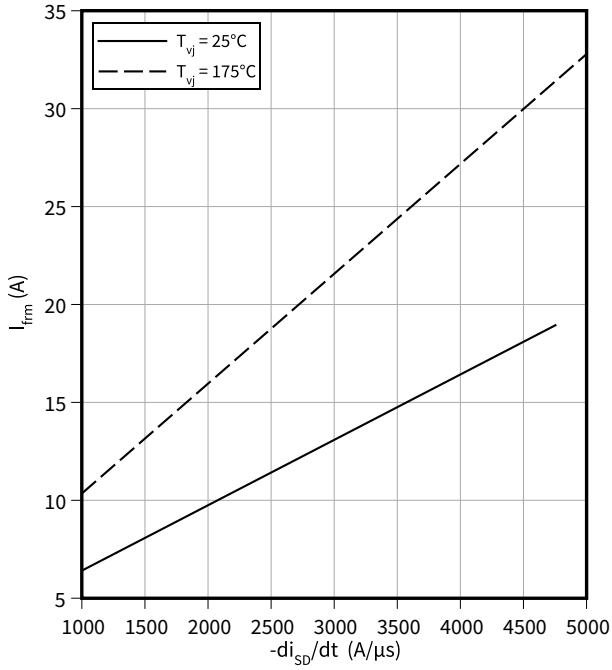
V_{GS} = 0/18 V, I_{SD} = 18 A, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$I_{frm} = f(-di_{SD}/dt)$

V_{GS} = 0/18 V, I_{SD} = 18 A, V_{DD} = 800 V

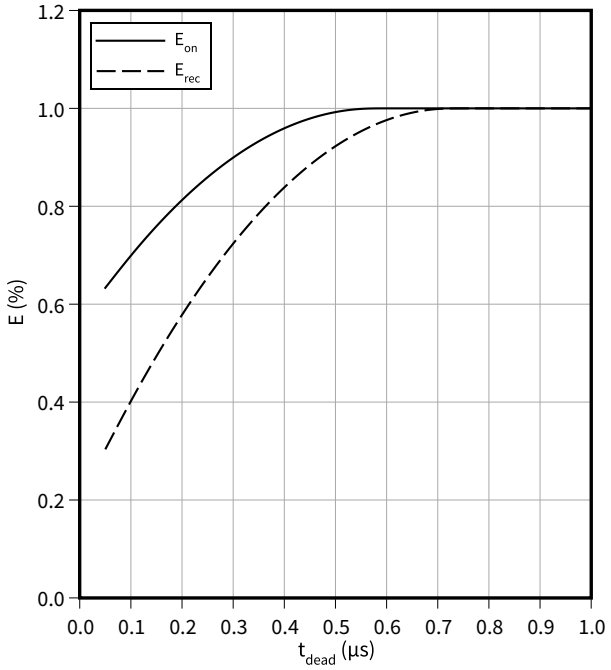


Typical switching energy as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(t_{dead})$

V_{GS} = 0/18 V, I_D = 18 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω

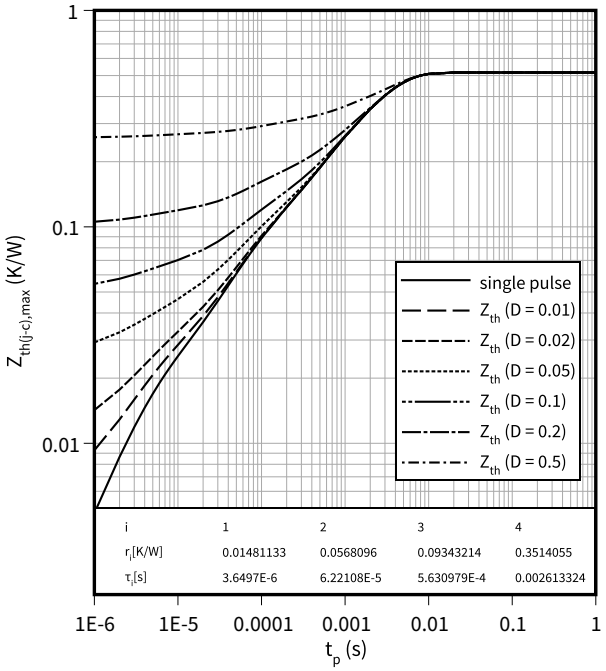
V_{DD} = 800 V



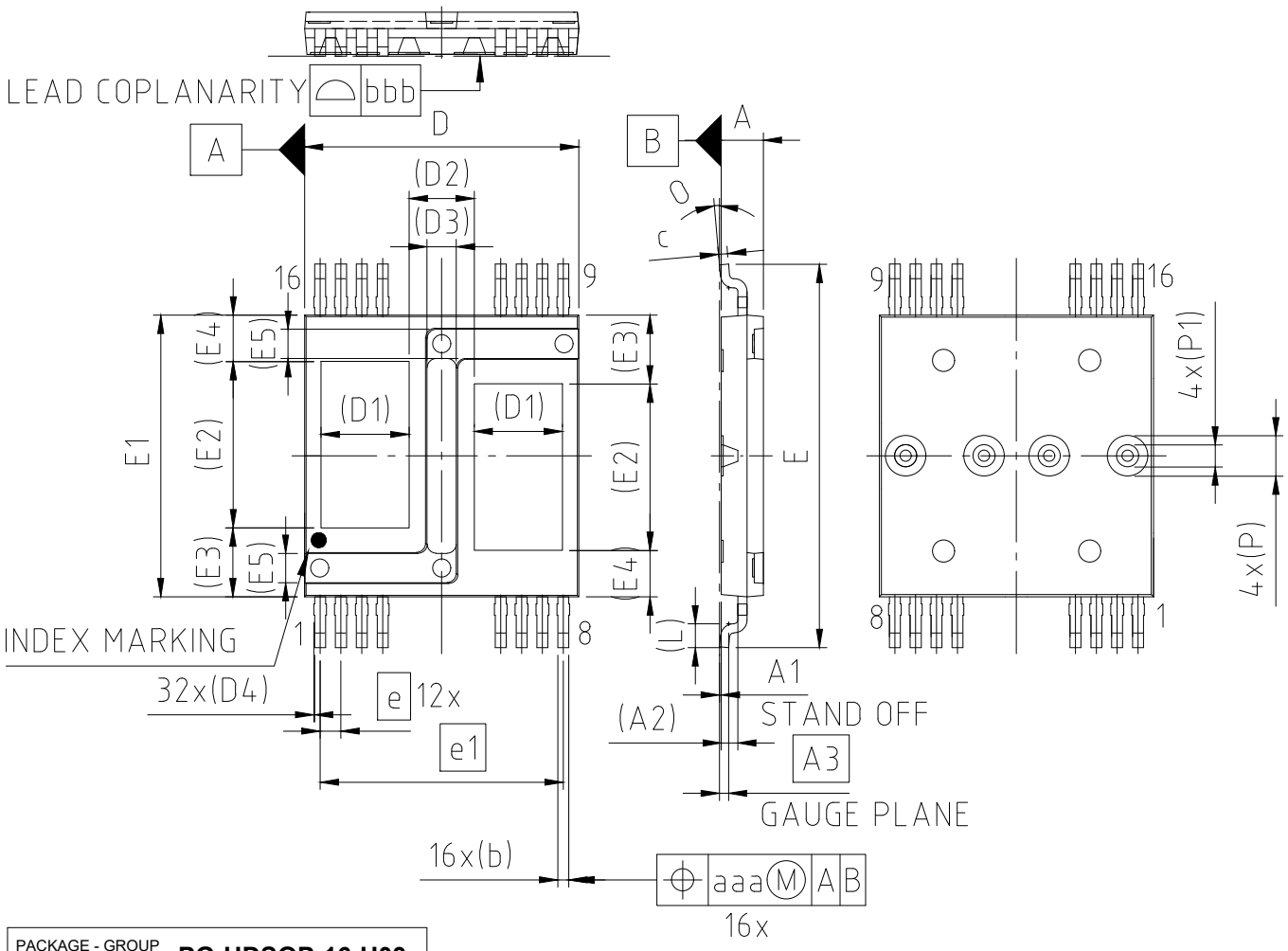
Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



5 Package outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U03	

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.90	
A3	0.50	
b	0.60	
c	0.46	0.58
D	14.90	15.10
D1	4.82	
D2	3.56	
D3	1.60	
D4	0.15	
E	20.81	21.11
E1	15.30	15.50
E2	9.10	
E3	3.76	
E4	2.54	
E5	1.60	

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
e	1.14	
e1	13.30	
L	1.30	
N	16	
O	0.00°	8°
P	2.20	
P1	1.20	
aaa	0.25	
bbb	0.10	

NOTES:
ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT
DIMENSIONS DO NOT INCLUDE MOLD FLASH,
PROTRUSION OR GATE BURRS

Figure 1

6 Testing conditions

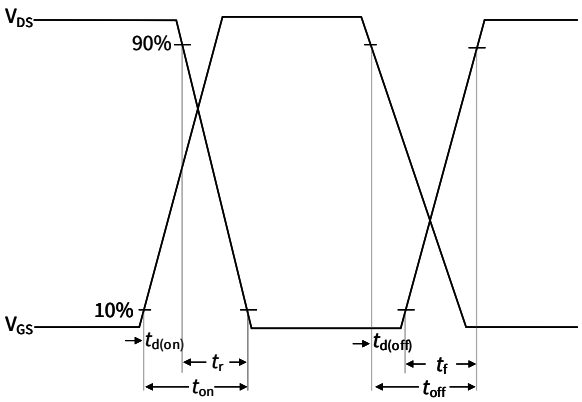


Figure A. **Definition of switching times**

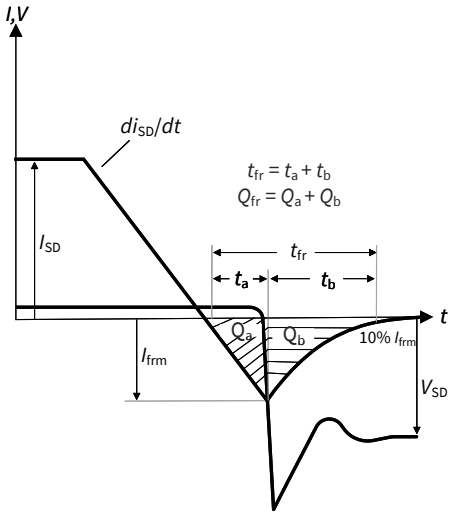


Figure B. **Definition of body diode switching characteristics**

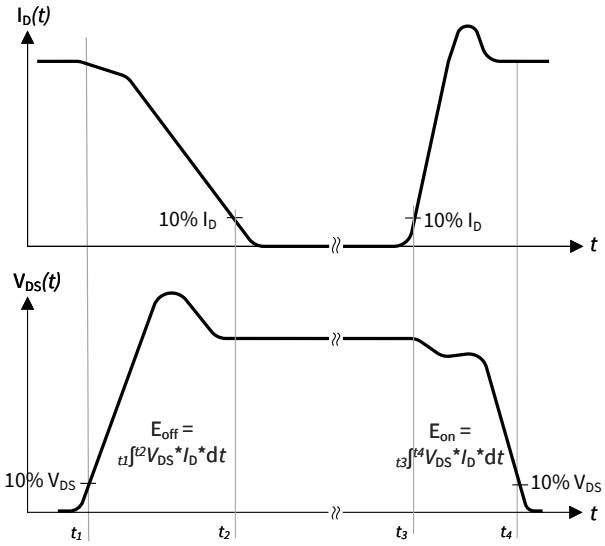


Figure C. **Definition of switching losses**

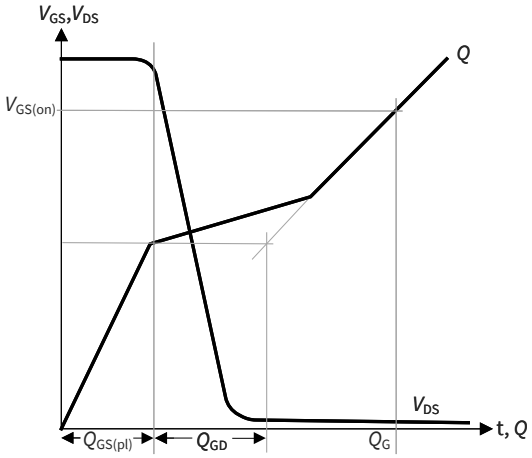


Figure D. **Definition of QGD**

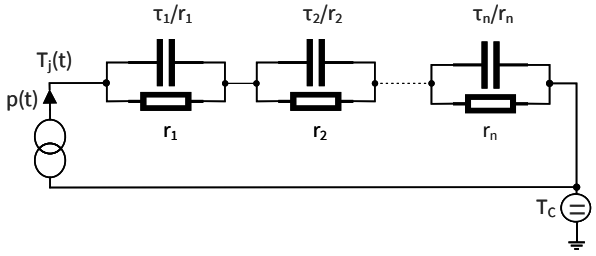


Figure E. **Thermal equivalent circuit**

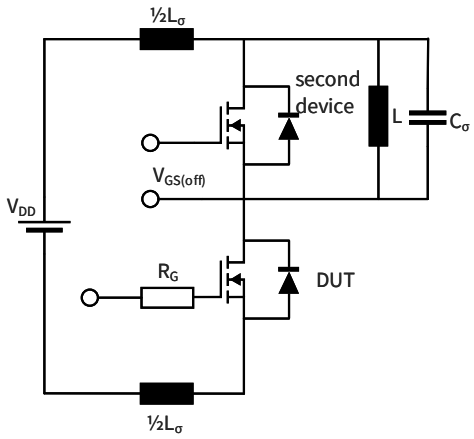


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2022-10-28	Target datasheet
0.20	2023-11-24	Preliminary datasheet
1.00	2025-02-13	Final datasheet
1.10	2026-10-05	Updated I_{DSS} max in Table 4 Editorial changes

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Edition 2026-10-05

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-ABF942-004

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