

SiC MOSFET

CoolSiC™ MOSFET 650 V G2

Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

Features

- Ultra-low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)} = 4.5 \text{ V}$
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance

Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

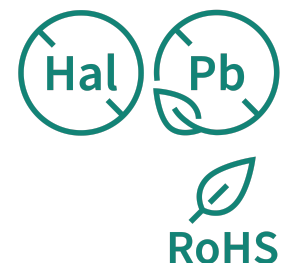
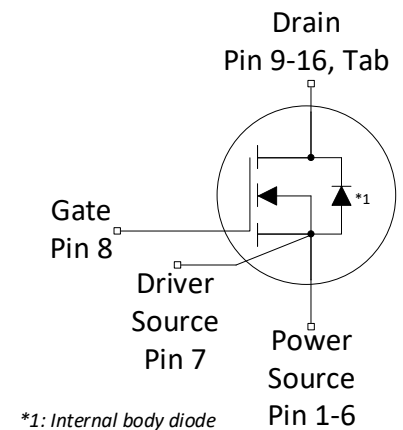
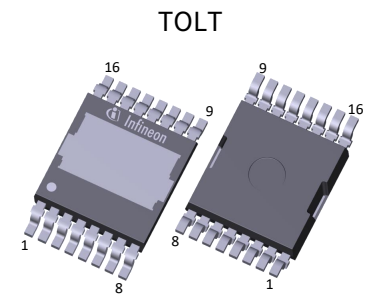
Product validation

Qualified according to relevant JEDEC tests.

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	650	V
$R_{DS(on),typ}$	60	mΩ
$R_{DS(on),max}$	73	mΩ
$Q_{G,typ}$	19	nC
$I_{D,pulse}$	96	A
$Q_{oss} @ 400 \text{ V}$	40	nC
$E_{oss} @ 400 \text{ V}$	5.5	μJ



Part number	Package	Marking	Related links
IMLT65R060M2H	PG-HDSOP-16	65R060M2	see Appendix A



Table of contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Operating range 5

Electrical characteristics 6

Electrical characteristics diagrams 8

Test circuits 13

Package outlines 14

Appendix A 17

Revision history 18

Trademarks 19

Disclaimer 19

1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous DC drain current ¹⁾	I_{DDC}	-	-	40	A	$T_c = 25^\circ\text{C}$
				28		$T_c = 100^\circ\text{C}$
Peak drain current ²⁾	I_{DM}	-	-	96	A	$T_c = 25^\circ\text{C}$, $V_{\text{GS}} = 18\text{ V}$
Avalanche energy, single pulse	E_{AS}	-	-	89	mJ	$I_D = 3.3\text{ A}$, $V_{\text{DD}} = 50\text{ V}$; see table 11
Avalanche energy, repetitive	E_{AR}			0.44		
Avalanche current, single pulse	I_{AS}	-	-	3.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	200	V/ns	$V_{\text{DS}} = 0 \dots 400\text{ V}$
Gate source voltage (static) ³⁾	V_{GS}	-7	-	23	V	-
Gate source voltage (transient)	V_{GS}	-10	-	25	V	$t_p \leq 500\text{ ns}$, duty cycle $\leq 1\%$
Power dissipation	P_{tot}	-	-	200	W	$T_c = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55		175	$^\circ\text{C}$	
Mounting torque	-	-		n.a.	Ncm	
Continuous reverse drain current ¹⁾	I_{SDC}	-	-	40	A	$V_{\text{GS}} = 18\text{ V}$, $T_c = 25^\circ\text{C}$
				28		$V_{\text{GS}} = 0\text{ V}$, $T_c = 25^\circ\text{C}$
Peak reverse drain current ²⁾	I_{SM}	-	-	96	A	$T_c = 25^\circ\text{C}$, $t_p \leq 250\text{ ns}$
				29		$T_c = 25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_c = 25^\circ\text{C}$, $t = 1\text{ min}$

¹⁾ Limited by $T_{j,\text{max}}$.

²⁾ Pulse width t_{pulse} limited by $T_{j,\text{max}}$.

³⁾ The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	0.75	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Operating range

Table 4 **Operating range**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$		0			

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DSS}	650	-	-	V	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 0.31\text{ mA}$
Gate threshold voltage ⁴⁾	$V_{\text{GS(th)}}$	3.5	4.5	5.6	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 3.1\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	1	75	μA	$V_{\text{DS}} = 650\text{ V}$, $V_{\text{GS}} = 0\text{ V}$, $T_j = 25^\circ\text{C}$
			3	-		$V_{\text{DS}} = 650\text{ V}$, $V_{\text{GS}} = 0\text{ V}$, $T_j = 175^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{\text{GS}} = 20\text{ V}$, $V_{\text{DS}} = 0\text{ V}$
Drain-source on-state resistance	$R_{\text{DS(on)}}$	-	78	-	m Ω	$V_{\text{GS}} = 15\text{ V}$, $I_{\text{D}} = 15.4\text{ A}$, $T_j = 25^\circ\text{C}$
			60	73		$V_{\text{GS}} = 18\text{ V}$, $I_{\text{D}} = 15.4\text{ A}$, $T_j = 25^\circ\text{C}$
			55	-		$V_{\text{GS}} = 20\text{ V}$, $I_{\text{D}} = 15.4\text{ A}$, $T_j = 25^\circ\text{C}$
			98	-		$V_{\text{GS}} = 18\text{ V}$, $I_{\text{D}} = 15.4\text{ A}$, $T_j = 175^\circ\text{C}$
Internal gate resistance	$R_{\text{G,int}}$	-	5.1	-	Ω	$f = 1\text{ MHz}$

4) Tested after 1 ms pulse at $V_{\text{GS}} = +20\text{ V}$. "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
 Stray inductances and coupling capacitances must be minimized.
 For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	669	-	pF	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 400\text{ V}$, $f = 250\text{ kHz}$
Reverse transfer capacitance	C_{rss}		4.5	-		
Output capacitance ⁵⁾	C_{oss}		56	73		
Output charge ⁵⁾	Q_{oss}	-	40	52	nC	calculation based on C_{oss}
Effective output capacitance, energy related ⁶⁾	$C_{\text{o(er)}}$	-	68	-	pF	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 0 \dots 400\text{ V}$
Effective output capacitance, time related ⁷⁾	$C_{\text{o(tr)}}$	-	101	-	pF	$I_{\text{D}} = \text{constant}$, $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 0 \dots 400\text{ V}$
Turn-on delay time	$t_{\text{d(on)}}$	-	6.3	-	ns	$V_{\text{DD}} = 400\text{ V}$, $V_{\text{GS}} = 0/18\text{ V}$, $I_{\text{D}} = 15.4\text{ A}$, $R_{\text{G,ext}} = 1.8\text{ }\Omega$; see table 10
Rise time	t_{r}		5.6			
Turn-off delay time	$t_{\text{d(off)}}$		13.7			
Fall time	t_{f}		4.8			

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
 Stray inductances and coupling capacitances must be minimized.
 For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Turn-ON switching losses ⁸⁾	E_{on}	-	26	-	μJ	$V_{DD} = 400\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 15.4\text{ A}$, $R_{G,ext} = 1.8\ \Omega$
Turn-OFF switching losses ⁸⁾	E_{off}		13			
Total switching losses ⁸⁾	E_{tot}		39			

⁵⁾ Maximum specification is defined by calculated six sigma upper confidence bound

⁶⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

⁷⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

⁸⁾ MOSFET used in half-bridge configuration without external diode.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	4.7	-	nC	$V_{DD} = 400\text{ V}$, $I_D = 15.4\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	Q_{GD}		3.6			
Total gate charge	Q_G		19			

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	4.3	-	V	$V_{GS} = 0\text{ V}$, $I_S = 15.4\text{ A}$, $T_j = 25^\circ\text{C}$
MOSFET forward recovery time	t_{fr}	-	10.2	-	ns	$V_{DD} = 400\text{ V}$, $I_S = 15.4\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9
			5.1			$V_{DD} = 400\text{ V}$, $I_S = 15.4\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9
MOSFET forward recovery charge ⁹⁾	Q_{fr}	-	42	-	nC	$V_{DD} = 400\text{ V}$, $I_S = 15.4\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9
			50			$V_{DD} = 400\text{ V}$, $I_S = 15.4\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9
MOSFET peak forward recovery current	I_{frm}	-	8.2	-	A	$V_{DD} = 400\text{ V}$, $I_S = 15.4\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9
			19.7			$V_{DD} = 400\text{ V}$, $I_S = 15.4\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9

⁹⁾ Q_{fr} includes Q_{oss} .

5 Electrical characteristics diagrams

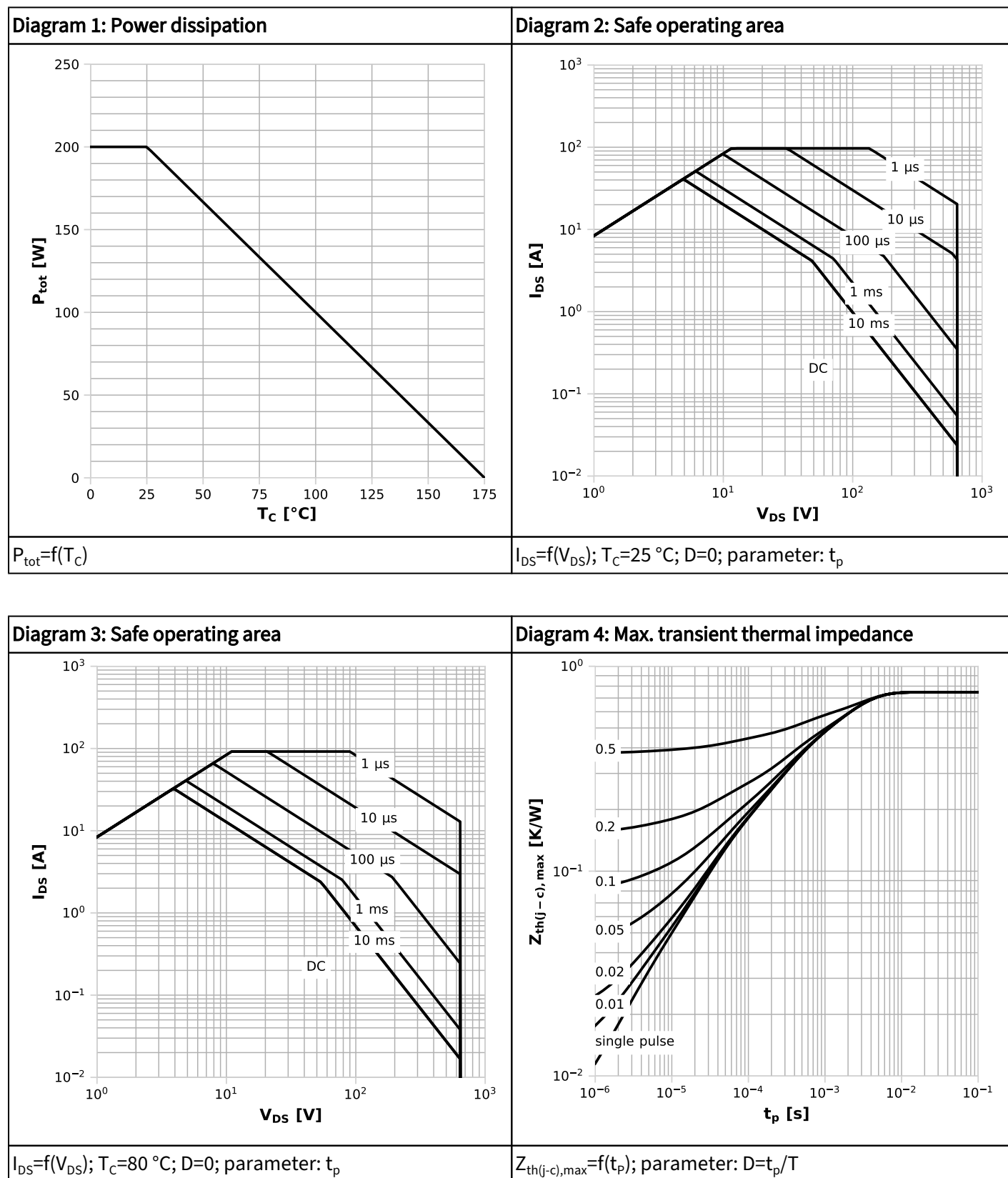
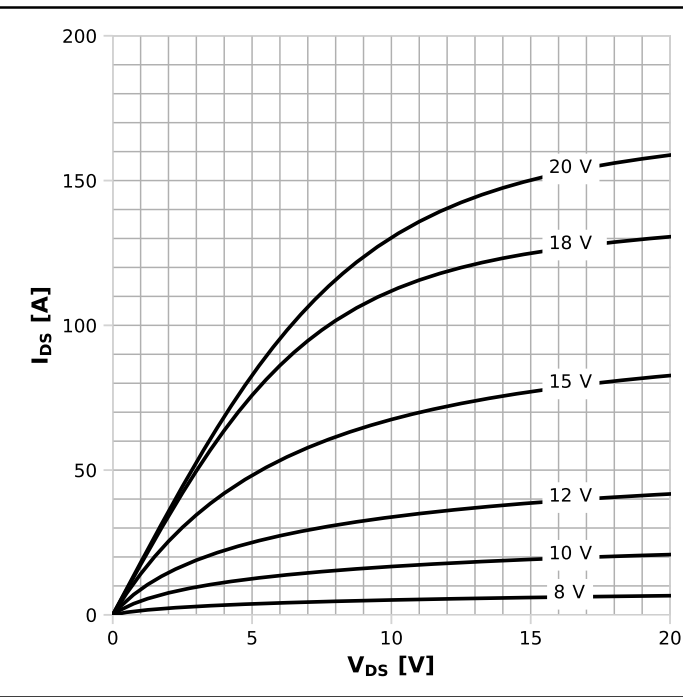
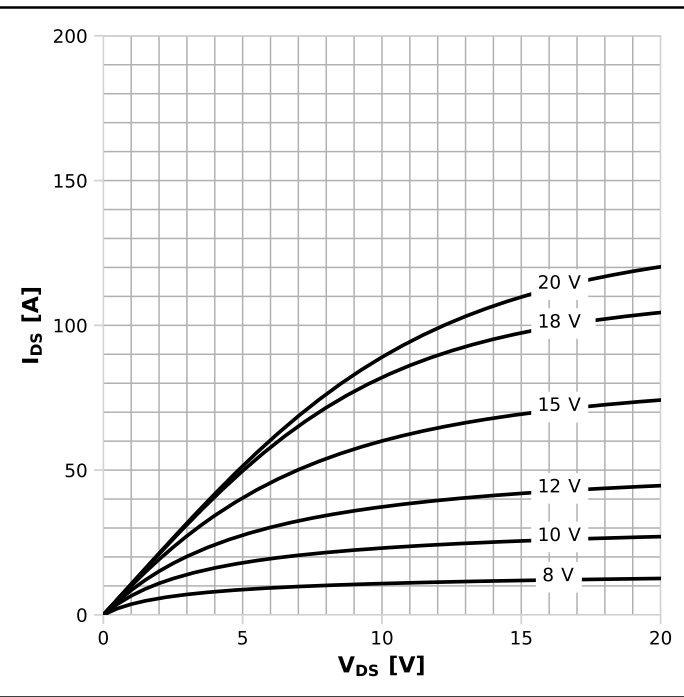


Diagram 5: Typ. output characteristics



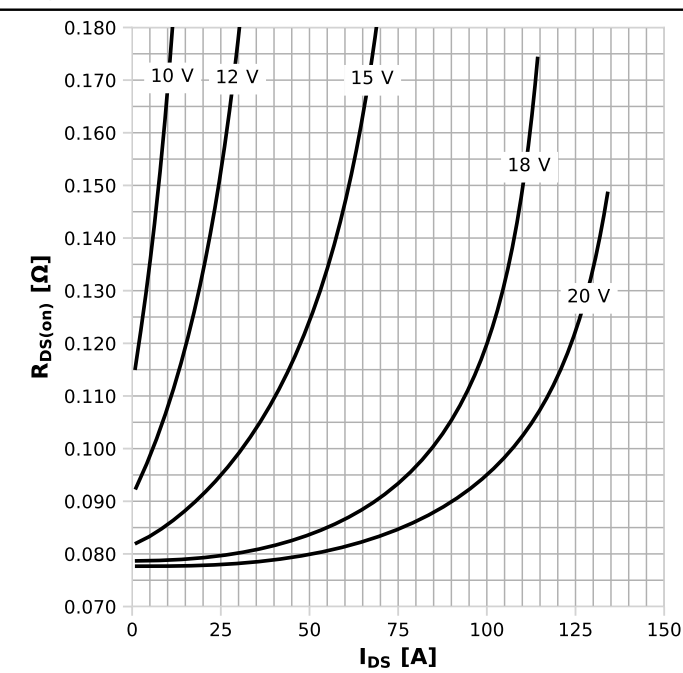
$I_{DS}=f(V_{DS})$; $T_j=25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



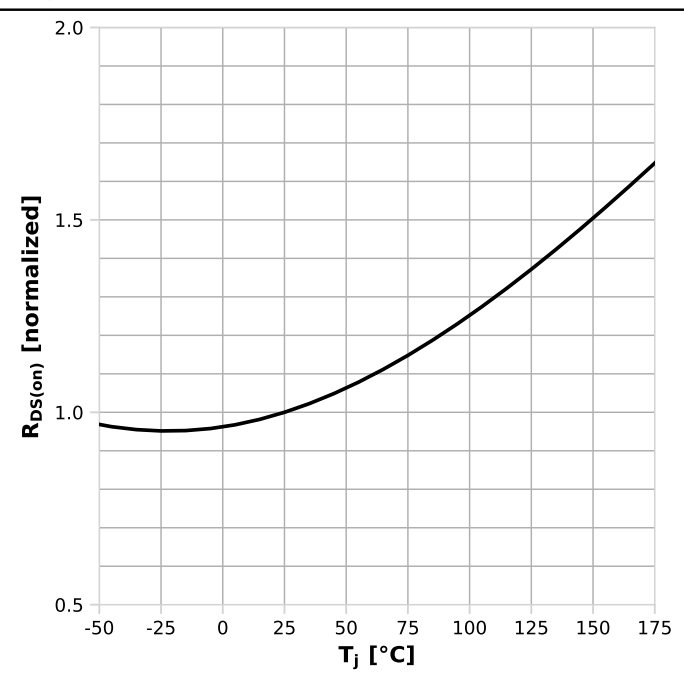
$I_{DS}=f(V_{DS})$; $T_j=175\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



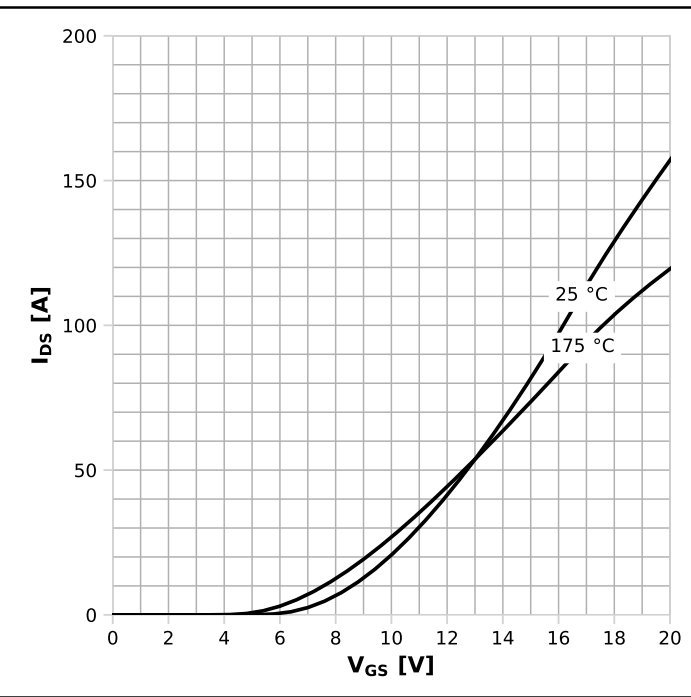
$R_{DS(on)}=f(I_{DS})$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



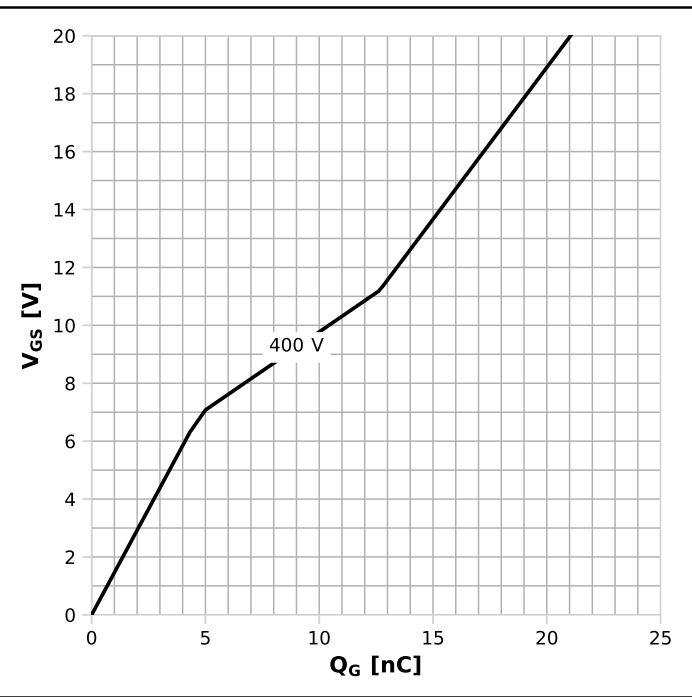
$R_{DS(on)}=f(T_j)$; $I_D=15.4\text{ A}$; $V_{GS}=18\text{ V}$

Diagram 9: Typ. transfer characteristics



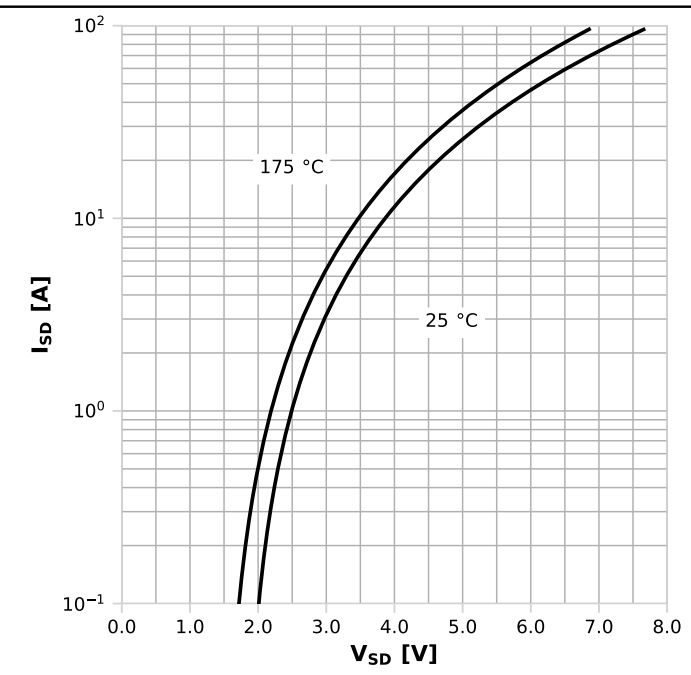
$I_{DS}=f(V_{GS})$; $V_{DS}=20$ V; parameter: T_j

Diagram 10: Typ. gate charge



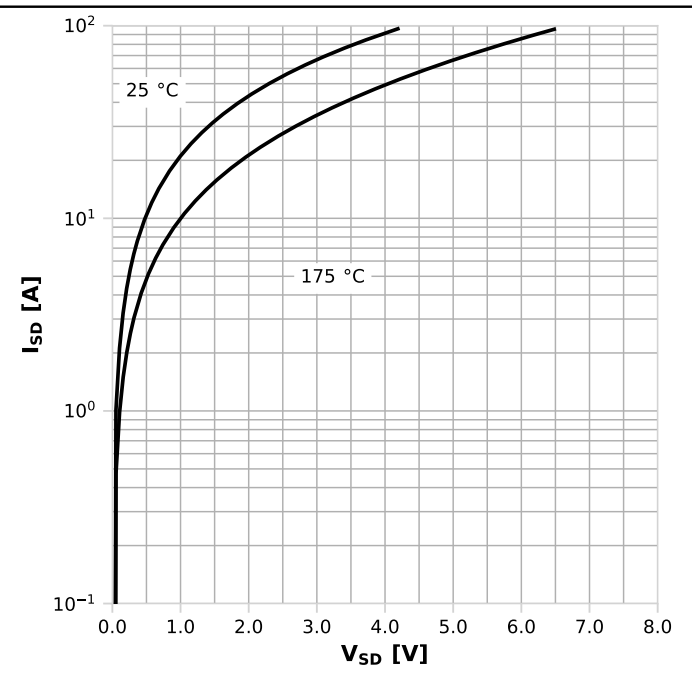
$V_{GS}=f(Q_G)$; $I_D=15.4$ A pulsed; parameter: V_{DD}

Diagram 11: Typ. reverse drain current characteristics



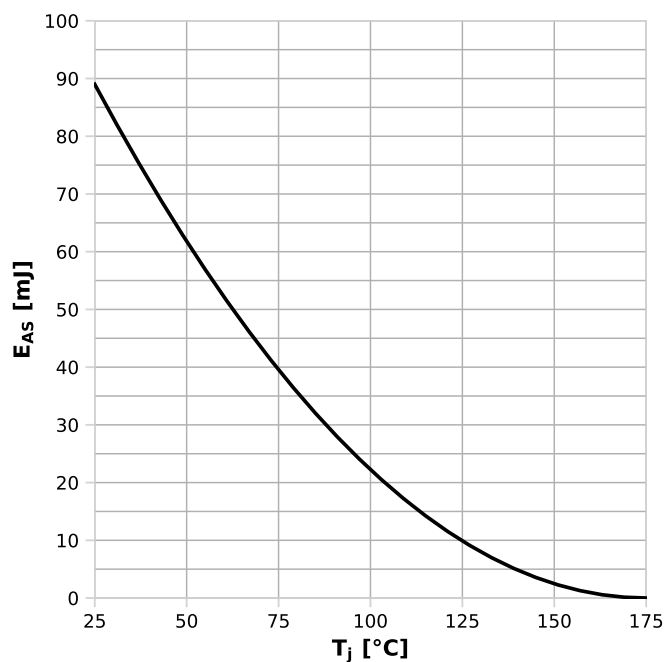
$I_{SD}=f(V_{SD})$; $V_{GS}=0$ V; parameter: T_j

Diagram 12: Typ. reverse drain current characteristics



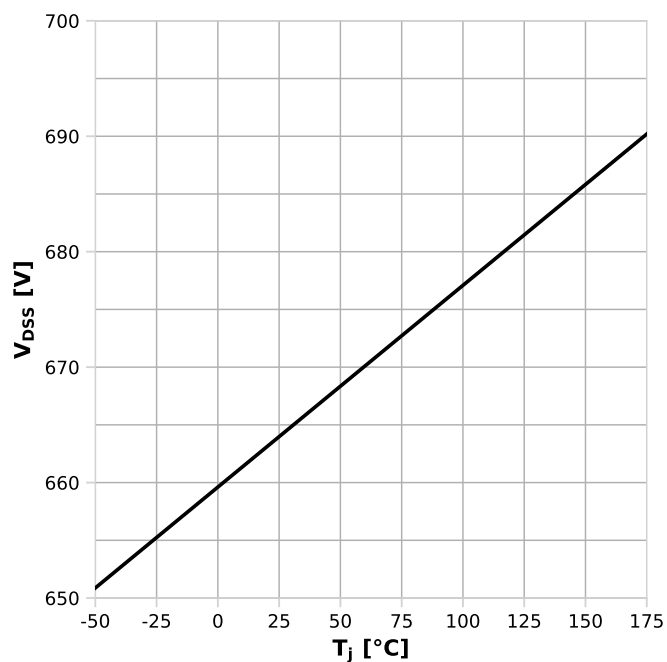
$I_{SD}=f(V_{SD})$; $V_{GS}=18$ V; parameter: T_j

Diagram 13: Avalanche energy



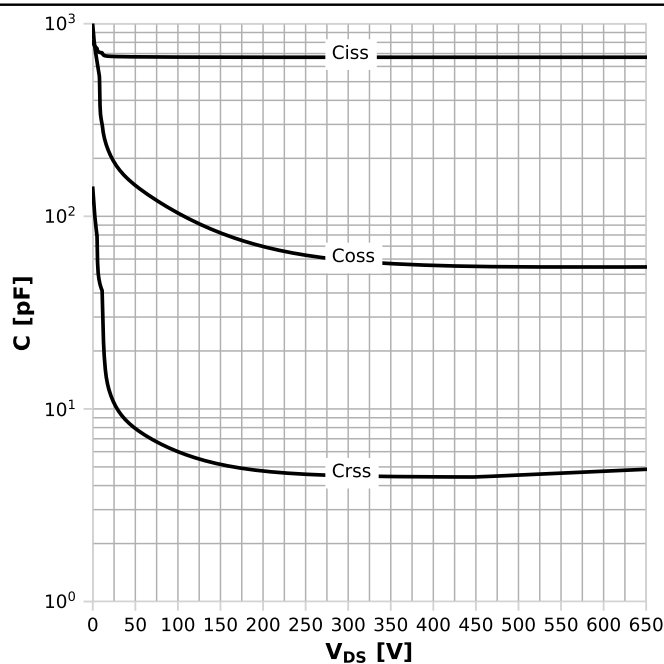
$E_{AS}=f(T_J); I_D=3.3\text{ A}; V_{DD}=50\text{ V}$

Diagram 14: Drain-source breakdown voltage



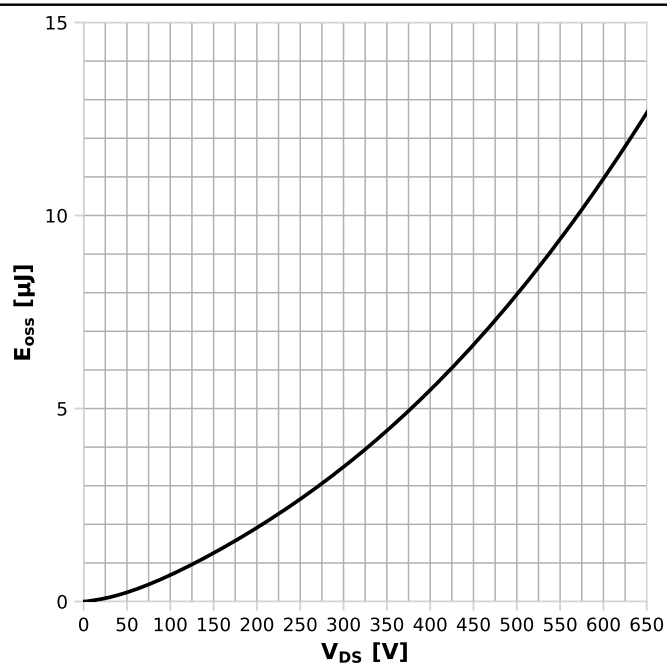
$V_{DSS}=f(T_J); I_D=0.31\text{ mA}$

Diagram 15: Typ. capacitances



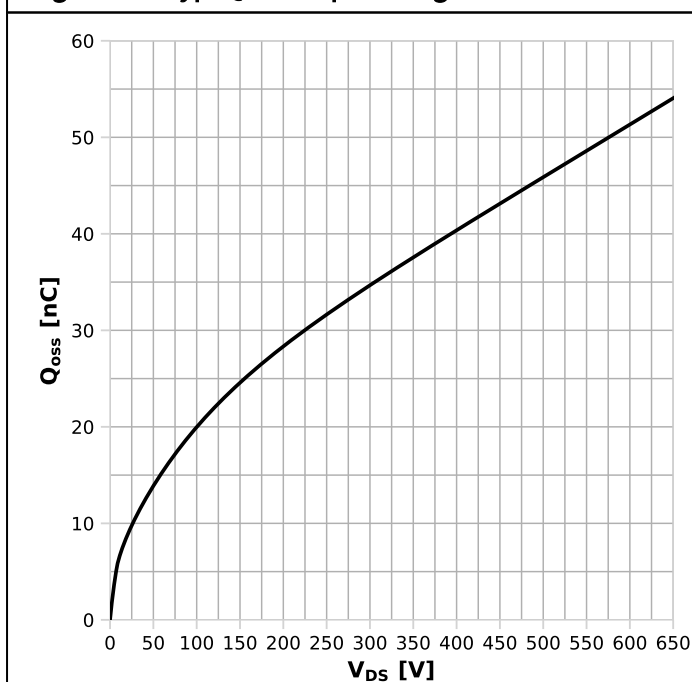
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 16: Typ. Coss stored energy



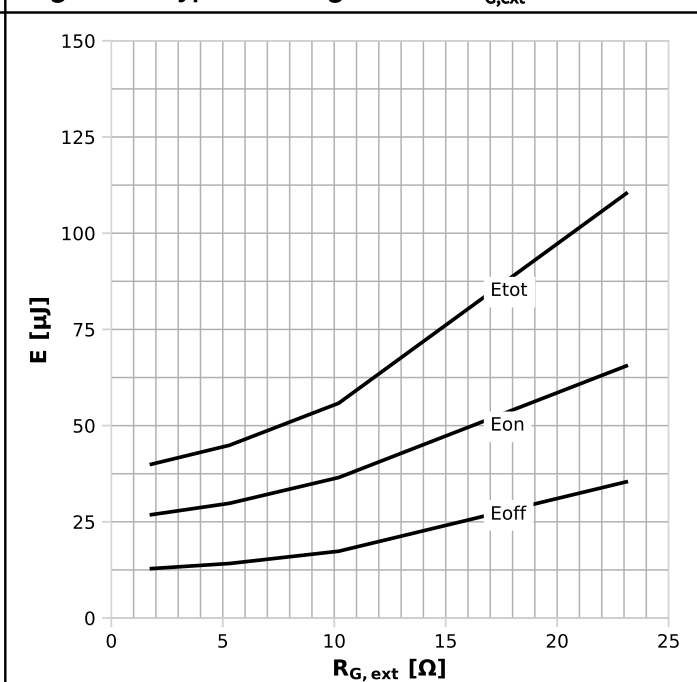
$E_{OSS}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



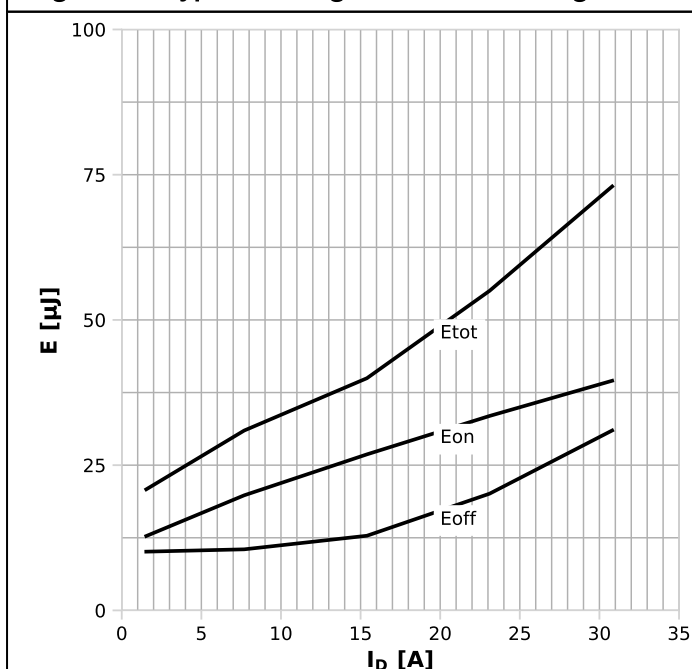
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. Switching Losses vs $R_{G,ext}$



$E=f(R_{G,ext}); V_{DD}=400\text{ V}; V_{GS}=0-18\text{ V}; I_D=15.4\text{ A}$

Diagram 19: Typ. Switching Losses vs switching current



$E=f(I_D); V_{DD}=400\text{ V}; V_{GS}=0-18\text{ V}; R_{G,ext}=1.8\text{ Ω}$

6 Test circuits

Table 9 Body diode characteristics

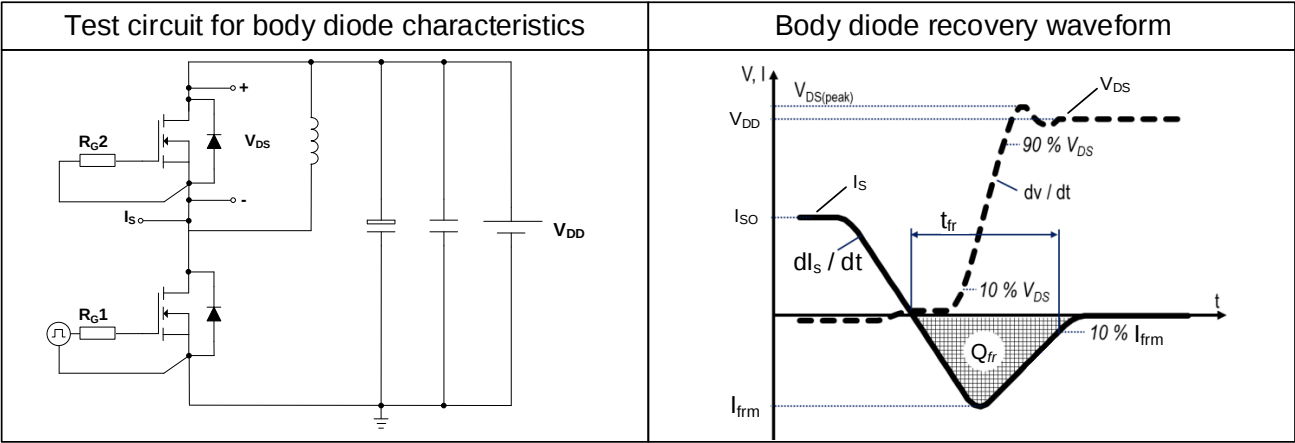


Table 10 Switching times

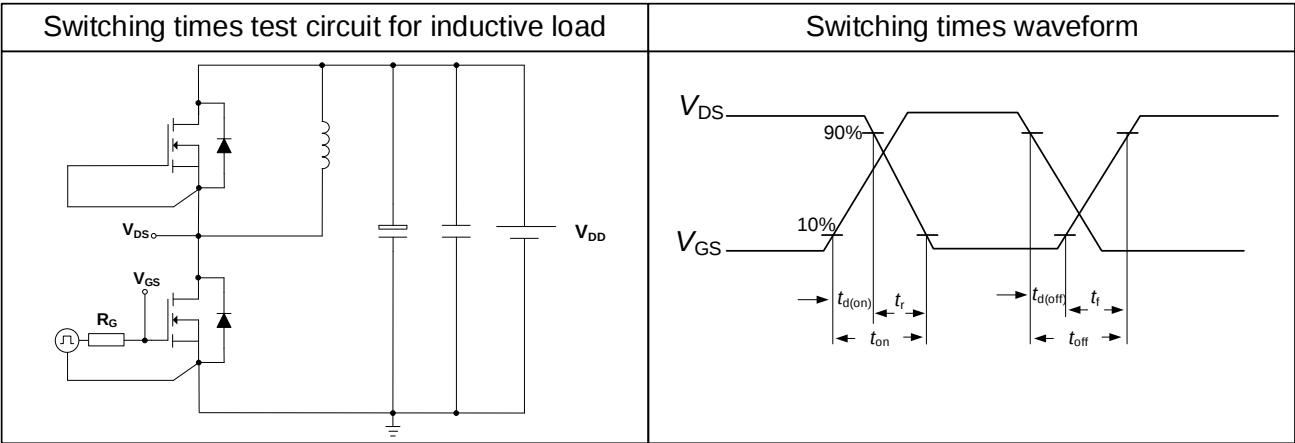
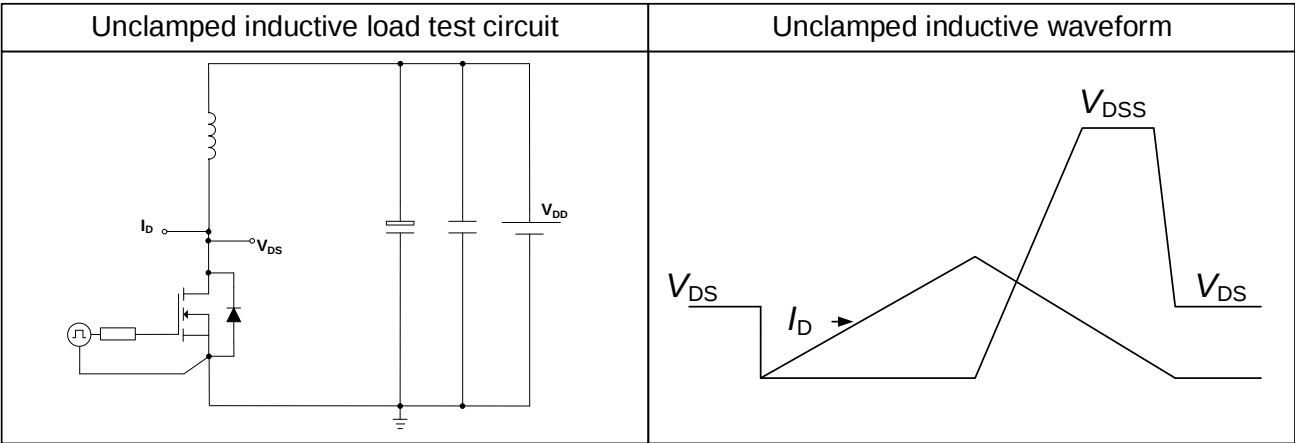


Table 11 Unclamped inductive load



7 Package outlines

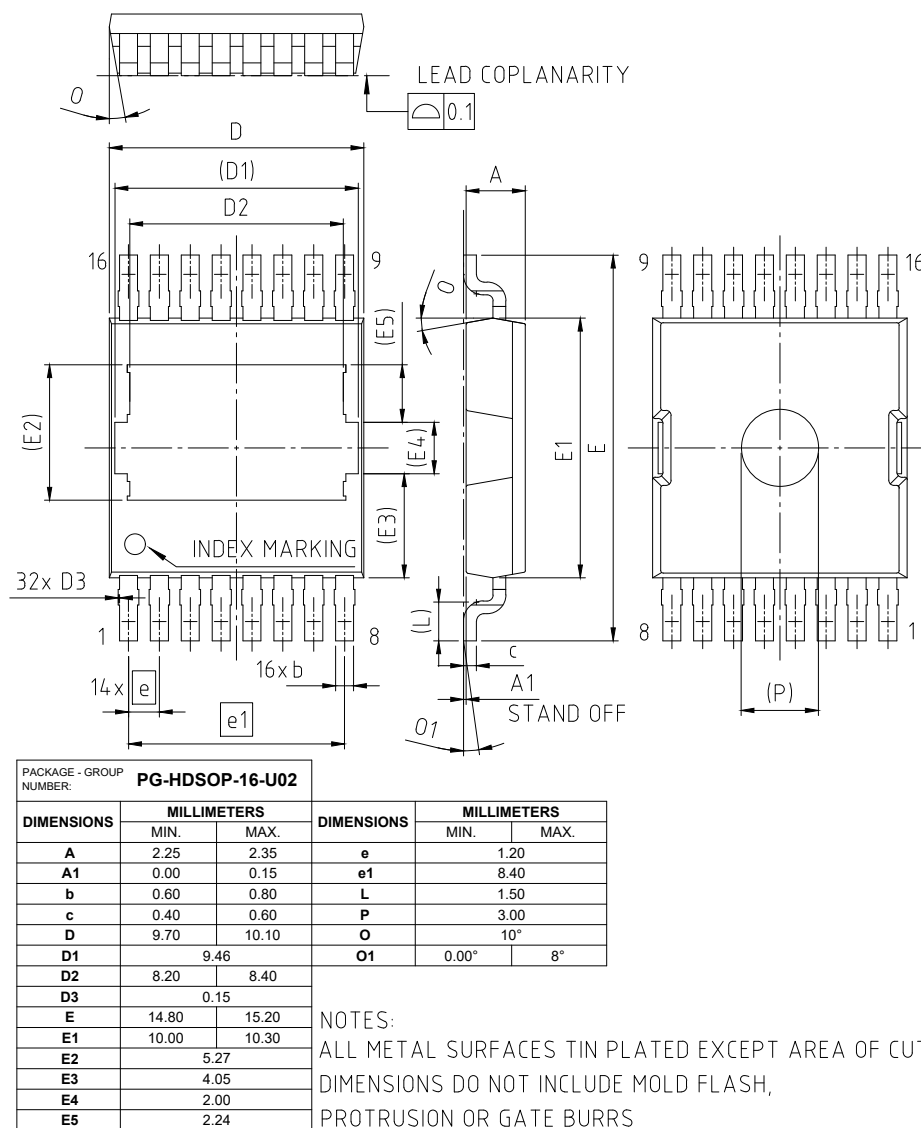


Figure 1 Outline PG-HDSOP-16, dimensions in mm

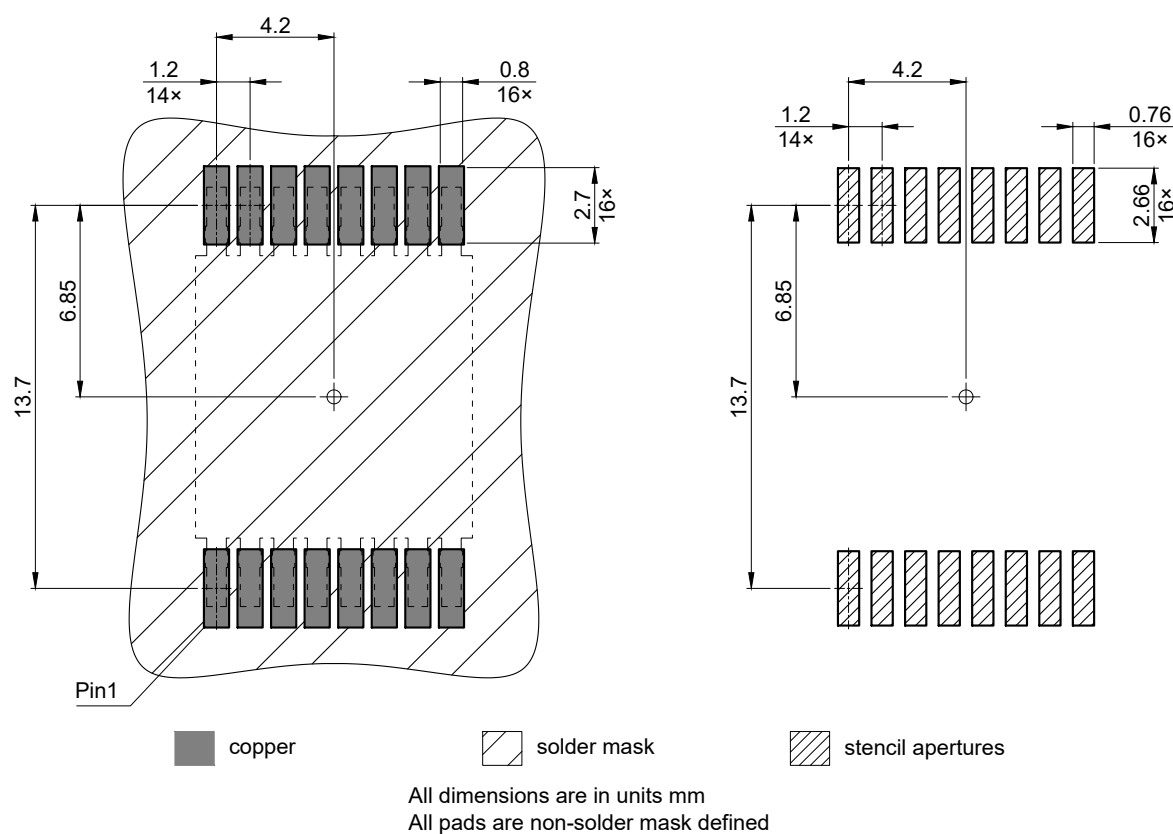
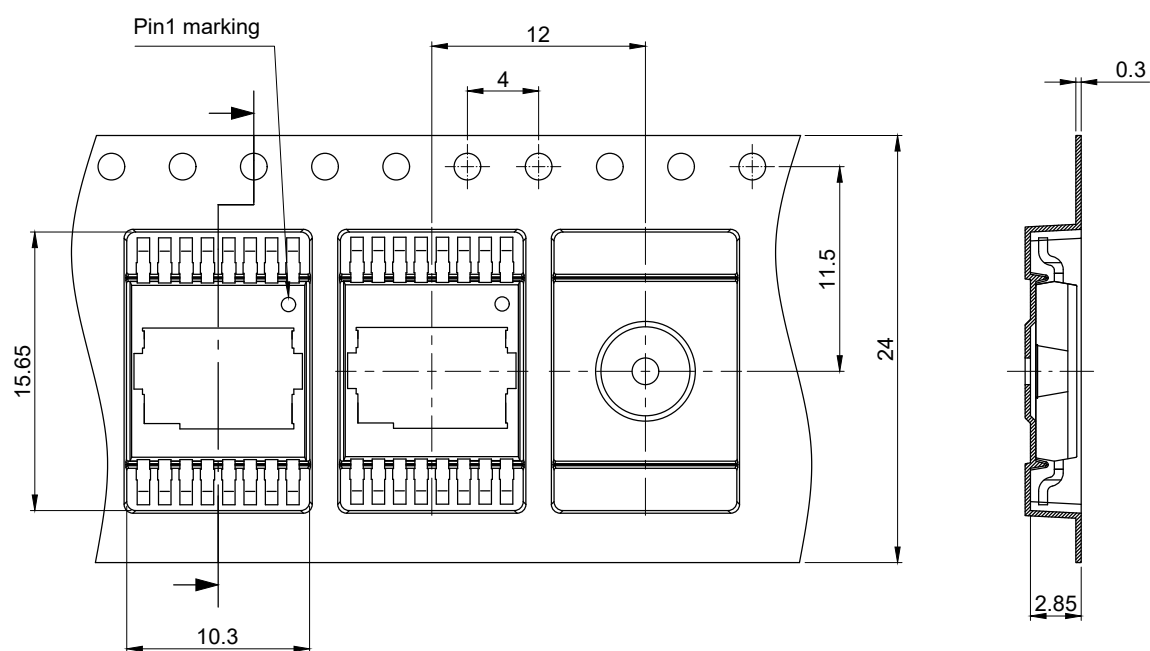


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm

8 Appendix A

Table 12 **Related links**

- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Application Note](#)
- [IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Simulation Model](#)
- [IFX Design tools](#)

Revision history

IMLT65R060M2H

Revision 2026-02-24, Rev. 2.3

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2024-05-03	Release of final
2.1	2024-11-20	update of reverse diode characteristics
2.2	2025-03-17	Revision of reverse diode characteristics
2.3	2026-02-24	Update of capacitances (Coss, Crss) related parameters

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Published by Infineon Technologies AG, Am Campeon 1-15, 85579 Neubiberg, Germany
Copyright (c) 2026 Infineon Technologies AG and its affiliates. All Rights Reserved.

Important notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features: Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:

The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit <https://www.infineon.com>.