

SiC MOSFET

CoolSiC™ MOSFET 750 V G2

Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 750 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class $R_{DS(on)} \times Q_{fr}$
- Excellent $R_{DS(on)} \times Q_{oss}$ and $R_{DS(on)} \times Q_G$
- Unique combination of low C_{rSS}/C_{iSS} and high $V_{GS(th)}$
- Infineon proprietary die attach technology
- Cutting edge TSC package with material group I
- Driver source pin available

Benefits

- Enhanced robustness and reliability for bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Best-in-class thermal dissipation
- Reduced switching losses through improved gate control

Potential applications

- Solid state relays and circuit breakers
- EV charging infrastructure
- Solar PV inverters and UPS
- Energy storage and battery formation
- Telecom and Server SMPS

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction. When paralleling MOSFETs the placement of the gate resistor is generally recommended to be in series to the Driver Source instead of the Gate.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	11.0	mΩ
$R_{DS(on),max}$	13.8	mΩ
$Q_{G,typ}$	106	nC
$I_{D,pulse}$	532	A
$Q_{oss,typ}$ @ 500 V	226	nC
$E_{oss,typ}$ @ 500 V	39	μJ

Part number	Package	Marking	Related links
IMDQ75R011M2H	PG-HDSOP-22	75R011M2	see Appendix A

Q-DPAK

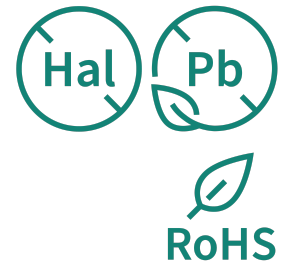
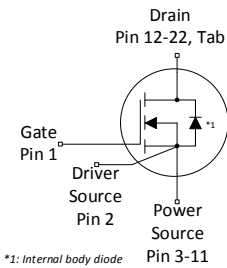
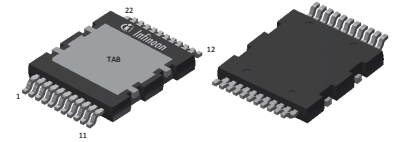


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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

“Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DSS}	-	-	750	V	static, $T_j = -55^\circ\text{C}$ to 175°C
Continuous DC drain current ¹⁾	I_{DDC}	-	-	148	A	$T_c = 25^\circ\text{C}$
				105		$T_c = 100^\circ\text{C}$
Peak drain current ²⁾	I_{DM}	-	-	532	A	$T_c = 25^\circ\text{C}$, $V_{\text{GS}} = 18\text{ V}$
Avalanche energy, single pulse	E_{AS}	-	-	507	mJ	$I_{\text{D}} = 19.0\text{ A}$, $V_{\text{DD}} = 50\text{ V}$; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	2.62		
Avalanche current, single pulse	I_{AS}	-	-	19.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	200	V/ns	$V_{\text{DS}} = 0 \dots 500\text{ V}$
Gate source voltage (static) ³⁾	V_{GS}	-7	-	23	V	-
Gate source voltage (transient)	V_{GS}	-11	-	25	V	$t_p \leq 500\text{ ns}$, duty cycle $\leq 1\%$
Power dissipation	P_{tot}	-	-	555	W	$T_c = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		
Extended operating junction temperature ⁴⁾	T_j	-	-	200	°C	$\leq 100\text{ h}$ in the application lifetime
Mounting torque	-	-	-	n.a	Ncm	-
Continuous reverse drain current ¹⁾	I_{SDC}	-	-	148	A	$V_{\text{GS}} = 18\text{ V}$, $T_c = 25^\circ\text{C}$
				95		$V_{\text{GS}} = 0\text{ V}$, $T_c = 25^\circ\text{C}$
Peak reverse drain current ²⁾	I_{SM}	-	-	532	A	$T_c = 25^\circ\text{C}$, $t_p \leq 250\text{ ns}$
				152		$T_c = 25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_c = 25^\circ\text{C}$, $t = 1\text{ min}$

1) Limited by $T_{j,\text{max}}$.

2) Pulse width t_{pulse} limited by $T_{j,\text{max}}$.

3) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

4) Up to 7500 temperature cycles, where maximum delta T is limited to 100K.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	0.19	0.27	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-		

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage ⁵⁾	$V_{(BR)DSS}$	840	-	-	V	$V_{GS} = 0\text{ V}, I_D = 1.78\text{ mA}$
Gate threshold voltage ⁶⁾	$V_{GS(th)}$	3.5	4.5	5.6	V	$V_{DS} = V_{GS}, I_D = 17.8\text{ mA}, T_j = 25^\circ\text{C}$
		-	3.3	-		$V_{DS} = V_{GS}, I_D = 17.8\text{ mA}, T_j = 175^\circ\text{C}$
Zero gate voltage drain current	I_{DSS}	-	1	75	μA	$V_{DS} = 750\text{ V}, V_{GS} = 0\text{ V}, T_j = 25^\circ\text{C}$
			10	-		$V_{DS} = 750\text{ V}, V_{GS} = 0\text{ V}, T_j = 175^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS} = 23\text{ V}, V_{DS} = 0\text{ V}, T_j = 25^\circ\text{C}$
				-100		$V_{GS} = -7\text{ V}, V_{DS} = 0\text{ V}, T_j = 25^\circ\text{C}$
Forward transconductance	g_{fs}	-	48	-	S	$I_D = 80.9\text{ A}, V_{DS} = 20\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	14.0	-	m Ω	$V_{GS} = 15\text{ V}, I_D = 80.9\text{ A}, T_j = 25^\circ\text{C}$
			11.0	13.8		$V_{GS} = 18\text{ V}, I_D = 80.9\text{ A}, T_j = 25^\circ\text{C}$
			10.0	-		$V_{GS} = 20\text{ V}, I_D = 80.9\text{ A}, T_j = 25^\circ\text{C}$
Drain-source on-state resistance ⁷⁾	$R_{DS(on)}$	-	17.5	22.0	m Ω	$V_{GS} = 18\text{ V}, I_D = 80.9\text{ A}, T_j = 150^\circ\text{C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	20.0	-	m Ω	$V_{GS} = 18\text{ V}, I_D = 80.9\text{ A}, T_j = 175^\circ\text{C}$
Internal gate resistance	$R_{G,int}$	-	1.2	-	Ω	$f = 1\text{ MHz}$

⁵⁾ Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

⁶⁾ Tested after pre-conditioning pulse at $V_{GS} = +20\text{ V}$. "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

⁷⁾ Specified by design, not subject to production test.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3689	-	pF	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, f = 250\text{ kHz}$
Reverse transfer capacitance	C_{rss}		19	-		
Output capacitance ⁸⁾	C_{oss}		245	318		
Output charge ⁸⁾	Q_{oss}	-	226	294	nC	calculation based on C_{oss}
Effective output capacitance, energy related ⁹⁾	$C_{o(er)}$	-	312	-	pF	$V_{GS} = 0\text{ V}, V_{DS} = 0 \dots 500\text{ V}$
Effective output capacitance, time related ¹⁰⁾	$C_{o(tr)}$	-	452	-	pF	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0 \dots 500\text{ V}$

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD} = 500\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_D = 80.9\text{ A}$, $R_{G,ext} = 1.8\ \Omega$, $L_{stray} = 15\text{ nH}$; see table 10
Rise time	t_r	-	14	-	ns	
Turn-off delay time	$t_{d(off)}$	-	31	-	ns	
Fall time	t_f	-	8	-	ns	
Turn-ON switching losses ¹¹⁾	E_{on}	-	133	-	μJ	
Turn-OFF switching losses ¹¹⁾	E_{off}	-	149	-	μJ	
Total switching losses ¹¹⁾	E_{tot}	-	282	-	μJ	

8) Maximum specification is defined by calculated six sigma upper confidence bound.

9) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500 V.

10) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500 V.

11) MOSFET used in half-bridge configuration without external diode. Parameter verified by characterization according to IEC 60747-8.

Table 7 Gate charge characteristics

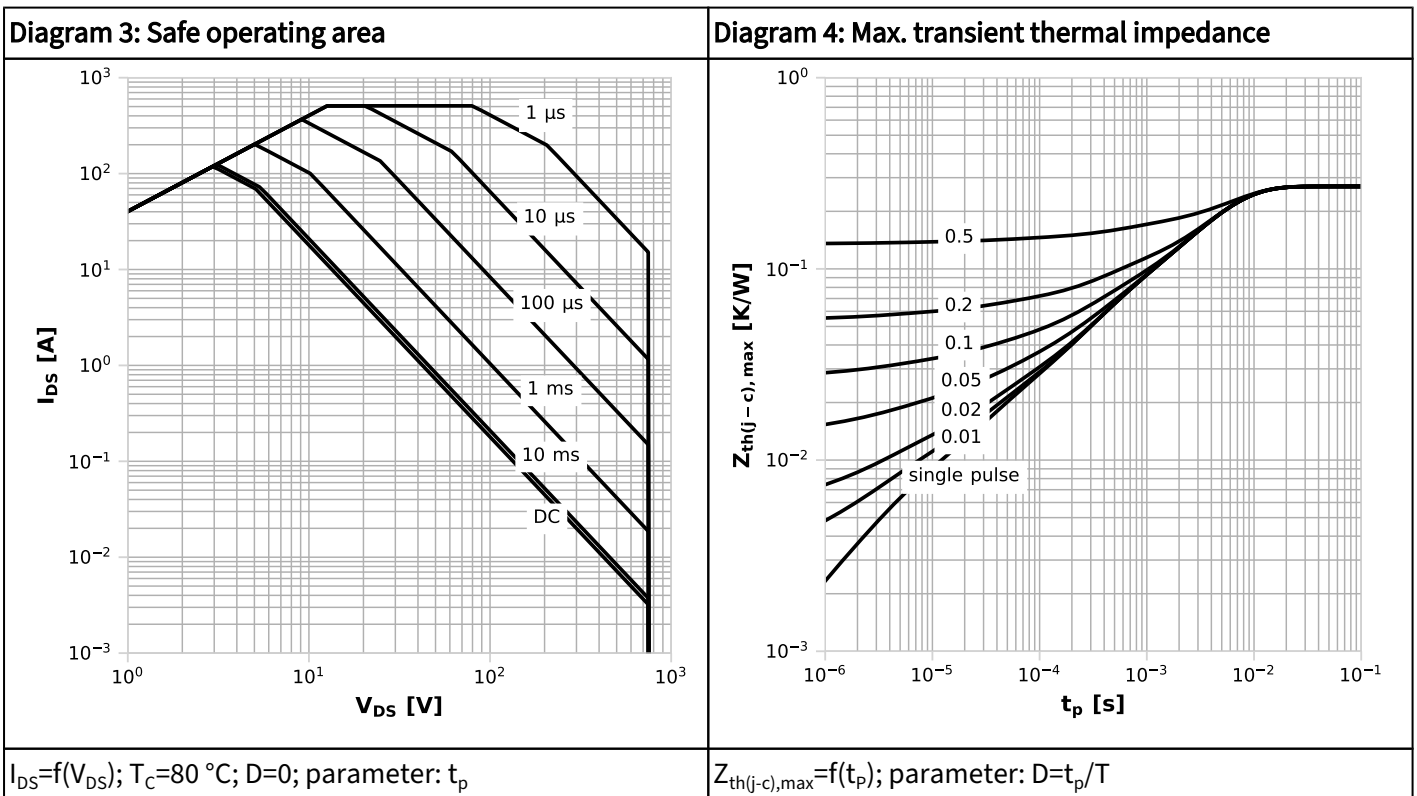
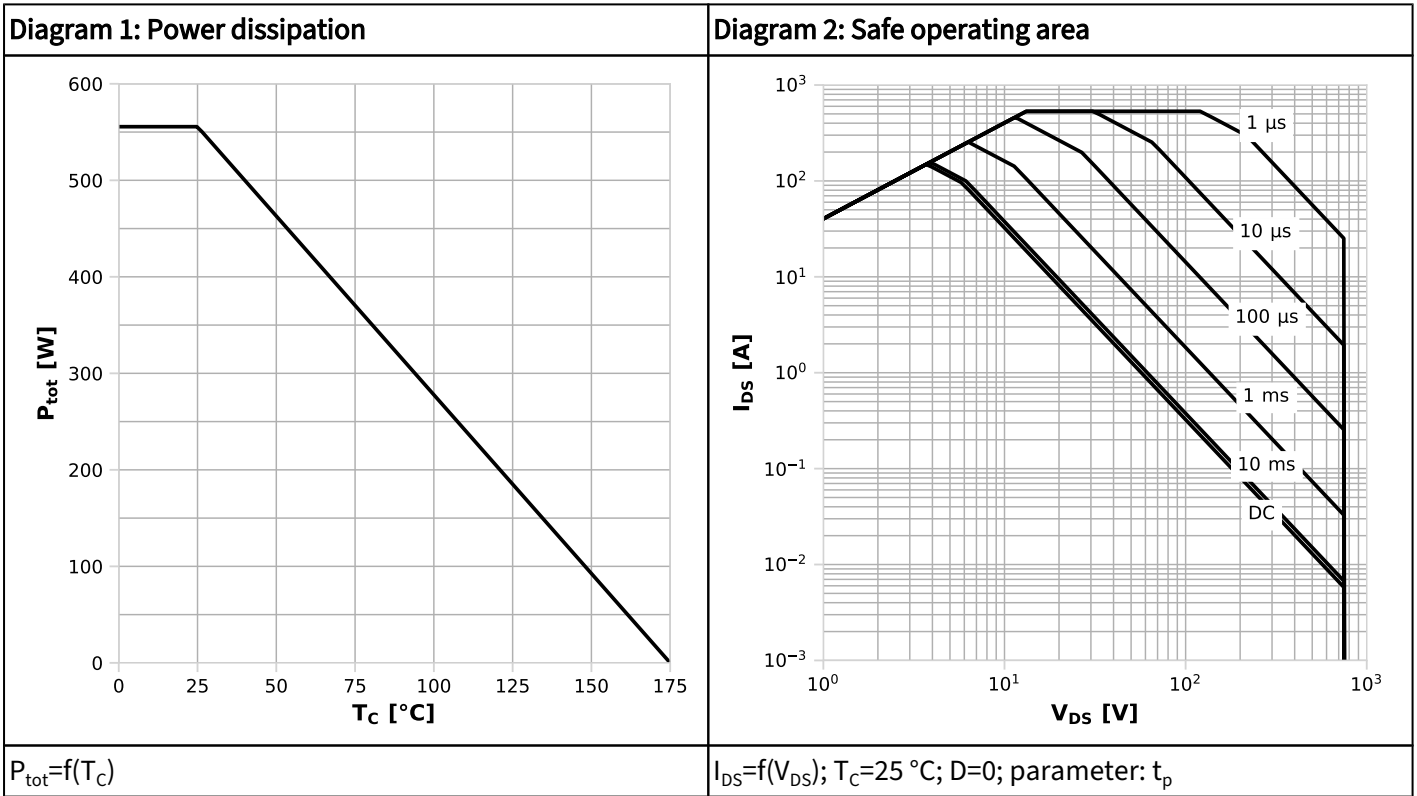
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	27	-	nC	$V_{DD} = 500\text{ V}$, $I_D = 80.9\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	Q_{GD}	-	23	-		
Total gate charge	Q_G	-	106	-		

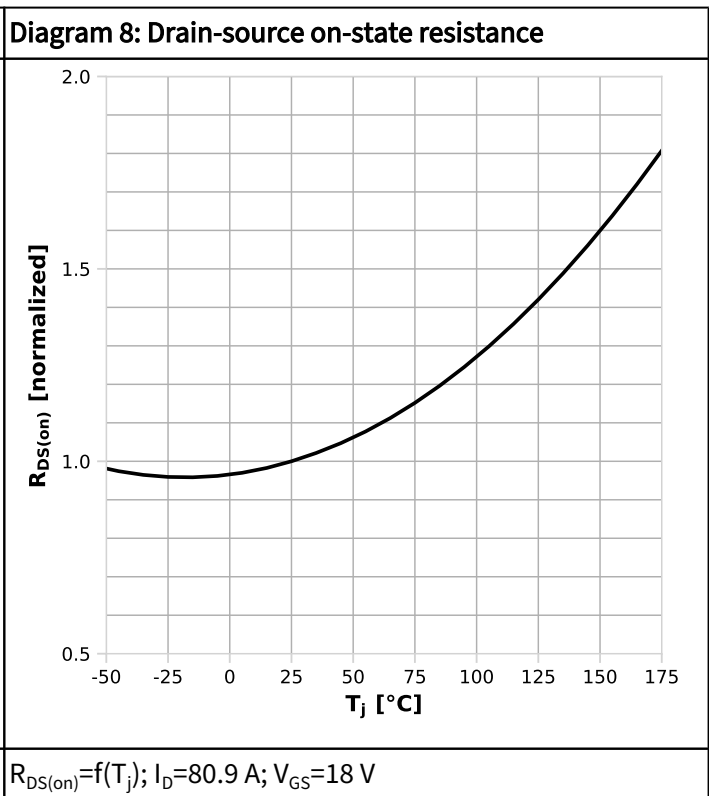
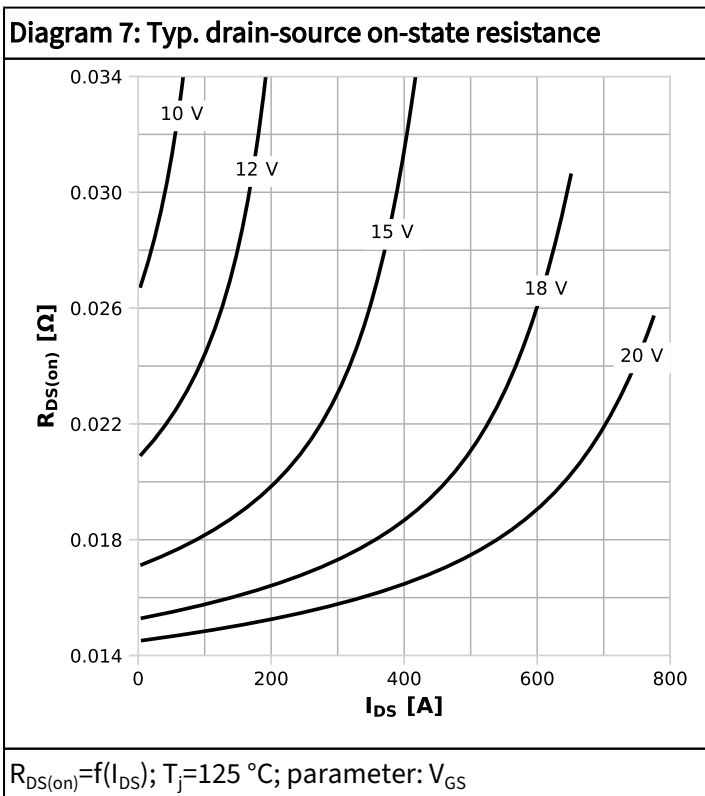
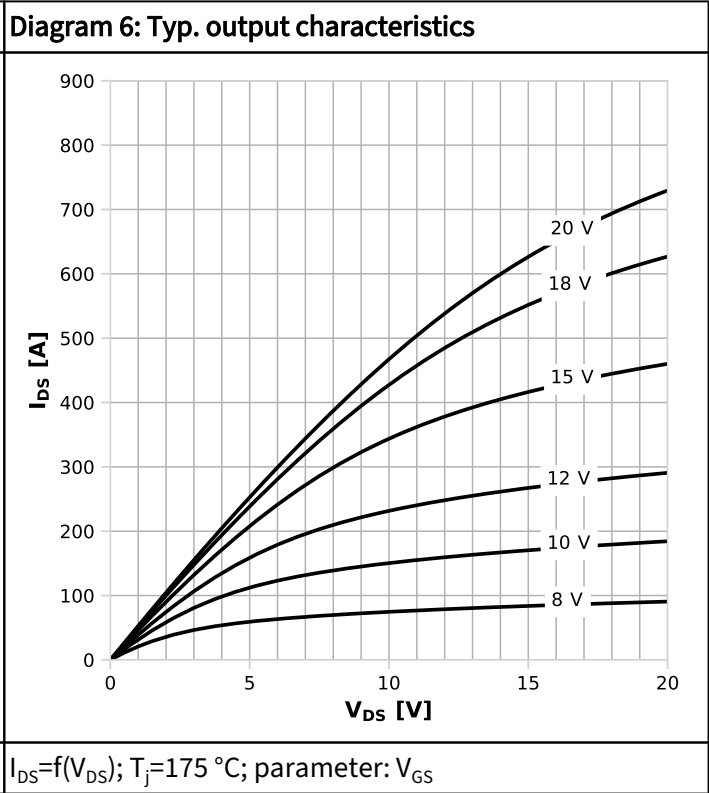
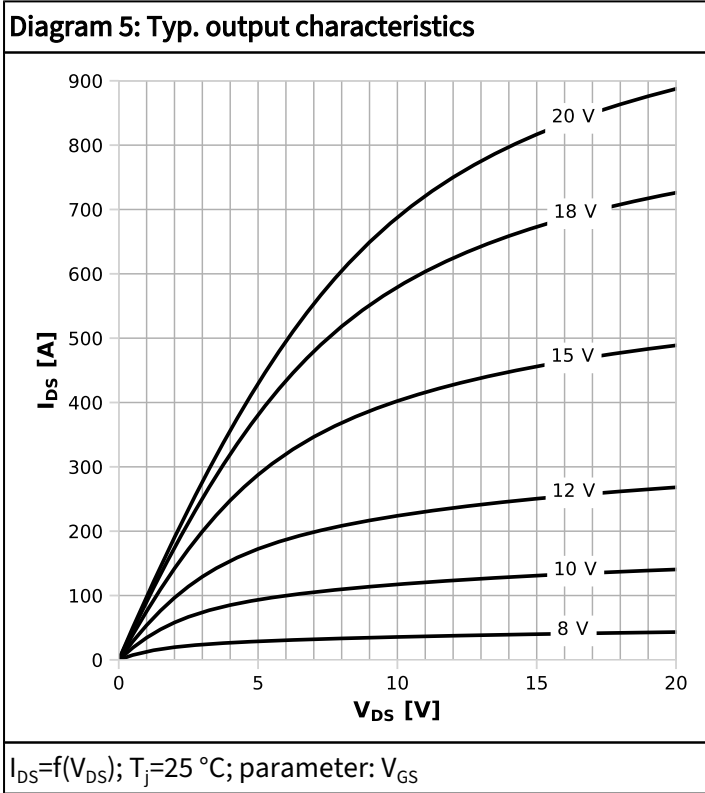
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	4.1	5.0	V	$V_{GS} = 0\text{ V}$, $I_S = 80.9\text{ A}$, $T_j = 25^\circ\text{C}$
			3.8	-		$V_{GS} = 0\text{ V}$, $I_S = 80.9\text{ A}$, $T_j = 175^\circ\text{C}$
MOSFET forward recovery time	t_{fr}	-	16	-	ns	$V_{DD} = 500\text{ V}$, $I_S = 80.9\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9
MOSFET forward recovery charge ¹²⁾	Q_{fr}	-	311	-	nC	
MOSFET peak forward recovery current	I_{frm}	-	39	-	A	

12) Q_{fr} includes Q_{oss} .

5 Electrical characteristics diagrams





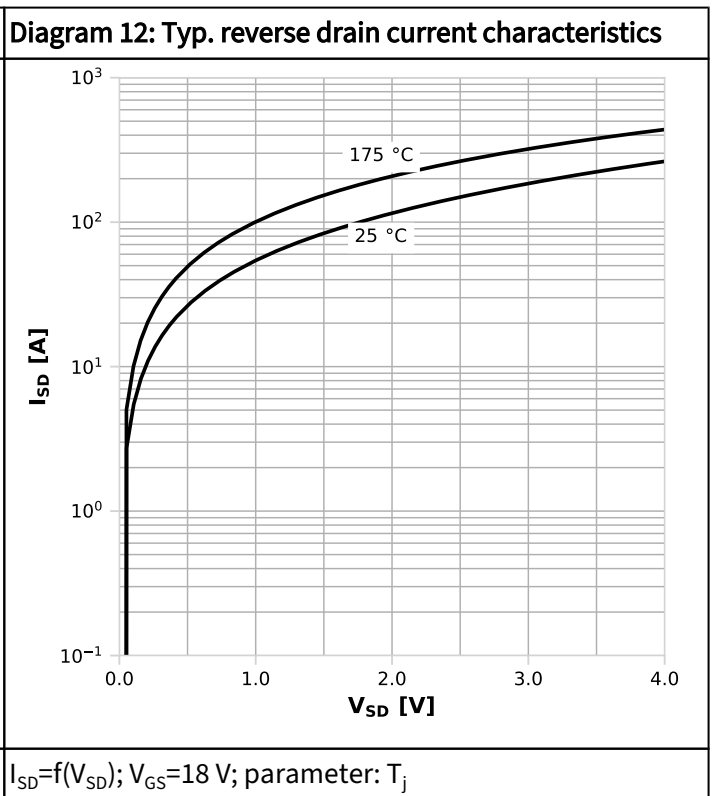
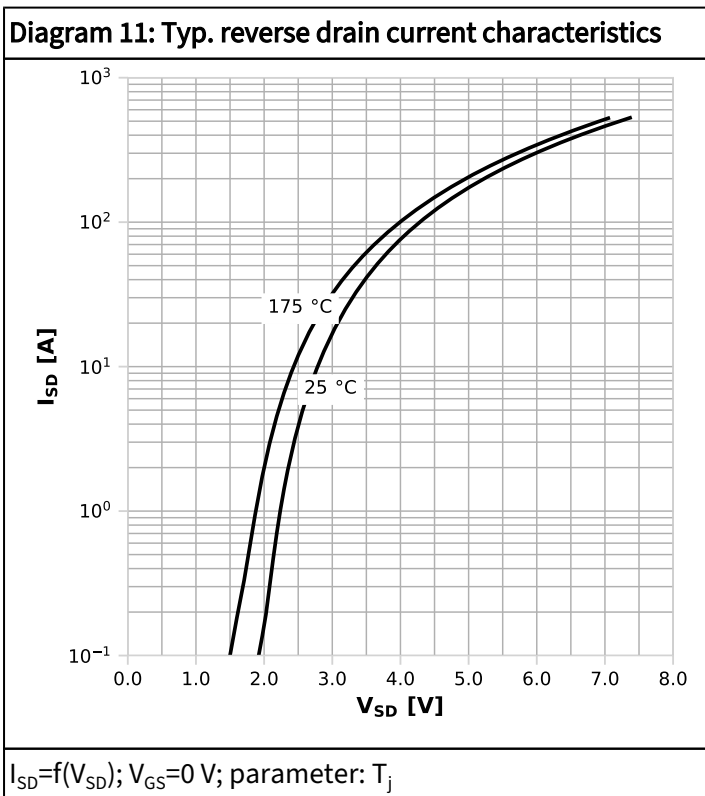
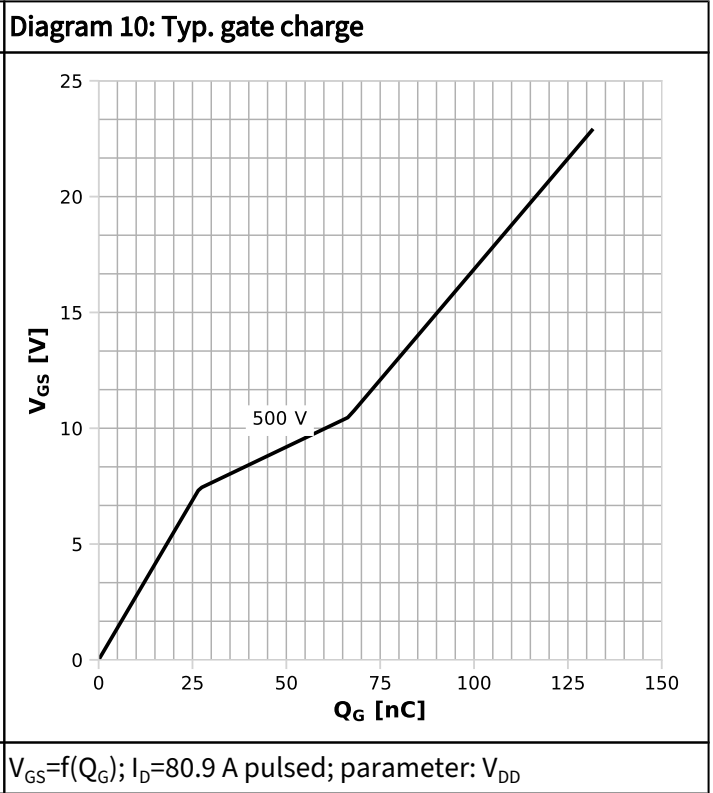
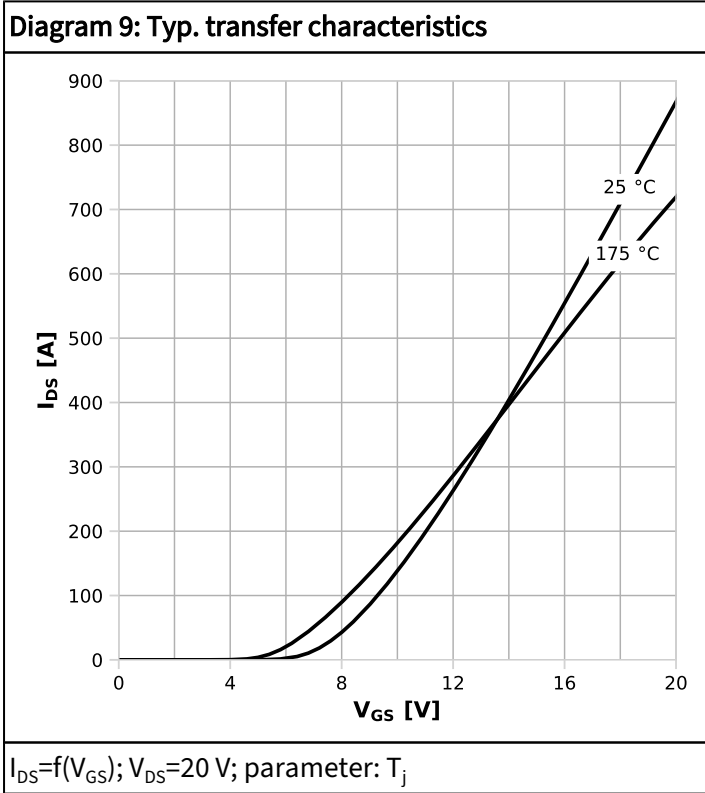
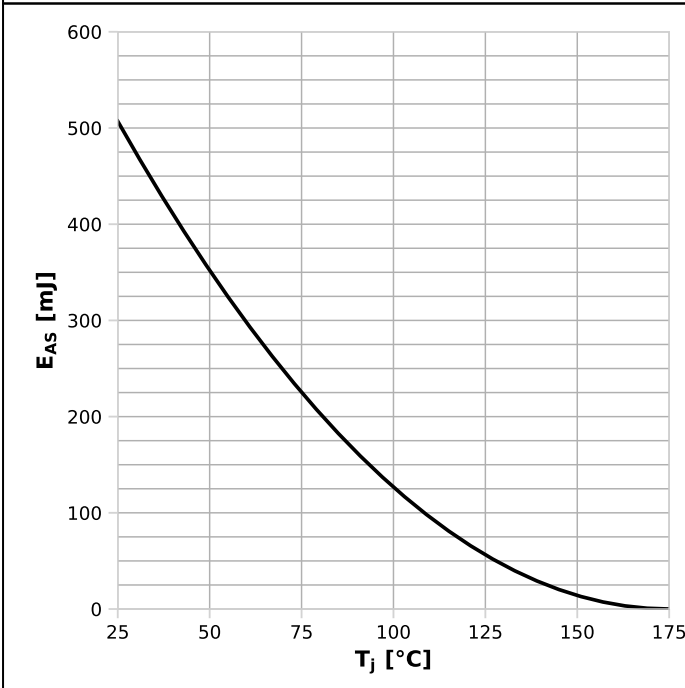
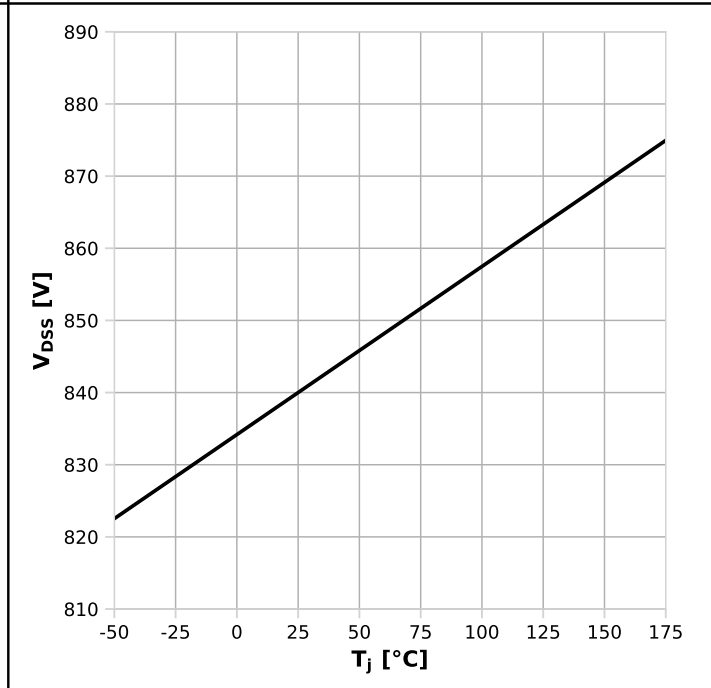


Diagram 13: Avalanche energy



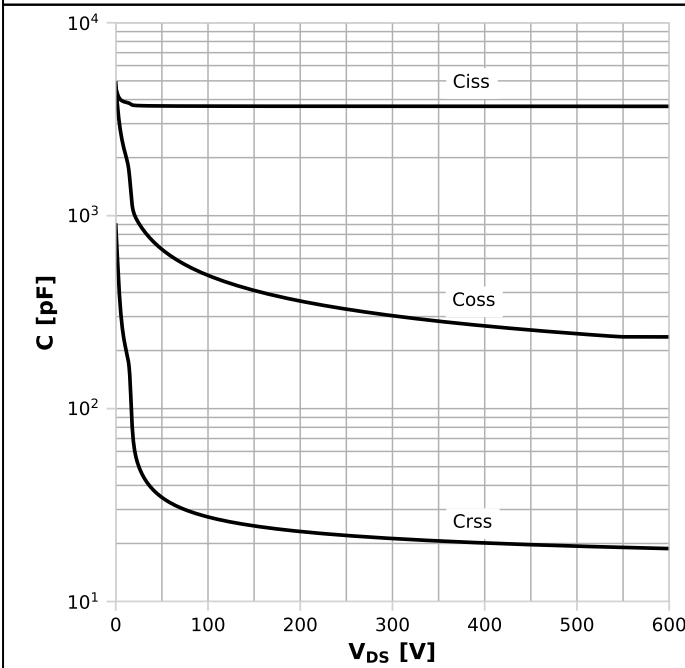
$E_{AS}=f(T_j); I_D=19.0\text{ A}; V_{DD}=50\text{ V}$

Diagram 14: Drain-source breakdown voltage



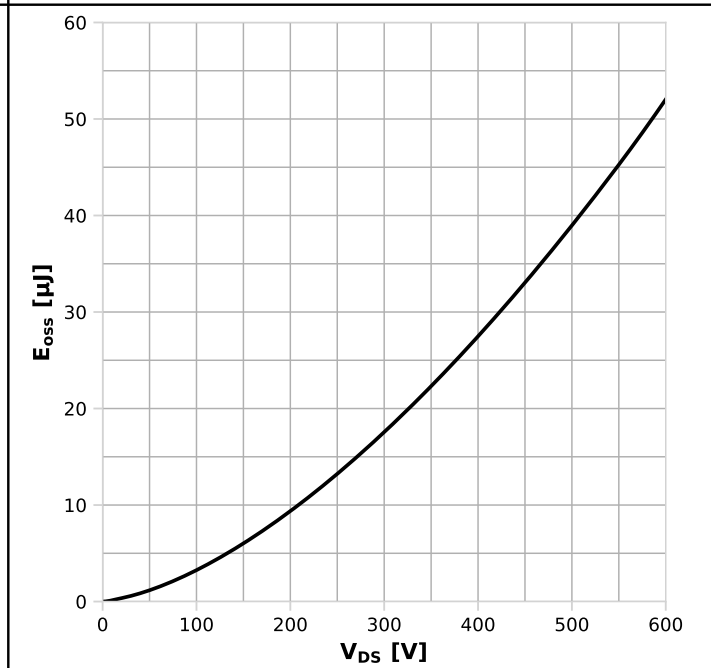
$V_{DSS}=f(T_j); I_D=1.78\text{ mA}$

Diagram 15: Typ. capacitances



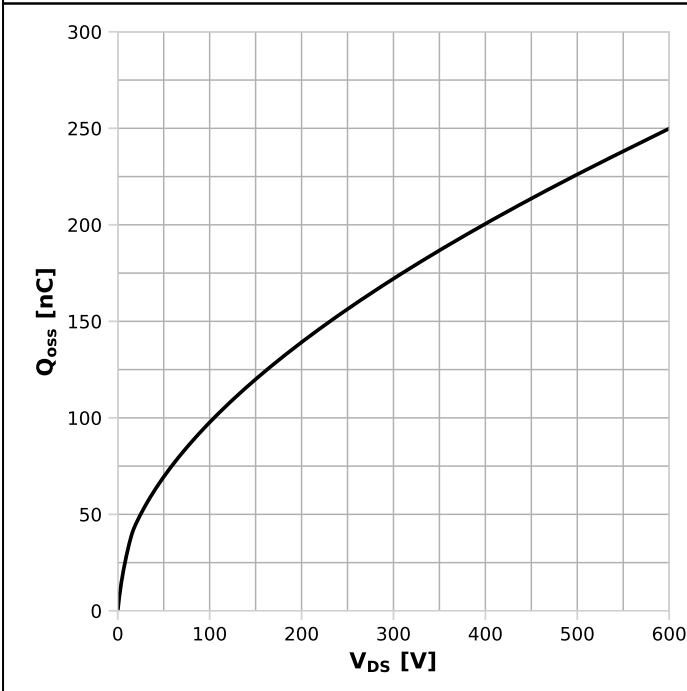
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 16: Typ. Coss stored energy



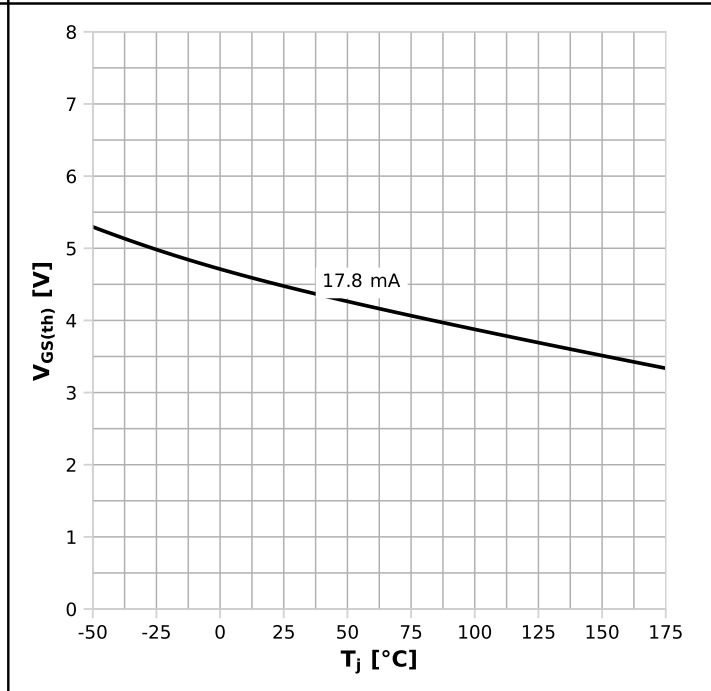
$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



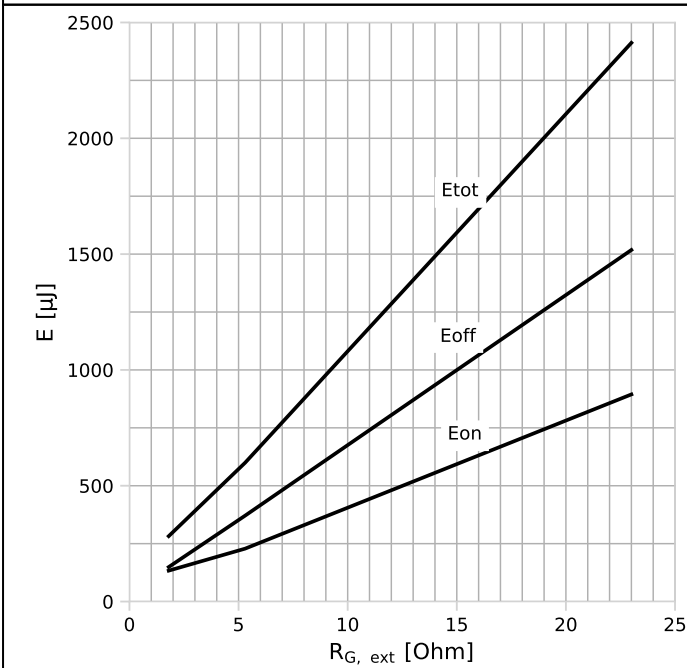
$Q_{oss}=f(V_{DS})$

Diagram 18: Typ. gate threshold voltage



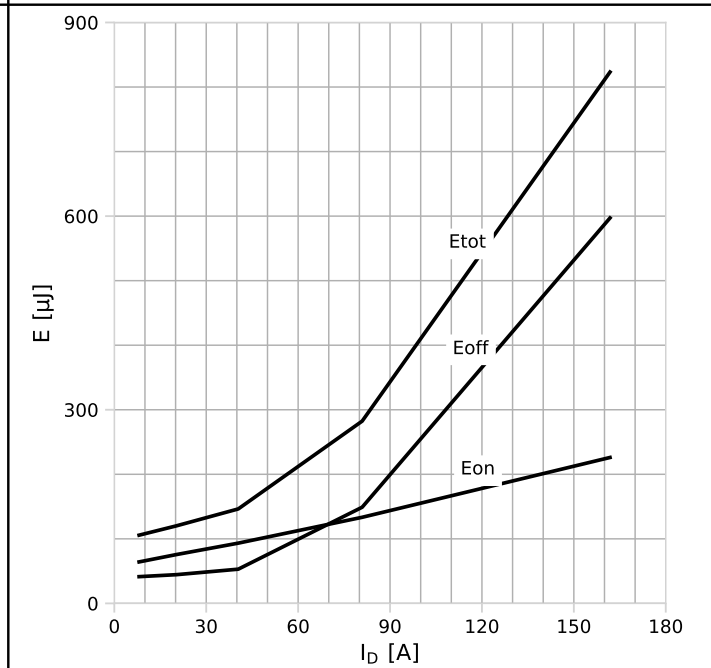
$V_{GS(th)}=f(T_J), V_{GS}=V_{DS};$ parameter: I_D

Diagram 19: Typ. Switching Losses vs R_{G,ext}

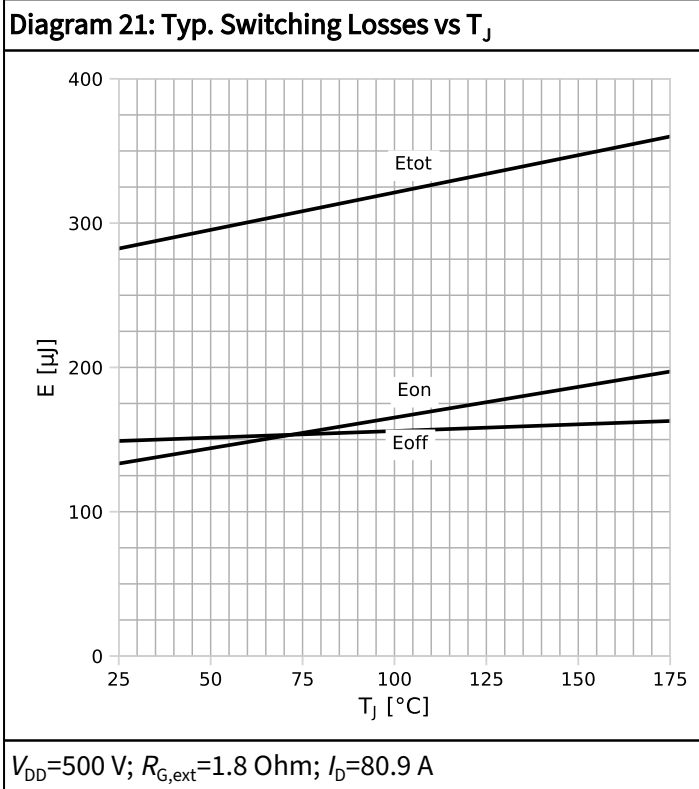


$V_{DD}=500\text{ V}; I_D=80.9\text{ A}; T_J=25\text{ °C}$

Diagram 20: Typ. Switching Losses vs switching current



$V_{DD}=500\text{ V}; R_{G,ext}=1.8\text{ Ohm}; T_J=25\text{ °C}$



6 Test circuits

Table 9 Body diode characteristics

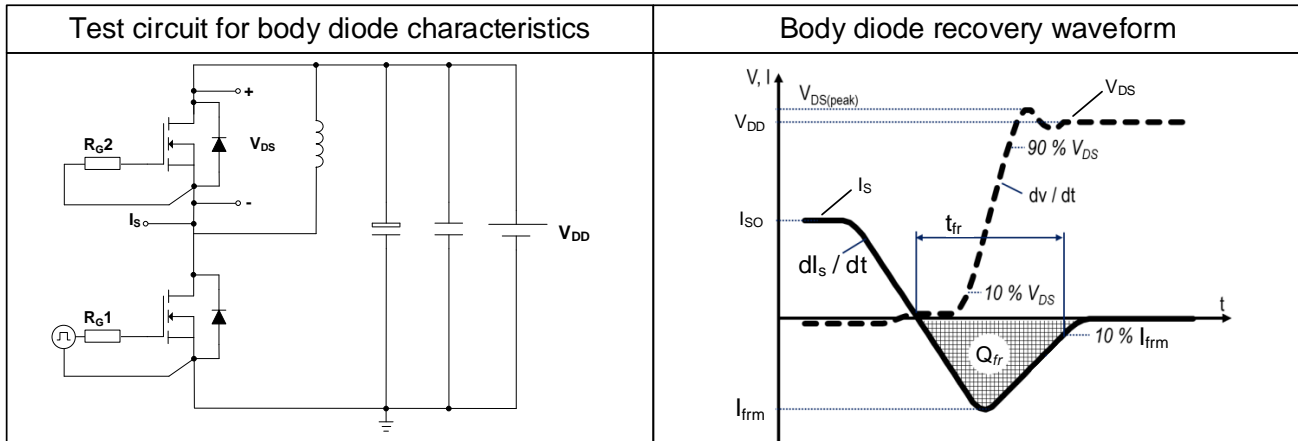


Table 10 Switching times

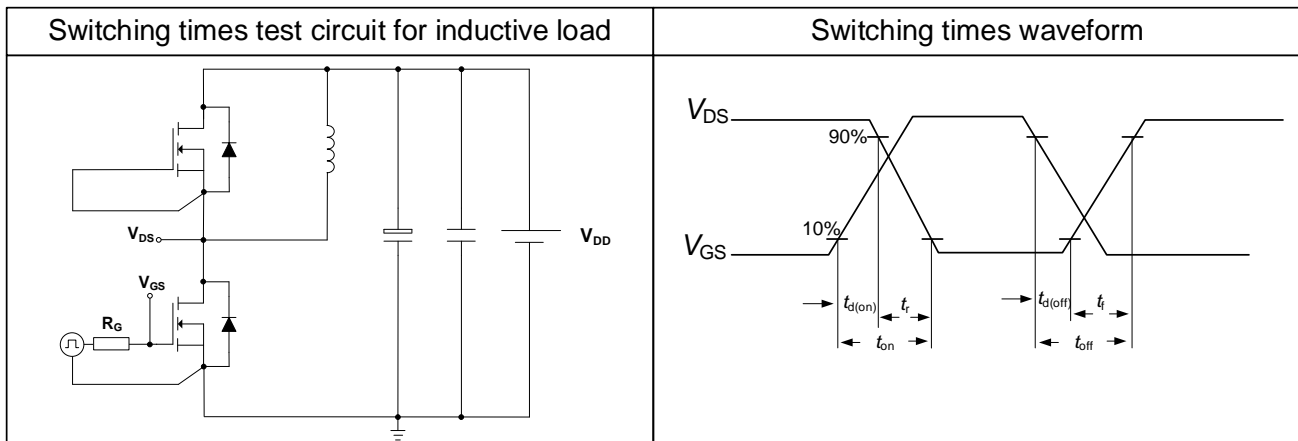
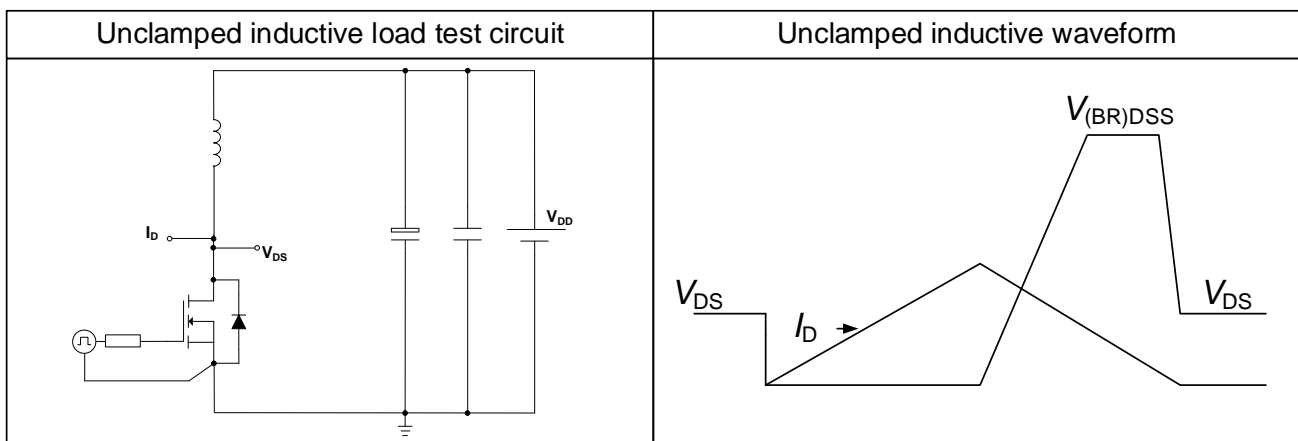


Table 11 Unclamped inductive load



7 Package outlines

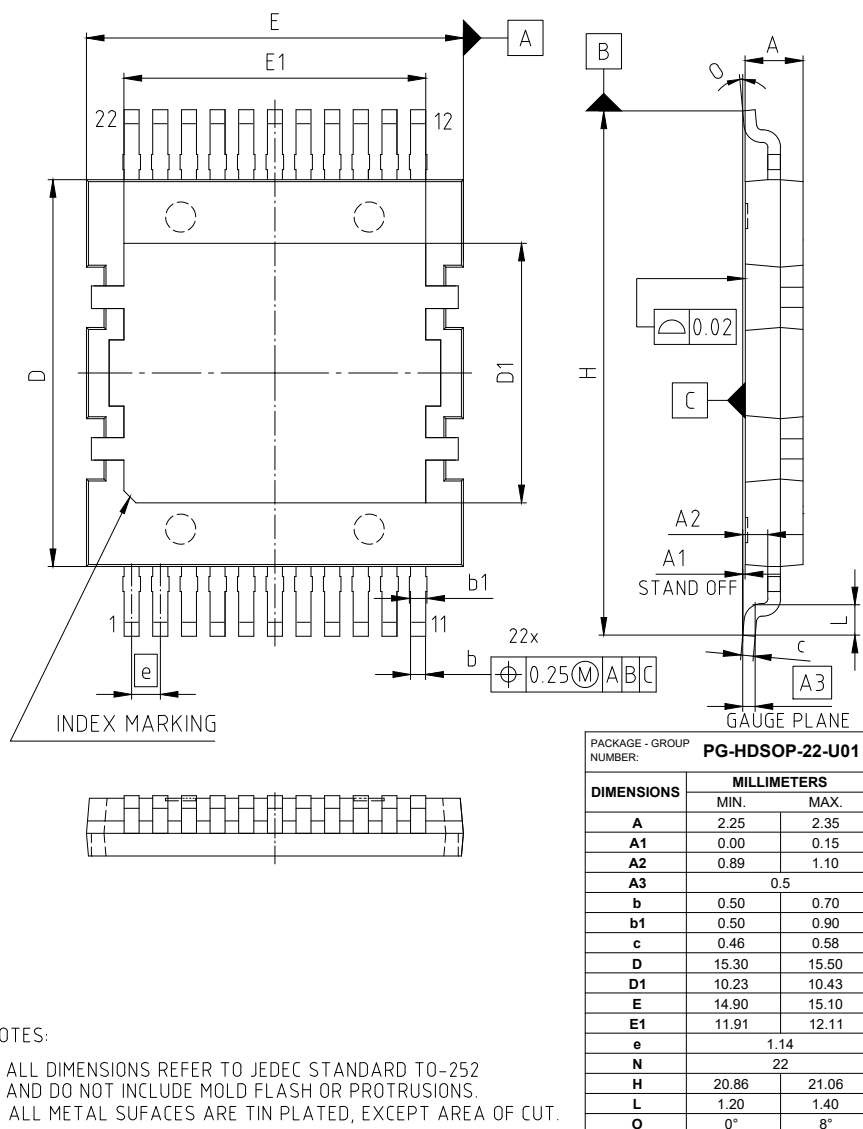


Figure 1 Outline PG-HDSOP-22, dimensions in mm

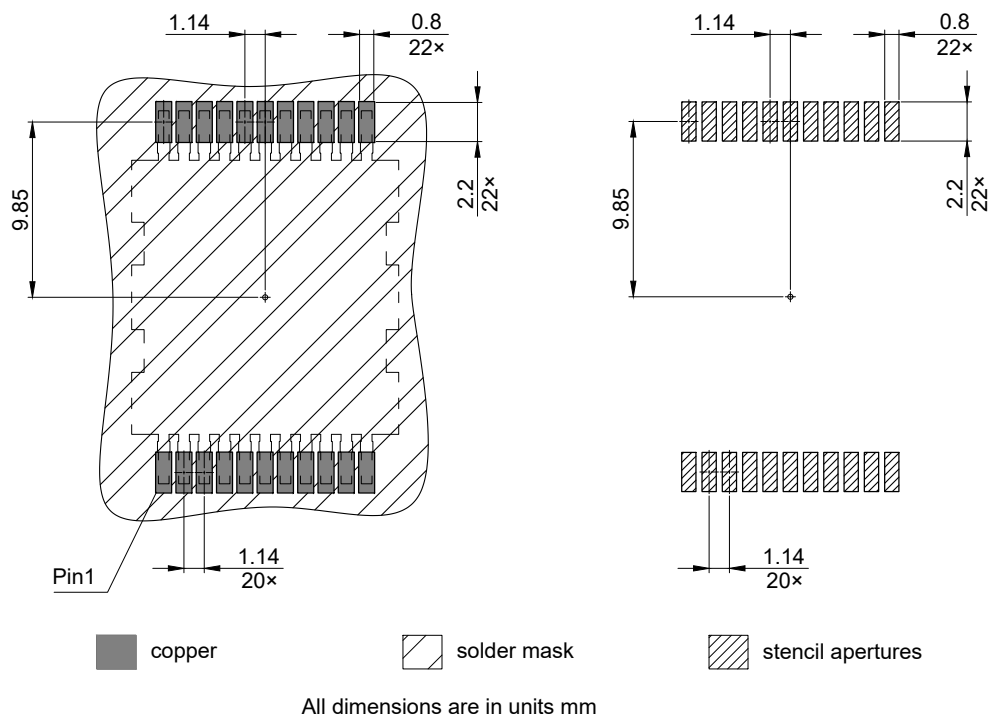


Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm

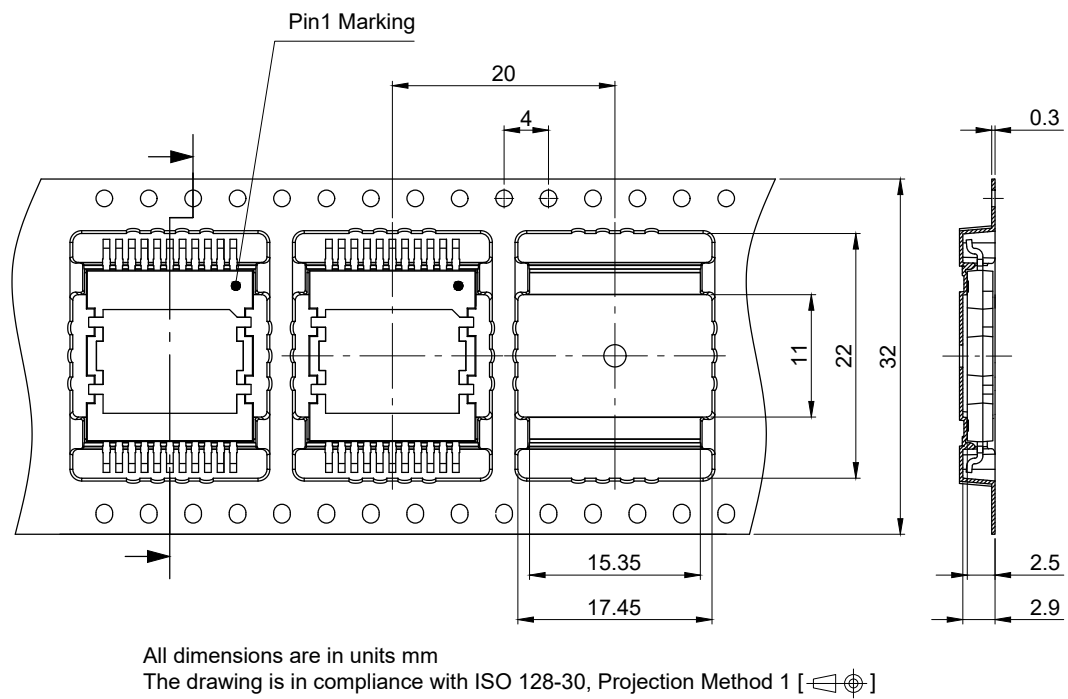


Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

8 Appendix A

Table 12 Related links

- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Application Note](#)
- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Simulation Model](#)
- [IFX Design tools](#)

Revision history

IMDQ75R011M2H

Revision 2025-09-17, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-09-17	Release of final version

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