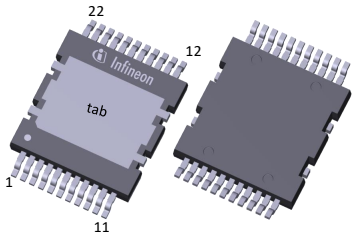
CoolSiC™ BDS 750 V G2

750 V CoolSiC™ Bidirectional switch (BDS)

Built on rugged CoolSiC™ G2 technology, it integrates two SiC power switches in a dual-die common-drain architecture within a top-side-cooled Q-DPAK package, simplifying system design and enabling next-generation topologies. Designed for modern power grids and energy systems, it delivers high reliability, efficiency, and low lifetime TCO.

PG-HDSOP-22



Features

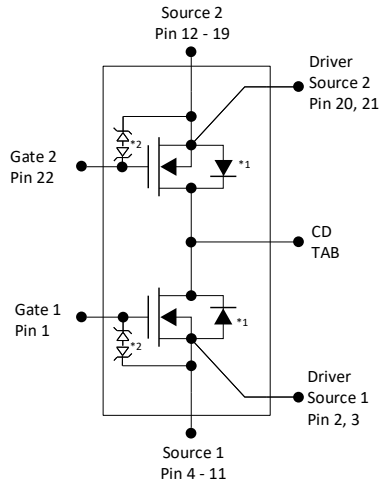
- Two dies in back to back configuration
- Overload operation up to T_j = 200°C for 100 h
- Ready for native liquid cooling
- Short circuit ruggedness (typ. 2 µs)
- 100% avalanche tested

Benefits

- Lowest system TCO through full-load compliance and simpler design
- Maximum hard-switching efficiency for lower energy losses
- Enhanced thermal performance for longer lifetime
- Robust 750 V CoolSiC™ technology
- Up to 66% lower parasitic inductance for reliable switching

Potential applications

- HVDC AI PSU, BBU, CBU
- Residential Solar and ESS
- eVTOL CSI Drive
- Bidirectional EV charging
- HVAC Indirect Matrix Converter
- Solid-State Circuit Breaker



**1: Internal body diode*
**2: Integrated ESD diode*

Product validation

Qualified according to relevant JEDEC tests.

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction. When paralleling MOSFETs the placement of the gate resistor is generally recommended to be in series to the Driver Source instead of the Gate.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{SS} over full $T_{j,range}$	±750	V
$R_{SS(on),typ}$	66.0	mΩ
$R_{SS(on),max}$	82.5	mΩ
$Q_{G,typ}$	37	nC
$I_{SS,pulse}$	164	A
$Q_{oss,typ}$ @ 500 V	87	nC
$E_{oss,typ}$ @ 500 V	15.4	µJ

Hal Pb RoHS

Part number	Package	Marking	Related links
IMDQ75B066M2H	PG-HDSOP-22	75R066B2	see Appendix A

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1 Maximum ratings

at T_j = 25°C, unless otherwise specified. V_{GS1} = V_{GS2} = V_{GS} unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.
For applications with applied blocking voltage > 525 V, it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support.
"Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source voltage	V_{SS}	-750	-	750	V	static, V_{GS} = 0 V, T_j = -55°C to 175°C
Continuous DC source-to-source current [1]	$I_{SS,DC}$	-38	-	38	A	V_{GS} = 18 V, T_c = 25°C
		-26		26		V_{GS} = 18 V, T_c = 100°C
Continuous DC source-to-source current, diode mode [1]	$I_{SS,DC}$	-37	-	37	A	V_{GSx} = 0 V, V_{GSy} = 18 V, T_c = 25°C
Peak source-to-source current [2]	I_{SSM}	-164	-	164	A	V_{GS} = 18 V, T_c = 25°C
Peak source-to-source current, diode mode [2]	I_{SSM}	-164	-	164	A	V_{GSx} = 0 V, V_{GSy} = 18 V, t_p ≤ 250 ns
		-37		37		V_{GSx} = 0 V, V_{GSy} = 18 V
Avalanche energy, single pulse	E_{AS}	-	-	169	mJ	I_{SS} = 6.3 A, V_{DD} = 50 V; see table 11
Avalanche energy, repetitive	E_{AR}			0.84		
Avalanche current, single pulse	I_{AS}	-	-	6.3	A	-
MOSFET *dv/dt* ruggedness	*dv/dt*	-	-	200	V/ns	V_{SS} = 0…500 V
Gate source voltage (static) [3]	V_{GS}	-7	-	23	V	-
Gate source voltage (transient)	V_{GS}	-11	-	25	V	t_p ≤ 500 ns, duty cycle ≤ 1%
Power dissipation	P_{tot}	-	-	217	W	T_c = 25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		
Extended operating junction temperature [4]	T_j	-	-	200	°C	≤ 100 h in the application lifetime
Mounting torque	-	-	-	n.a.	Ncm	-
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_c = 25°C, t = 1 min

1) Limited by $T_{j,max}$.
2) Pulse width t_{pulse} limited by $T_{j,max}$.
3) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.
4) Up to 7500 temperature cycles, where maximum delta T is limited to 100 K.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case [5]	$R_{th(j-c)}$	-	0.49	0.69	K/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

[5] Thermal resistance for each die.

3 Operating range

V_{GS1} = V_{GS2} = V_{GS} unless otherwise specified.

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$		0			

4 Electrical characteristics

at T_j = 25°C, unless otherwise specified. V_{GS1} = V_{GS2} = V_{GS} unless otherwise specified.

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source breakdown voltage [6]	$V_{(BR)SS}$	-840	-	840	V	V_{GS} = 0 V, I_{SS} = 0.59 mA
Gate threshold voltage [7]	$V_{GS(th)}$	3.5	4.5	5.6	V	V_{SS} = V_{GS}, I_{SS} = 5.9 mA, T_j = 25°C
		-	3.3	-		V_{SS} = V_{GS}, I_{SS} = 5.9 mA, T_j = 175°C
Zero gate voltage source-to-source current	$I_{SS,leakage}$	-	1	75	µA	V_{SS} = 750 V, V_{GS} = 0 V, T_j = 25°C
			10	-		V_{SS} = 750 V, V_{GS} = 0 V, T_j = 175°C
Gate-source leakage current [8]	$I_{GS,leakage}$	-	-	1	µA	V_{GS} = 23V, V_{SS} = 0 V, T_j = 25°C
				-1		V_{GS} = -7V, V_{SS} = 0 V, T_j = 25°C
Forward transconductance	g_{fs}	-	16.0	-	S	I_{SS} = 27.0 A, V_{SS} = 20 V
Source-to-source on-state resistance	$R_{SS(on)}$	-	86.0	-	mΩ	V_{GS} = 15 V, I_{SS} = 27.0 A, T_j = 25°C
			66.0	82.5		V_{GS} = 18 V, I_{SS} = 27.0 A, T_j = 25°C
			59.0	-		V_{GS} = 20 V, I_{SS} = 27.0 A, T_j = 25°C
Source-to-source on-state resistance [9]	$R_{SS(on)}$	-	104.9	131.0	mΩ	V_{GS} = 18 V, I_{SS} = 27.0 A, T_j = 150°C
Source-to-source on-state resistance	$R_{SS(on)}$	-	119.0	-	mΩ	V_{GS} = 18 V, I_{SS} = 27.0 A, T_j = 175°C
Short-circuit withstand time [9]	t_{SC}	-	2.0	-	µs	V_{DD} = 500 V, V_{GS} = 18 V, $R_{G,on}$ = 2.3 Ω, $R_{G,off}$ = 15 Ω, $V_{SS(peak)}$ < 750 V
Internal gate resistance	$R_{G,int}$	-	2.5	-	Ω	f = 1 MHz

[6] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

[7] Tested after pre-conditioning pulse at V_{GS} = +20 V. “Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

[8] Tested individually for each die.

[9] Specified by design, not subject to production test.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1300	-	pF	V_{GS} = 0 V, V_{SS} = 500 V, f = 250 kHz
Reverse transfer capacitance	C_{rss}		7.1			
Output capacitance [10]	C_{oss}	-	100	130	pF	V_{GSx} = 0 V, V_{GSy} = 18 V, V_{SS} = 500 V, f = 250 kHz
			95	124		V_{GS} = 0 V, V_{SS} = 500 V, f = 250 kHz
Output charge [10]	Q_{oss}	-	87	113	nC	calculation based on C_{oss} with V_{GSx} = 0 V, V_{GSy} = 18 V
			76	99		calculation based on C_{oss} with V_{GS} = 0 V
Effective output capacitance, energy related [11]	$C_{o(er)}$	-	124	-	pF	V_{GS} = 0 V, V_{SS} = 0…500 V
Effective output capacitance, time related [12]	$C_{o(tr)}$	-	175	-	pF	I_{SS} = constant, V_{GS} = 0 V, V_{SS} = 0…500 V
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	V_{DD} = 500 V, V_{GS} = 0/18 V, I_{SS} = 27.0 A, $R_{G,ext}$ = 1.8 Ω L_{stray} = 15 nH; see table 10
Rise time	t_r		8		ns	
Turn-off delay time	$t_{d(off)}$		17		ns	
Fall time	t_f		6		ns	
Turn-ON switching losses [13]	E_{on}		46		µJ	
Turn-OFF switching losses [13]	E_{off}		20		µJ	
Total switching losses [13]	E_{tot}		66		µJ	

[10] Maximum specification is defined by calculated six sigma upper confidence bound.

[11] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{SS} is rising from 0 to 500 V.

[12] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{SS} is rising from 0 to 500 V.

[13] MOSFET used in half-bridge configuration without external diode. Parameter verified according to IEC 60747-8.

Table 7 Gate charge characteristics

Gate charge characteristics measured individually for each die.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	9.5	-	nC	V_{DD} = 500 V, I_{SS} = 27.0 A, V_{GS} = 0 to 18 V
Gate to drain charge	Q_{GD}		8.1			
Total gate charge	Q_G		37			

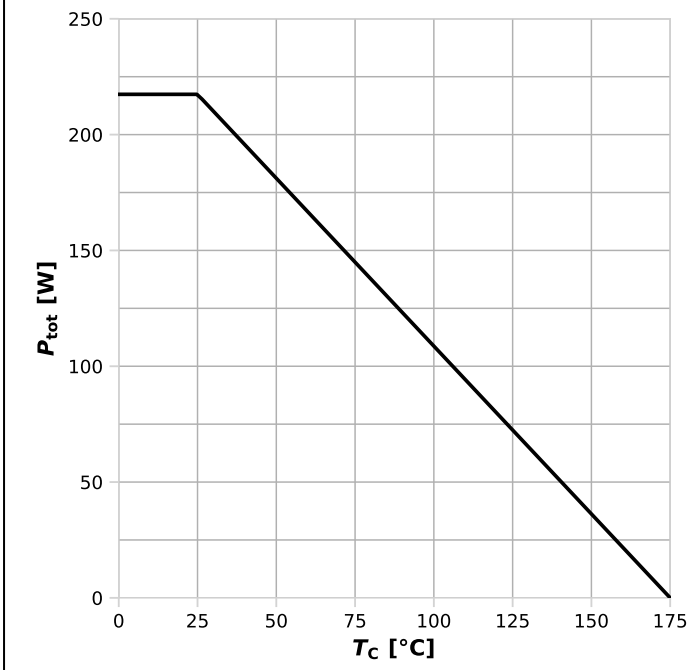
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source voltage, diode mode	$V_{SS,diode}$	-	5.0	-	V	V_{GSx} = 0 V, V_{GSy} = 18 V, I_{SS} = 27.0 A, T_j = 25°C
			5.3			V_{GSx} = 0 V, V_{GSy} = 18 V, I_{SS} = 27.0 A, T_j = 175°C
MOSFET forward recovery time	t_{fr}	-	8.0	-	ns	V_{DD} = 500 V, I_{SS} = 27.0 A, di_{SS}/dt = 4000 A/µs; see table 9
MOSFET forward recovery charge [14)]	Q_{fr}		89		nC	
MOSFET peak forward recovery current	I_{frm}		23		A	

14) Q_{fr} includes Q_{oss}

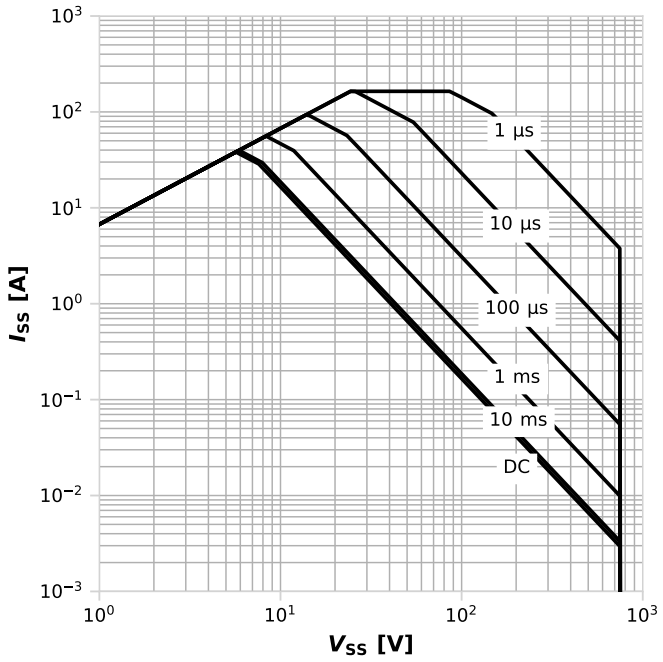
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



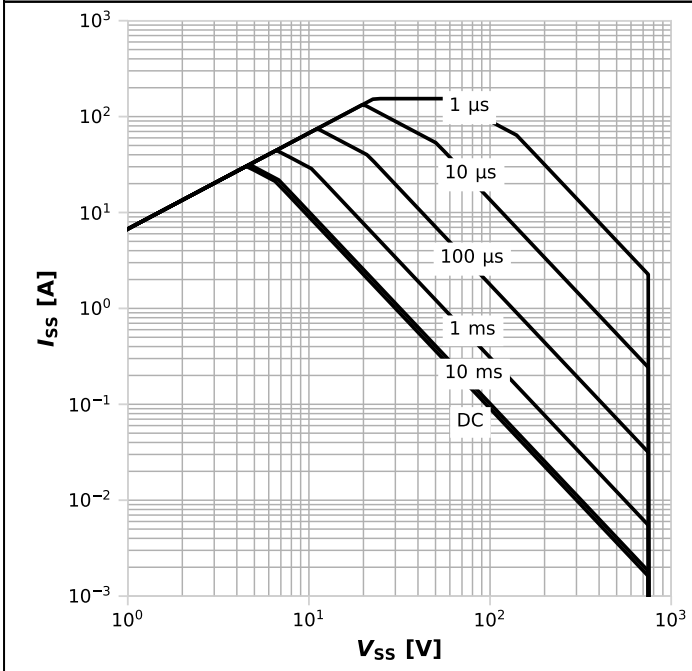
$P_{tot} = f(T_C)$

Diagram 2: Safe operating area



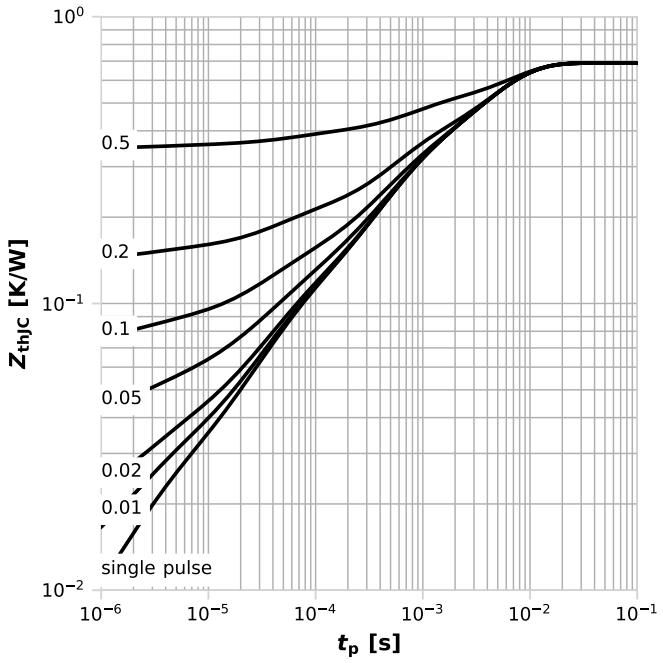
$I_{SS} = f(V_{SS})$; $T_C = 25°C$; $D = 0$; parameter: t_p

Diagram 3: Safe operating area



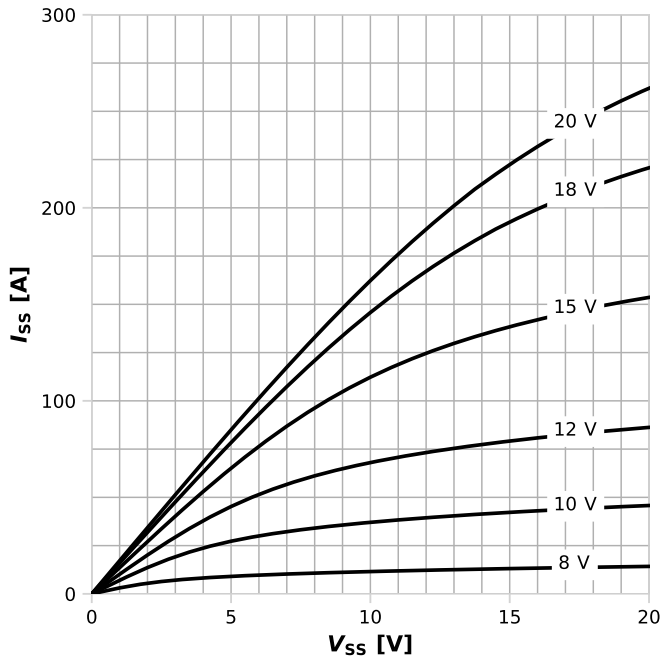
$I_{SS} = f(V_{SS})$; $T_C = 80°C$; $D = 0$; parameter: t_p

Diagram 4: Max. transient thermal impedance per die



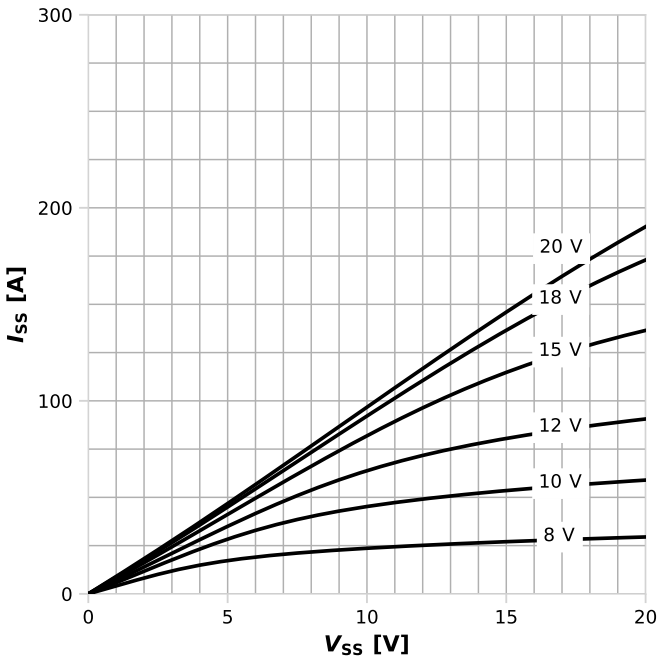
$Z_{thJC} = f(t_p)$; parameter: $D = t_p / T$

Diagram 5: Typ. output characteristics



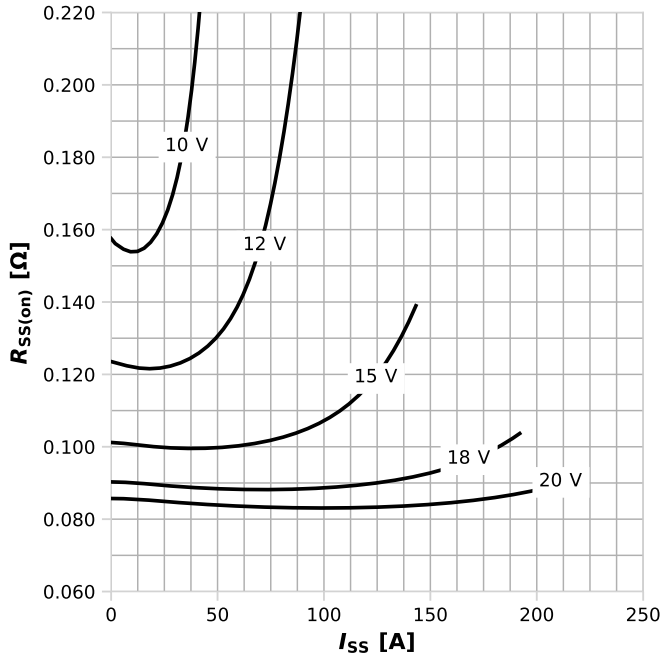
$I_{SS} = f(V_{SS})$; $T_j = 25°C$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



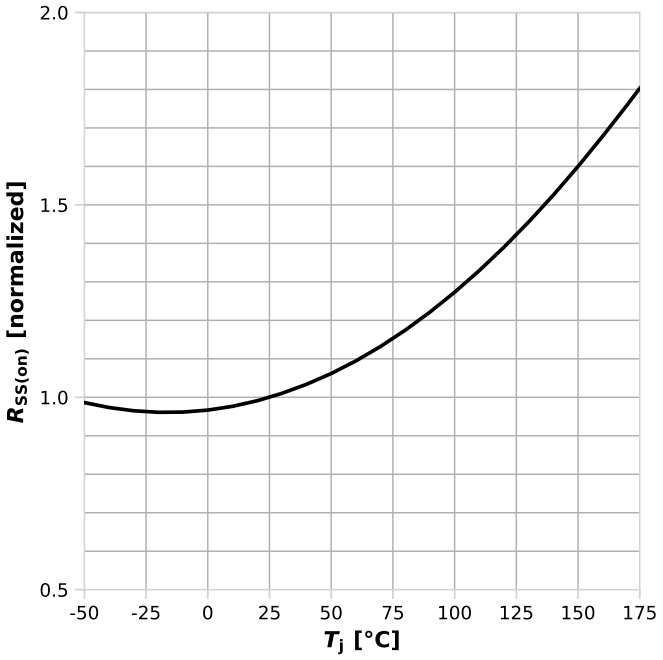
$I_{SS} = f(V_{SS})$; $T_j = 175°C$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



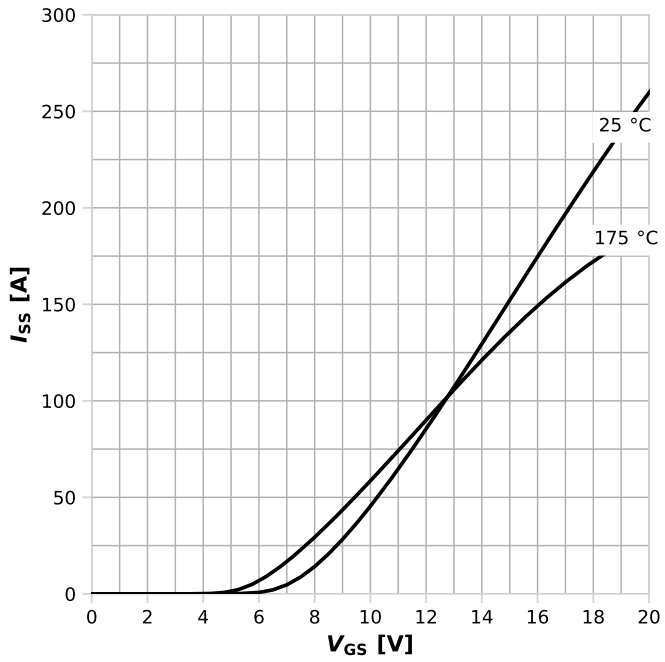
$R_{SS(on)} = f(I_{SS})$; $T_j = 125°C$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



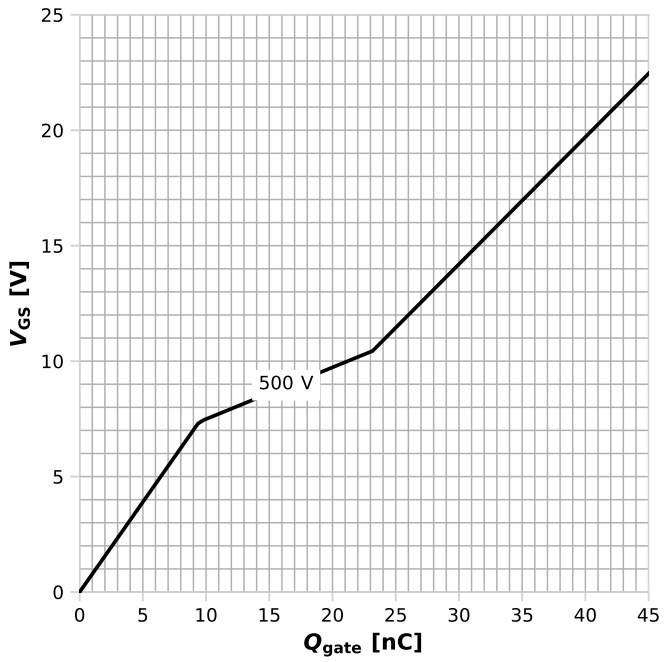
$R_{SS(on)} = f(T_j)$; $I_{SS} = 27.0$ A; $V_{GS} = 18$ V

Diagram 9: Typ. transfer characteristics



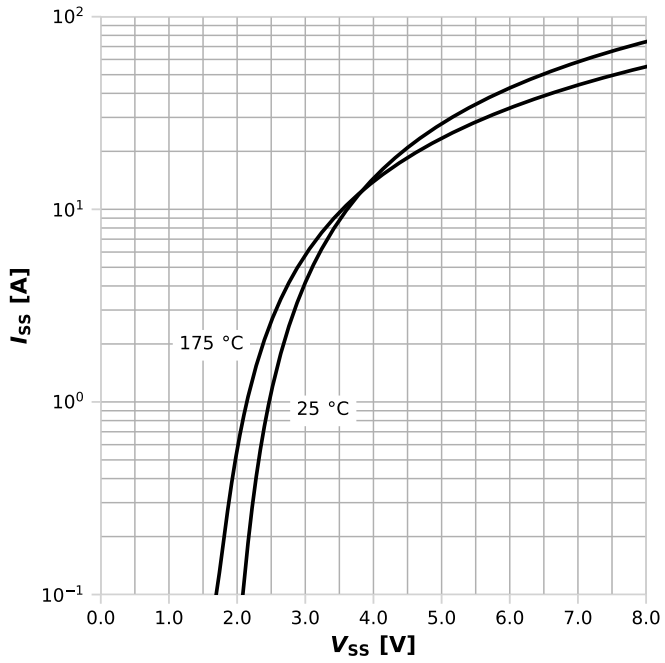
I_{SS}=f(V_{GS}); V_{SS} = 20 V; parameter: T_j

Diagram 10: Typ. gate charge



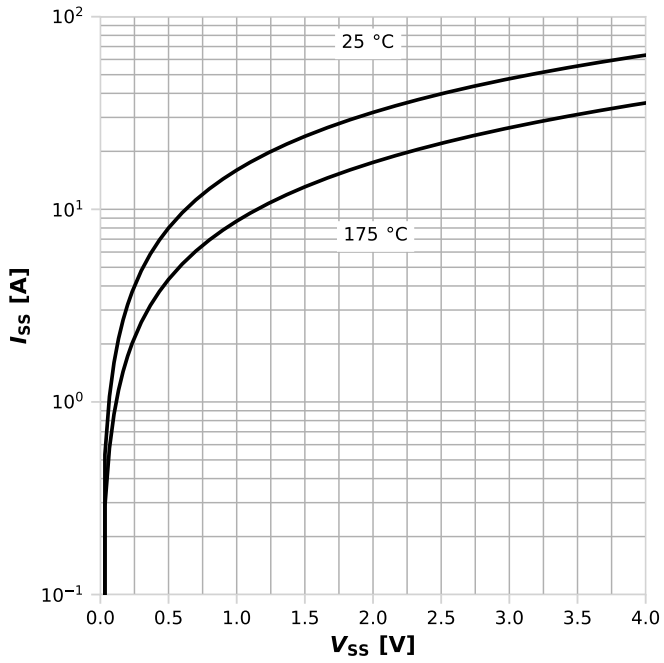
V_{GS} = f(Q_{gate}); I_{SS} = 27.0 A pulsed; parameter: V_{DD}

Diagram 11: Typ. reverse current characteristics



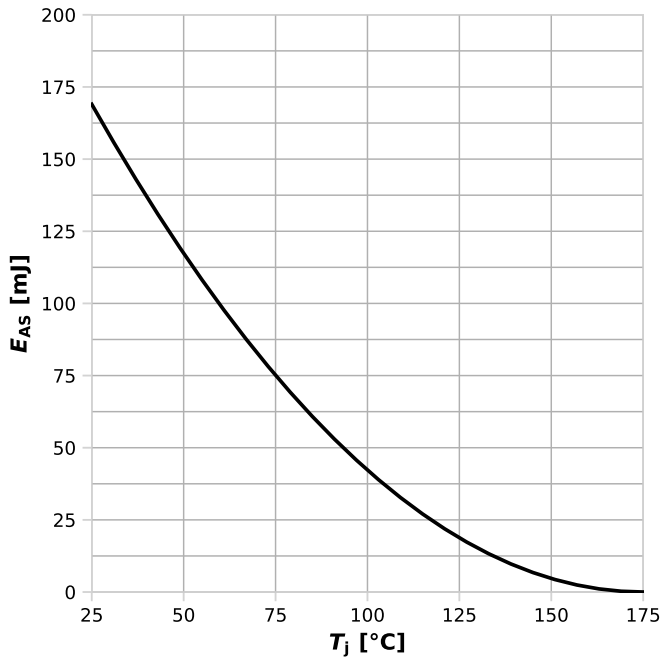
I_{SS} = f(V_{SS}); V_{GSx} = 18 V; V_{GSy} = 0 V; parameter: T_j

Diagram 12: Typ. reverse current characteristics



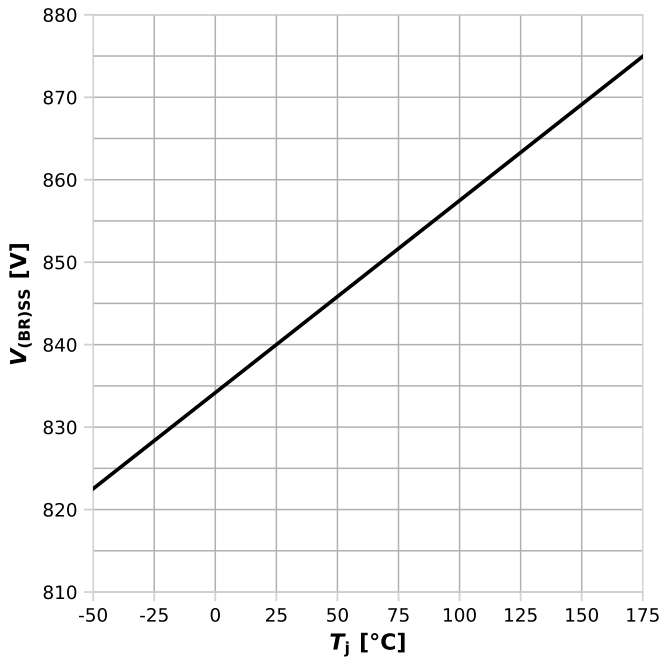
I_{SS} = f(V_{SS}); V_{GSx} = 18 V; V_{GSy} = 18 V; parameter: T_j

Diagram 13: Avalanche energy



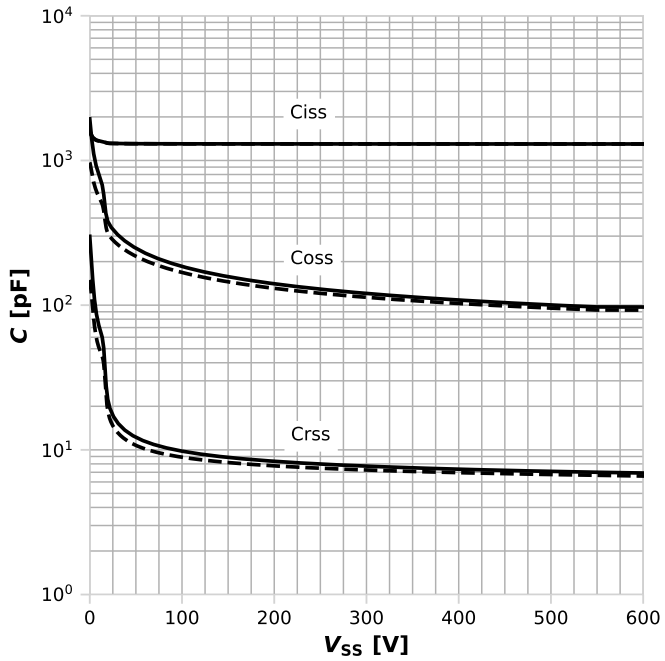
$E_{AS} = f(T_j)$; $I_{SS} = 6.3$ A; $V_{DD} = 50$ V

Diagram 14: Drain-source breakdown voltage



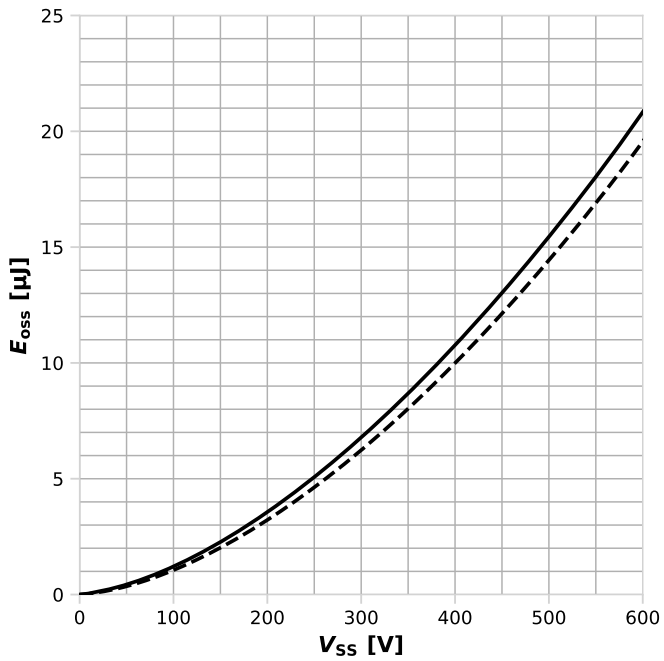
$V_{(BR)SS} = f(T_j)$; $I_{SS} = 0.59$ mA

Diagram 15: Typ. capacitances



$C = f(V_{SS})$; $f = 250$ kHz
solid: $V_{GSx} = 0$ V, $V_{GSy} = 18$ V; dashed: $V_{GSx} = 0$ V, $V_{GSy} = 0$ V

Diagram 16: Typ. Coss stored energy



$E_{oss} = f(V_{SS})$
solid: $V_{GSx} = 0$ V, $V_{GSy} = 18$ V; dashed: $V_{GSx} = 0$ V, $V_{GSy} = 0$ V

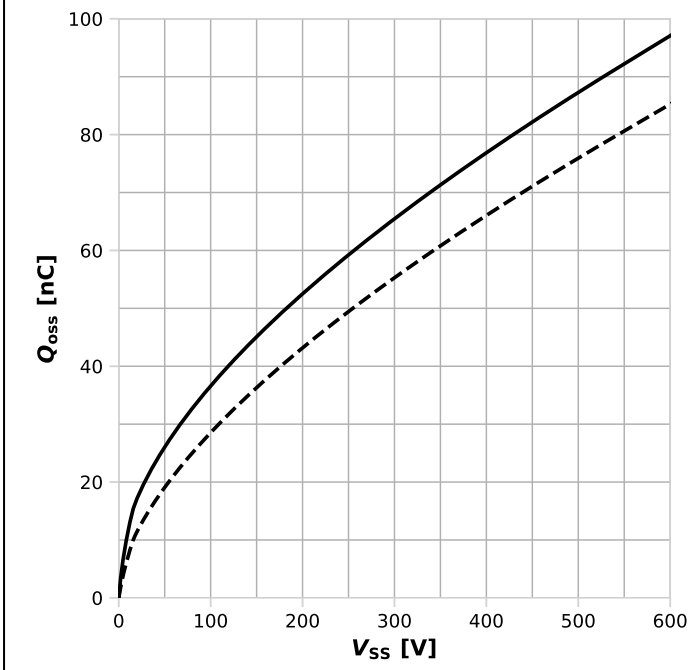
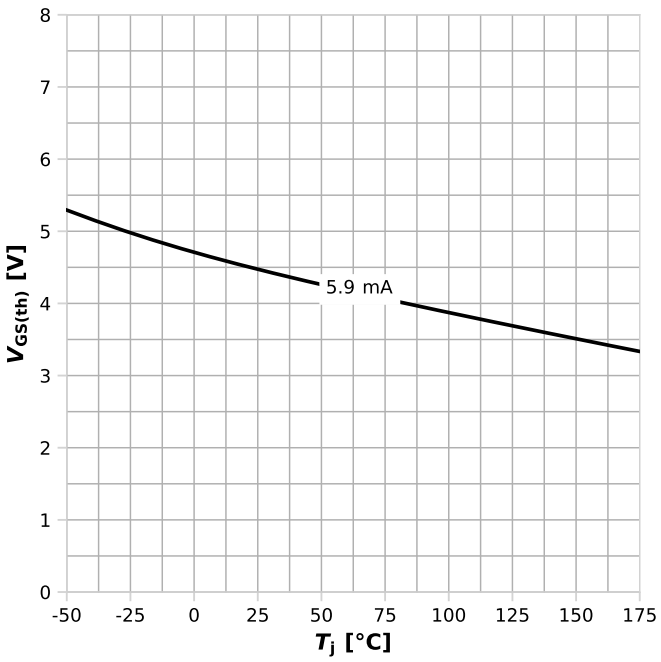
Diagram 17: Typ. Qoss output charge	Diagram 18: Typ. gate threshold voltage
	
$Q_{oss} = f(V_{SS})$ solid: V_{GSx} = 0 V, V_{GSy} = 18 V; dashed: V_{GSx} = 0 V, V_{GSy} = 0 V	$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{SS}$; parameter: I_{SS}

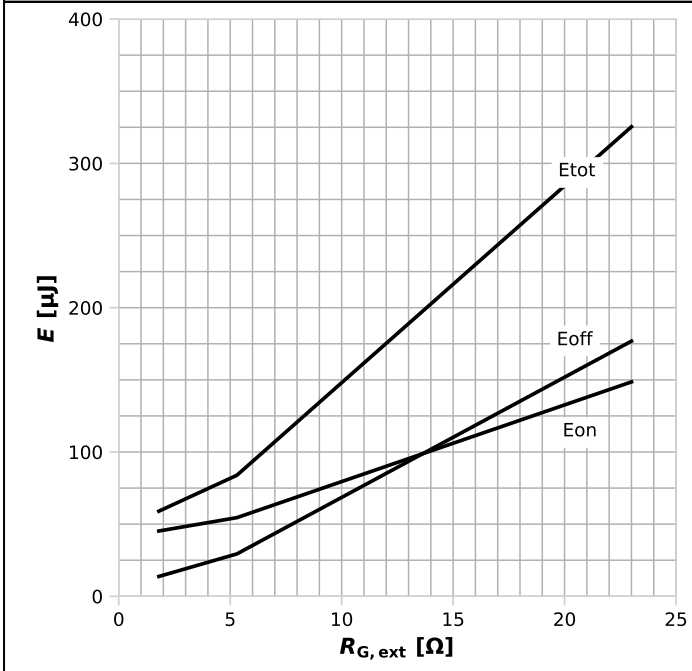
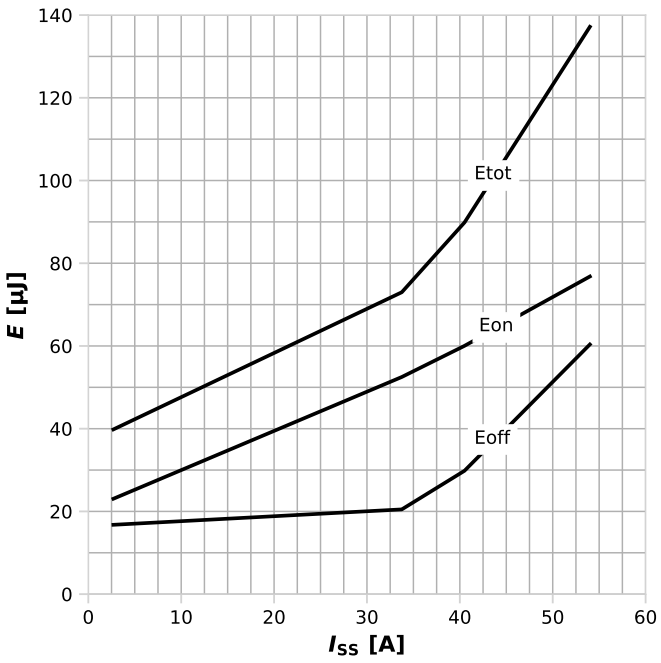
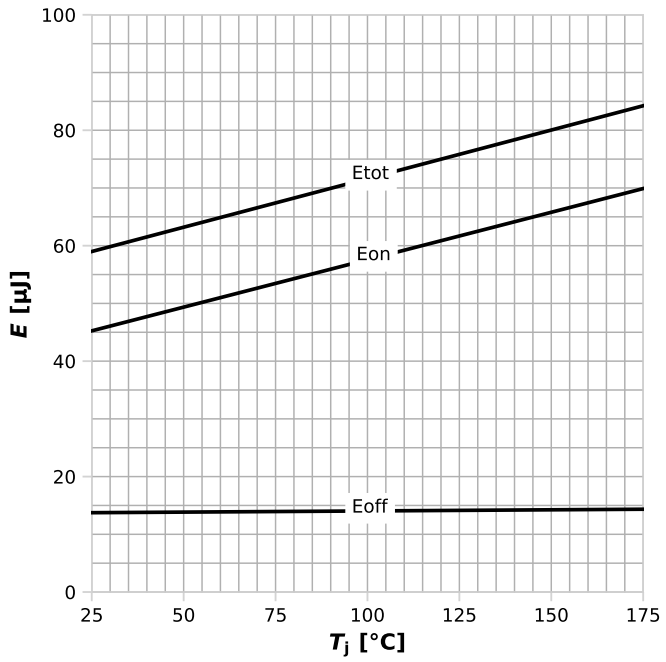
Diagram 19: Typ. Switching Losses vs $R_{G,ext}$	Diagram 20: Typ. Switching Losses vs switching current
	
V_{DD} = 500 V; I_{SS} = 27.0 A; T_j = 25°C	V_{DD} = 500 V; $R_{G,ext}$ = 1.8 Ω; T_j = 25°C

Diagram 21: Typ. Switching Losses vs T_j



V_{DD} = 500 V; $R_{G,ext}$ = 1.8 Ω; I_{SS} = 27.0 A

6 Test circuits

Table 9 Body diode characteristics

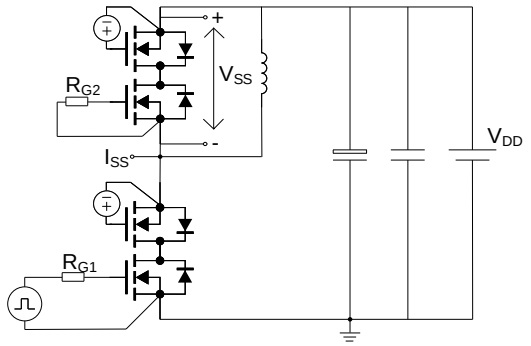
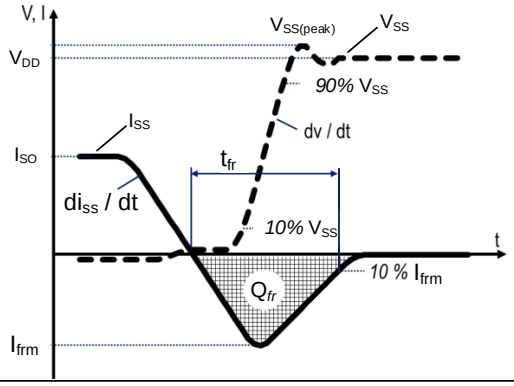
Test circuit for body diode characteristics	Body diode recovery waveform
	

Table 10 Switching times

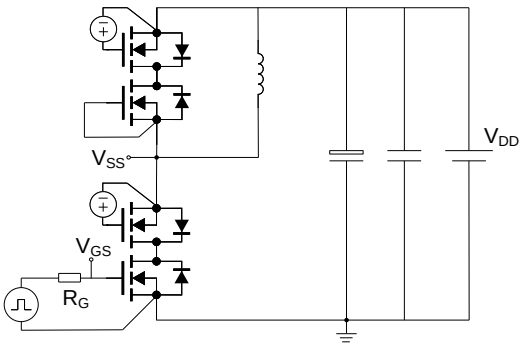
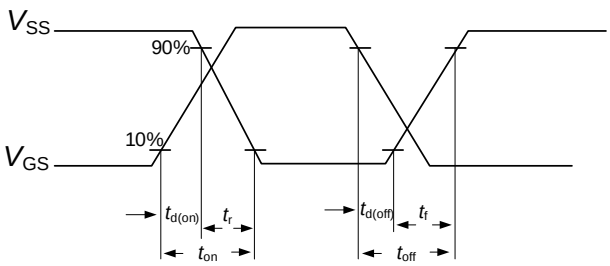
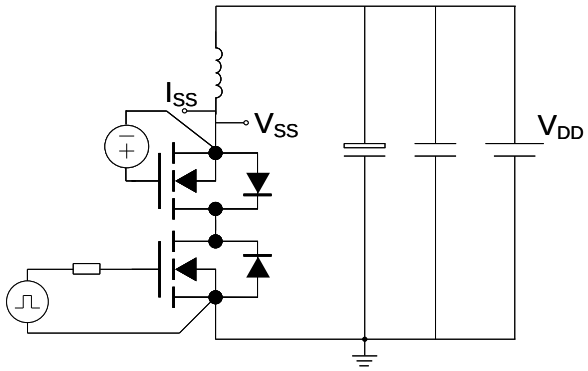
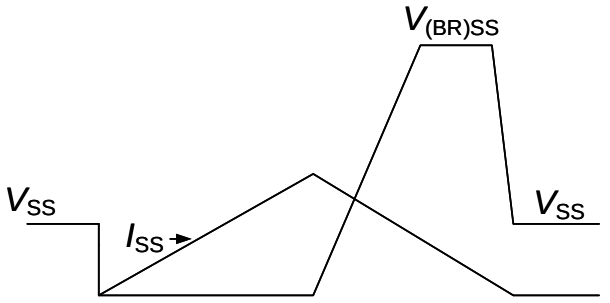
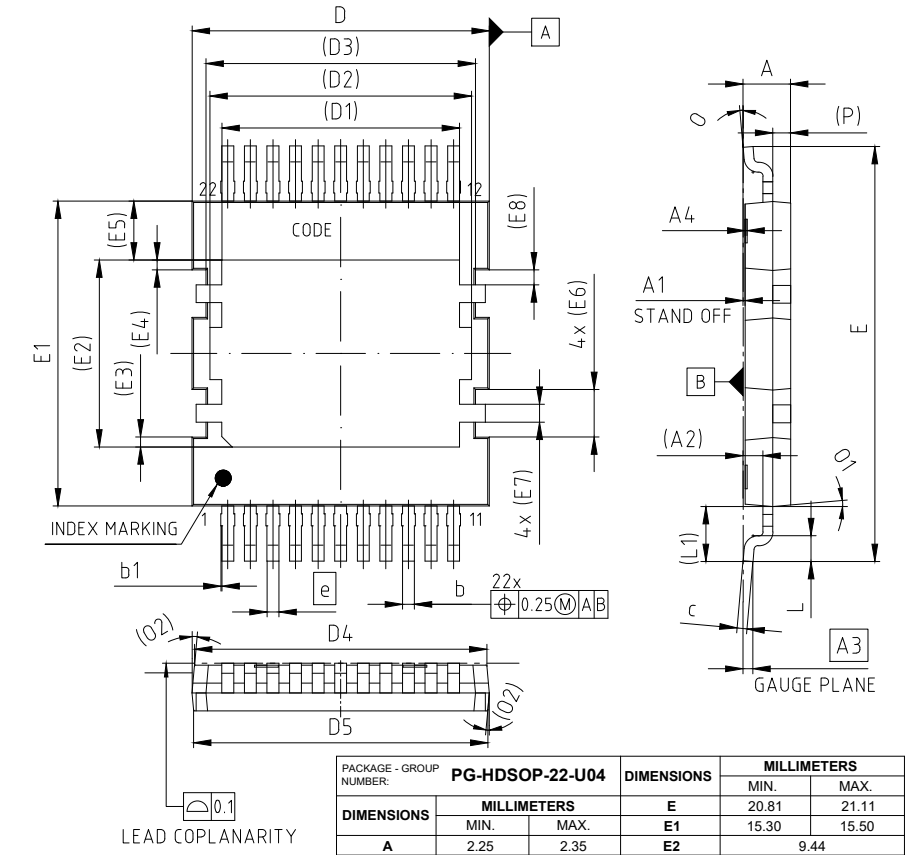
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package outlines



NOTES:

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER:	PG-HDSOP-22-U04		DIMENSIONS	MILLIMETERS	
				MIN.	MAX.
DIMENSIONS	MILLIMETERS		E	20.81	21.11
	MIN.	MAX.	E1	15.30	15.50
A	2.25	2.35	E2	9.44	
A1	0.00	0.15	E3	0.50	
A2	0.90		E4	0.50	
A3	0.50		E5	2.98	
A4	0.00	0.10	E6	2.40	
b	0.50	0.70	E7	0.90	
b1	---	0.15	E8	0.75	
c	0.46	0.58	e	1.14	
D	14.90	15.10	L	1.20	1.40
D1	12.00		L1	2.78	
D2	13.20		O	0°	8°
D3	13.60		O1	4°	6°
D4	14.76		O2	5°	
D5	14.84		P	0.90	

Figure 1 Outline PG-HDSOP-22, dimensions in mm

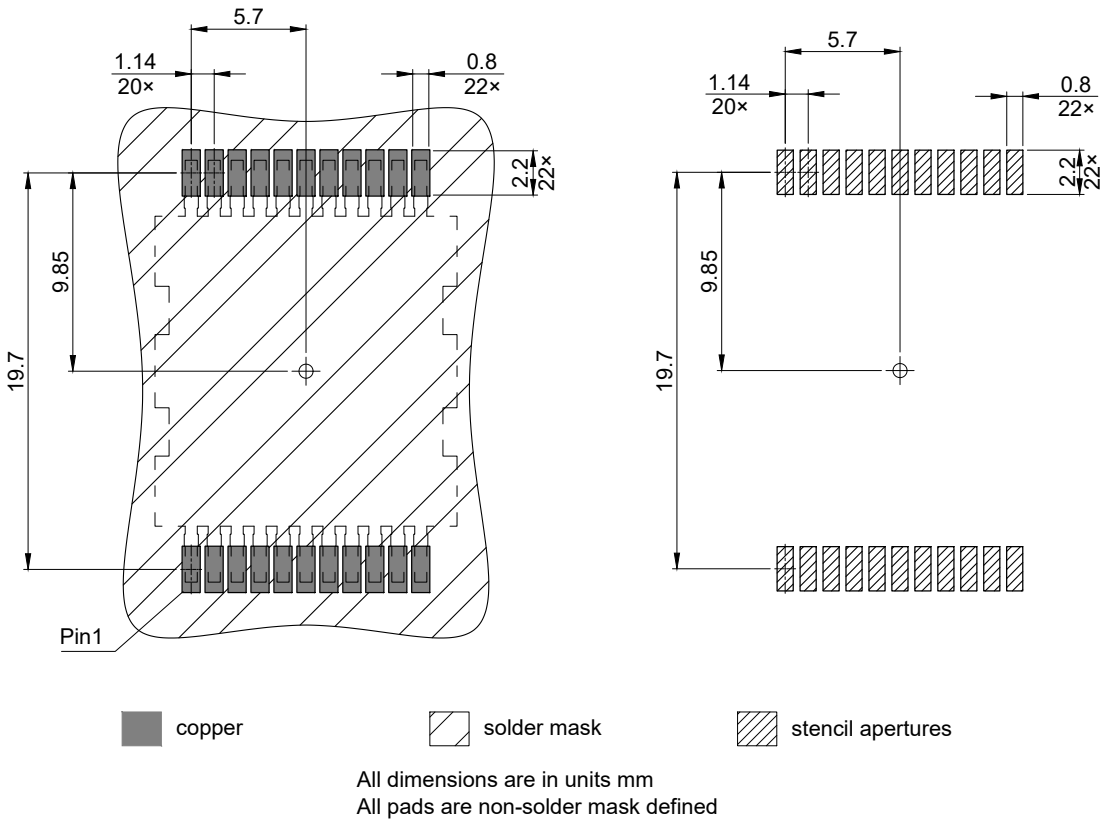


Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm

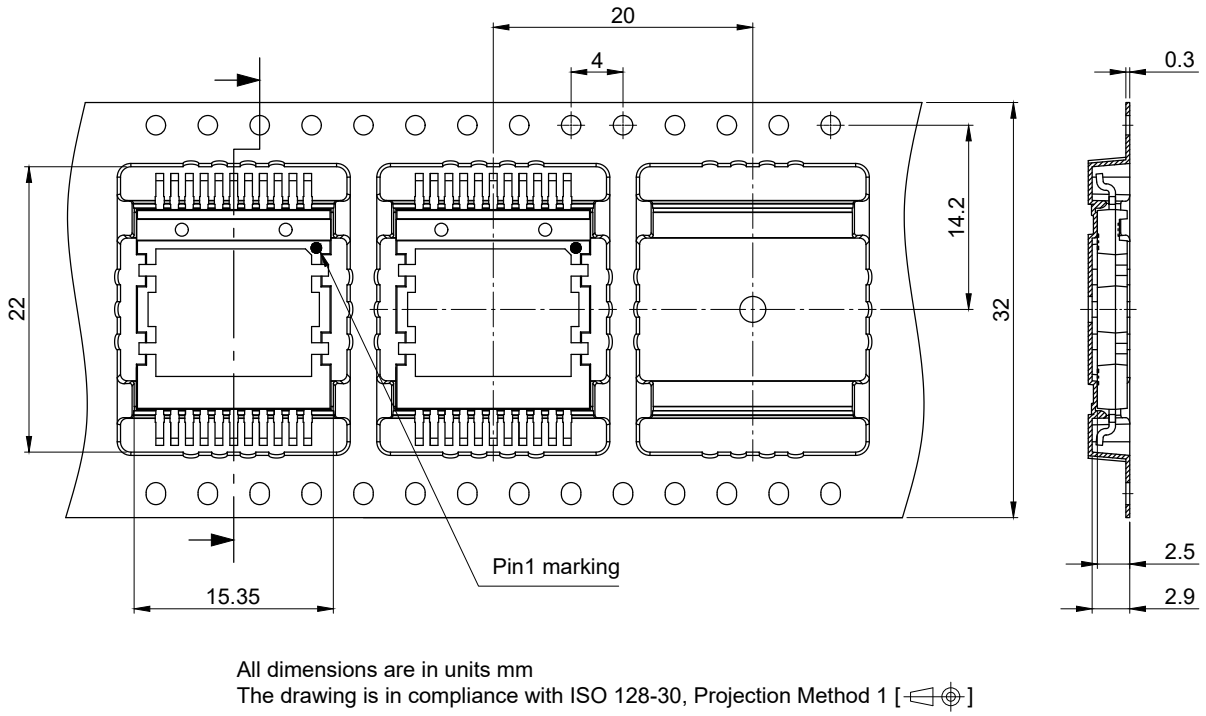


Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

8 Appendix A

Table 12 Related links

- IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Webpage
- IFX CoolSiC CoolSiC™ MOSFET 750 V G2 application note
- IFX CoolSiC CoolSiC™ MOSFET 750 V G2 simulation model
- IFX Design tools

Revision history

IMDQ75B066M2H

Revision 2026-09-07, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-09-07	Release of final version

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