

CoolSiC™ BDS 750 V G2

750 V CoolSiC™ Bidirectional switch (BDS)

Built on rugged CoolSiC™ G2 technology, it integrates two SiC power switches in a dual-die common-drain architecture within a top-side-cooled Q-DPAK package, simplifying system design and enabling next-generation topologies. Designed for modern power grids and energy systems, it delivers high reliability, efficiency, and low lifetime TCO.

Features

- Two dies in back to back configuration
- Overload operation up to $T_j = 200^\circ\text{C}$ for 100 h
- Ready for native liquid cooling
- Short circuit ruggedness (typ. 2 μs)
- 100% avalanche tested

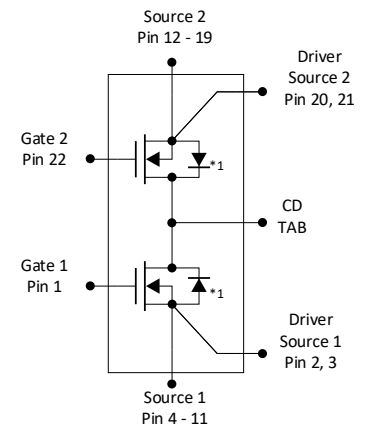
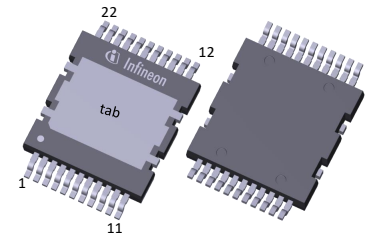
Benefits

- Lowest system TCO through full-load compliance and simpler design
- Maximum hard-switching efficiency for lower energy losses
- Enhanced thermal performance for longer lifetime
- Robust 750 V CoolSiC™ technology
- Up to 66% lower parasitic inductance for reliable switching

Potential applications

- HVDC AI PSU, BBU, CBU
- Residential Solar and ESS
- eVTOL CSI Drive
- Bidirectional EV charging
- HVAC Indirect Matrix Converter
- Solid-State Circuit Breaker

PG-HDSOP-22



*1: Internal body diode

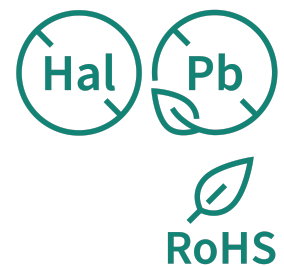
Product validation

Qualified according to relevant JEDEC tests.

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction. When paralleling MOSFETs the placement of the gate resistor is generally recommended to be in series to the Driver Source instead of the Gate.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{SS} over full $T_{j,range}$	± 750	V
$R_{SS(on),typ}$	40.0	m Ω
$R_{SS(on),max}$	50.0	m Ω
$Q_{G,typ}$	60	nC
$I_{SS,pulse}$	270	A
$Q_{oss,typ}$ @ 500 V	140	nC
$E_{oss,typ}$ @ 500 V	24.5	μJ



Part number	Package	Marking	Related links
IMDQ75B040M2H	PG-HDSOP-22	75R040B2	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified. $V_{GS1} = V_{GS2} = V_{GS}$ unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

For applications with applied blocking voltage > 525 V, it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support.

“Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source voltage	V_{SS}	-750	-	750	V	static, $V_{GS} = 0\text{ V}$, $T_j = -55^\circ\text{C}$ to 175°C
Continuous DC source-to-source current ¹⁾	$I_{SS,DC}$	-61	-	61	A	$V_{GS} = 18\text{ V}$, $T_c = 25^\circ\text{C}$
		-43		43		$V_{GS} = 18\text{ V}$, $T_c = 100^\circ\text{C}$
Continuous DC source-to-source current, diode mode ¹⁾	$I_{SS,DC}$	-56	-	56	A	$V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$, $T_c = 25^\circ\text{C}$
Peak source-to-source current ²⁾	I_{SSM}	-270	-	270	A	$V_{GS} = 18\text{ V}$, $T_c = 25^\circ\text{C}$
Peak source-to-source current, diode mode ²⁾	I_{SSM}	-270	-	270	A	$V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$, $t_p \leq 250\text{ ns}$
		-56		56		$V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$
Avalanche energy, single pulse	E_{AS}	-	-	280	mJ	$I_{SS} = 10.5\text{ A}$, $V_{DD} = 50\text{ V}$; see table 11
Avalanche energy, repetitive	E_{AR}			1.4		
Avalanche current, single pulse	I_{AS}	-	-	10.5	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	200	V/ns	$V_{SS} = 0 \dots 500\text{ V}$
Gate source voltage (static) ³⁾	V_{GS}	-7	-	23	V	-
Gate source voltage (transient)	V_{GS}	-11	-	25	V	$t_p \leq 500\text{ ns}$, duty cycle $\leq 1\%$
Power dissipation	P_{tot}	-	-	340	W	$T_c = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j			175		
Extended operating junction temperature ⁴⁾	T_j	-	-	200	$^\circ\text{C}$	$\leq 100\text{ h}$ in the application lifetime
Mounting torque	-	-	-	n.a.	Ncm	-
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_c = 25^\circ\text{C}$, $t = 1\text{ min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_{pulse} limited by $T_{j,max}$.

³⁾ The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

⁴⁾ Up to 7500 temperature cycles, where maximum delta T is limited to 100 K.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case 5)	$R_{th(j-c)}$	-	0.31	0.44	K/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

5) Thermal resistance for each die.

3 Operating range

$V_{GS1} = V_{GS2} = V_{GS}$ unless otherwise specified.

Table 4 **Operating range**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-		

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified. $V_{GS1} = V_{GS2} = V_{GS}$ unless otherwise specified.

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source breakdown voltage ⁶⁾	$V_{(BR)SS}$	-840	-	840	V	$V_{GS} = 0\text{ V}$, $I_{SS} = 0.98\text{ mA}$
Gate threshold voltage ⁷⁾	$V_{GS(th)}$	3.5	4.5	5.6	V	$V_{SS} = V_{GS}$, $I_{SS} = 9.8\text{ mA}$, $T_j = 25^\circ\text{C}$
		-	3.3	-		$V_{SS} = V_{GS}$, $I_{SS} = 9.8\text{ mA}$, $T_j = 175^\circ\text{C}$
Zero gate voltage source-to-source current	$I_{SS,leakage}$	-	1	75	μA	$V_{SS} = 750\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25^\circ\text{C}$
			10	-		$V_{SS} = 750\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 175^\circ\text{C}$
Gate-source leakage current ⁸⁾	$I_{GS,leakage}$	-	-	100	nA	$V_{GS} = 23\text{ V}$, $V_{SS} = 0\text{ V}$, $T_j = 25^\circ\text{C}$
				-100		$V_{GS} = -7\text{ V}$, $V_{SS} = 0\text{ V}$, $T_j = 25^\circ\text{C}$
Forward transconductance	g_{fs}	-	27.0	-	S	$I_{SS} = 44.7\text{ A}$, $V_{SS} = 20\text{ V}$
Source-to-source on-state resistance	$R_{SS(on)}$	-	52.0	-	m Ω	$V_{GS} = 15\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 25^\circ\text{C}$
			40.0	50.0		$V_{GS} = 18\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 25^\circ\text{C}$
			36.0	-		$V_{GS} = 20\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 25^\circ\text{C}$
Source-to-source on-state resistance ⁹⁾	$R_{SS(on)}$	-	63.6	80.0	m Ω	$V_{GS} = 18\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 150^\circ\text{C}$
Source-to-source on-state resistance	$R_{SS(on)}$	-	72.0	-	m Ω	$V_{GS} = 18\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 175^\circ\text{C}$
Short-circuit withstand time ⁹⁾	t_{SC}	-	2.0	-	μs	$V_{DD} = 500\text{ V}$, $V_{GS} = 18\text{ V}$, $R_{G,on} = 2.3\text{ }\Omega$, $R_{G,off} = 15\text{ }\Omega$, $V_{SS(peak)} < 750\text{ V}$
Internal gate resistance	$R_{G,int}$	-	2.0	-	Ω	$f = 1\text{ MHz}$

⁶⁾ Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

⁷⁾ Tested after pre-conditioning pulse at $V_{GS} = +20\text{ V}$. "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

⁸⁾ Tested individually for each die.

⁹⁾ Specified by design, not subject to production test.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2085	-	pF	$V_{GS} = 0\text{ V}$, $V_{SS} = 500\text{ V}$, $f = 250\text{ kHz}$
Reverse transfer capacitance	C_{rss}		11.2			
Output capacitance ¹⁰⁾	C_{oss}	-	158	205	pF	$V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$, $V_{SS} = 500\text{ V}$, $f = 250\text{ kHz}$
			150	195		$V_{GS} = 0\text{ V}$, $V_{SS} = 500\text{ V}$, $f = 250\text{ kHz}$
Output charge ¹⁰⁾	Q_{oss}	-	140	182	nC	calculation based on C_{oss} with $V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$
			122	159		calculation based on C_{oss} with $V_{GS} = 0\text{ V}$
Effective output capacitance, energy related ¹¹⁾	$C_{o(er)}$	-	196	-	pF	$V_{GS} = 0\text{ V}$, $V_{SS} = 0 \dots 500\text{ V}$
Effective output capacitance, time related ¹²⁾	$C_{o(tr)}$	-	281	-	pF	$I_{SS} = \text{constant}$, $V_{GS} = 0\text{ V}$, $V_{SS} = 0 \dots 500\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD} = 500\text{ V}$, $V_{GS} = 0/18\text{ V}$, $I_{SS} = 44.7\text{ A}$, $R_{G,ext} = 1.8\text{ }\Omega$, $L_{stray} = 15\text{ nH}$; see table 10
Rise time	t_r		10		ns	
Turn-off delay time	$t_{d(off)}$		22		ns	
Fall time	t_f		7		ns	
Turn-ON switching losses ¹³⁾	E_{on}		79		μJ	
Turn-OFF switching losses ¹³⁾	E_{off}		60		μJ	
Total switching losses ¹³⁾	E_{tot}		138		μJ	

¹⁰⁾ Maximum specification is defined by calculated six sigma upper confidence bound.

¹¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{SS} is rising from 0 to 500 V.

¹²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{SS} is rising from 0 to 500 V.

¹³⁾ MOSFET used in half-bridge configuration without external diode. Parameter verified according to IEC 60747-8.

Table 7 Gate charge characteristics

Gate charge characteristics measured individually for each die.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	15	-	nC	$V_{DD} = 500\text{ V}$, $I_{SS} = 44.7\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	Q_{GD}		13			
Total gate charge	Q_G		60			

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source voltage, diode mode	$V_{SS,diode}$	-	5.0	-	V	$V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 25^\circ\text{C}$
			5.3			$V_{GSx} = 0\text{ V}$, $V_{GSy} = 18\text{ V}$, $I_{SS} = 44.7\text{ A}$, $T_j = 175^\circ\text{C}$
MOSFET forward recovery time	t_{fr}	-	11.0	-	ns	$V_{DD} = 500\text{ V}$, $I_{SS} = 44.7\text{ A}$, $di_{SS}/dt = 4000\text{ A}/\mu\text{s}$; see table 9
MOSFET forward recovery charge ¹⁴⁾	Q_{fr}		162		nC	
MOSFET peak forward recovery current	I_{frm}		29		A	

¹⁴⁾ Q_{fr} includes Q_{oss}

5 Electrical characteristics diagrams

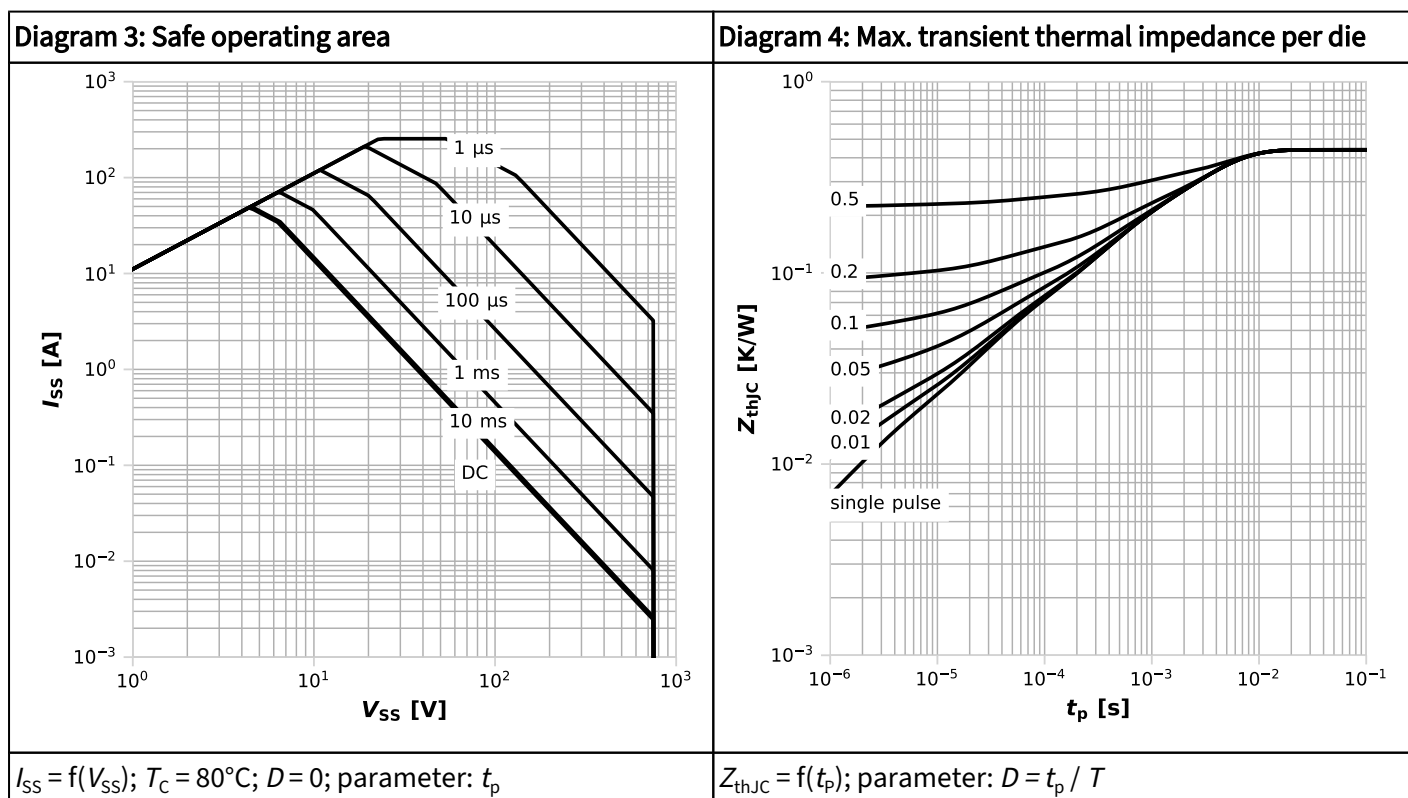
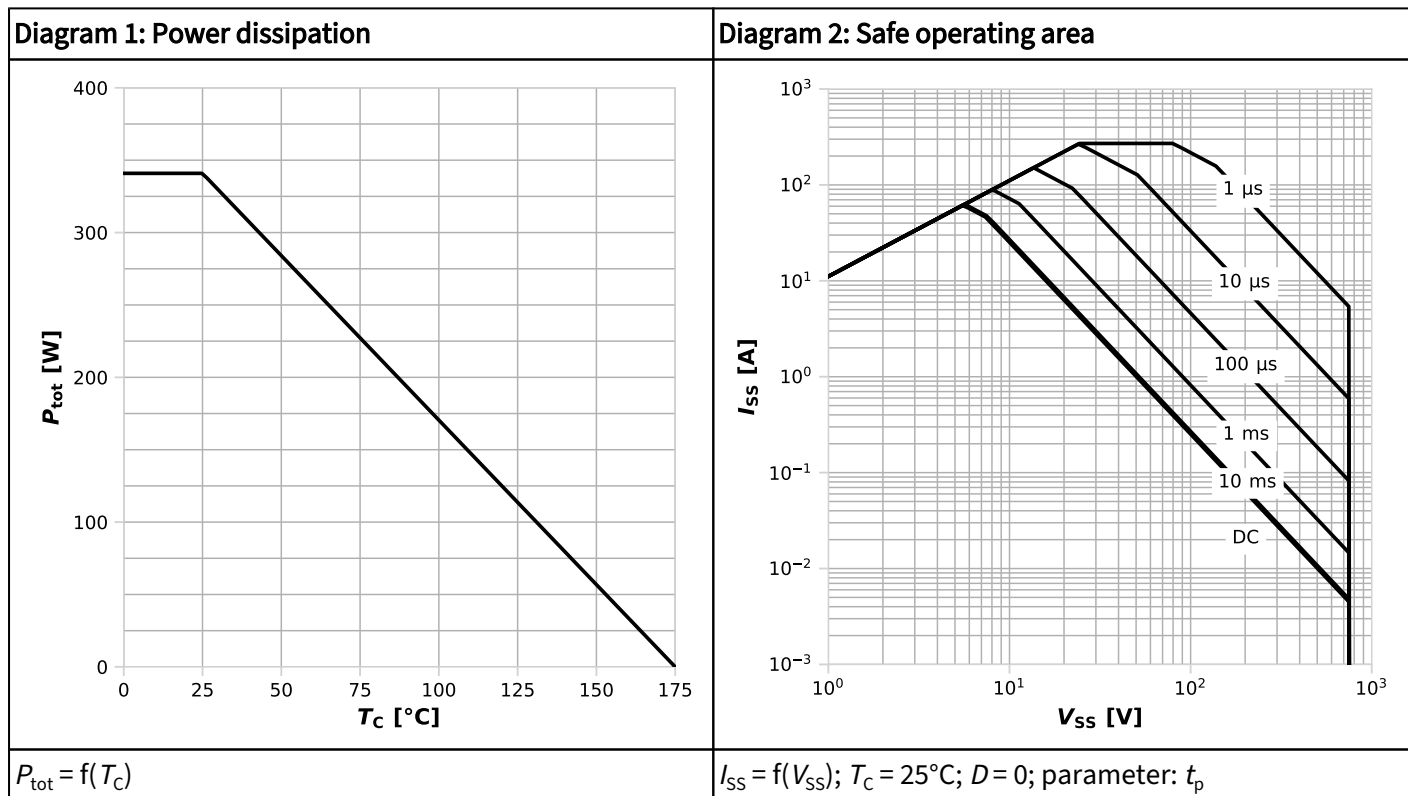
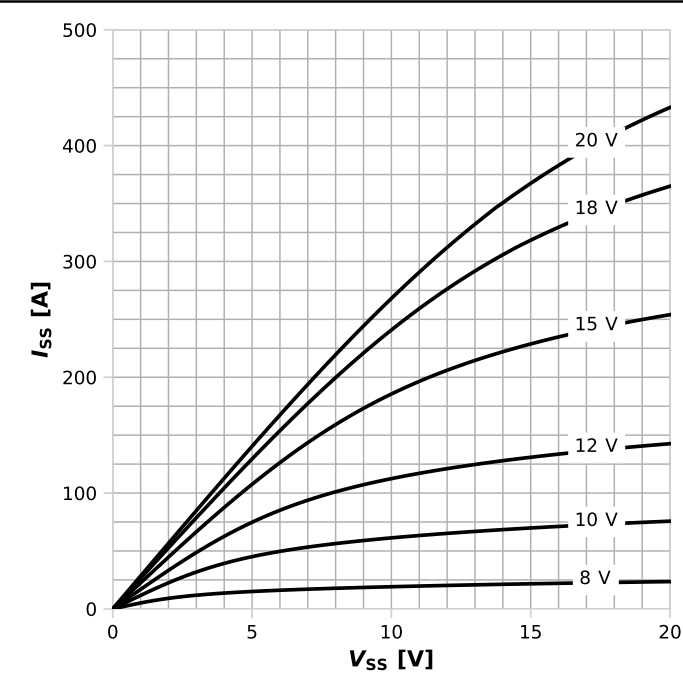
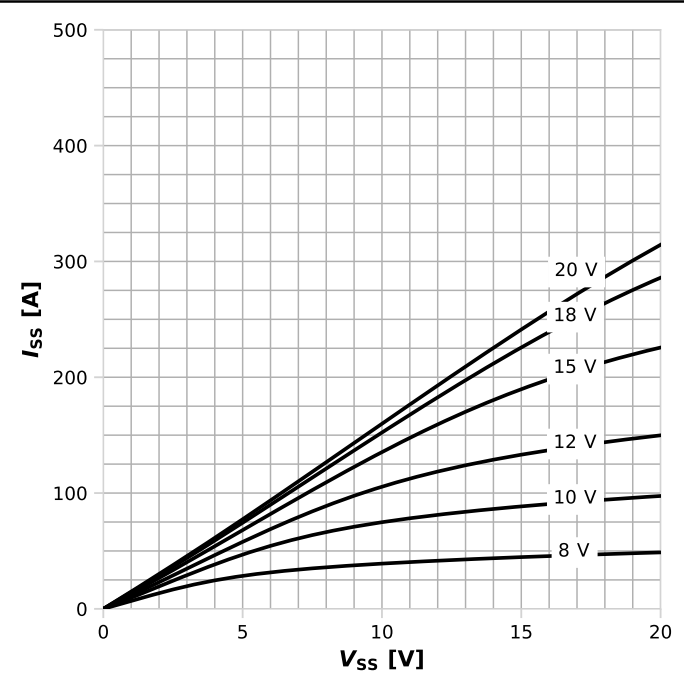


Diagram 5: Typ. output characteristics



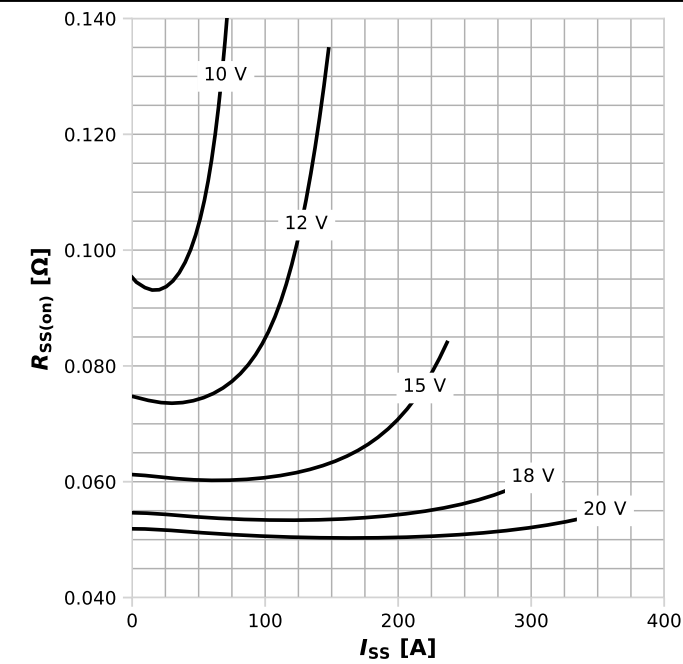
$I_{SS} = f(V_{SS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



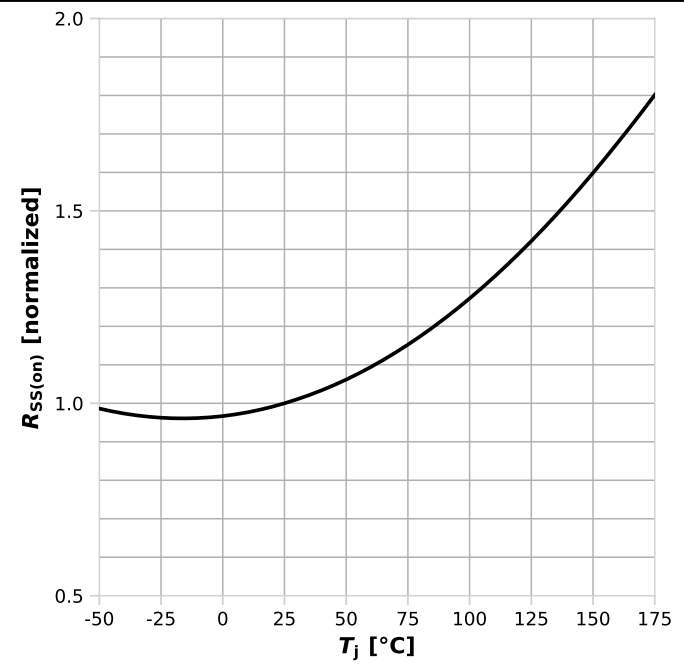
$I_{SS} = f(V_{SS})$; $T_j = 175^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



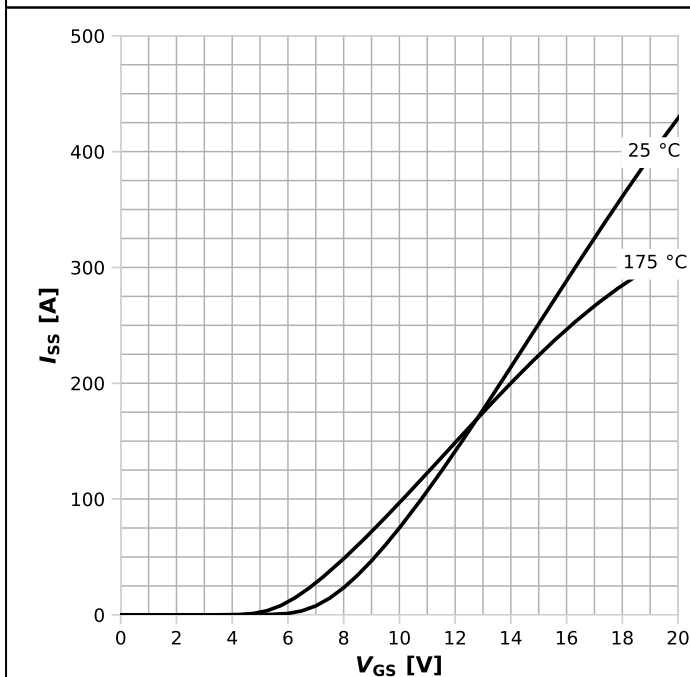
$R_{SS(on)} = f(I_{SS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



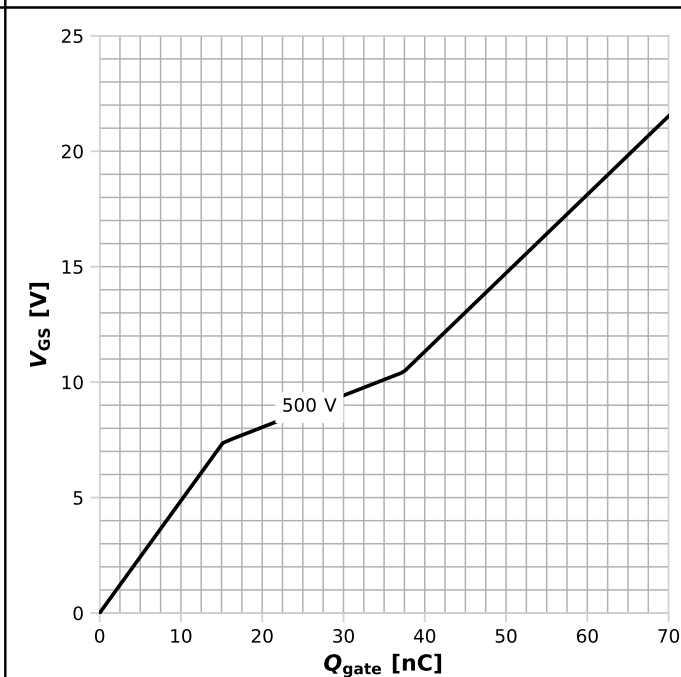
$R_{SS(on)} = f(T_j)$; $I_{SS} = 44.7\text{ A}$; $V_{GS} = 18\text{ V}$

Diagram 9: Typ. transfer characteristics



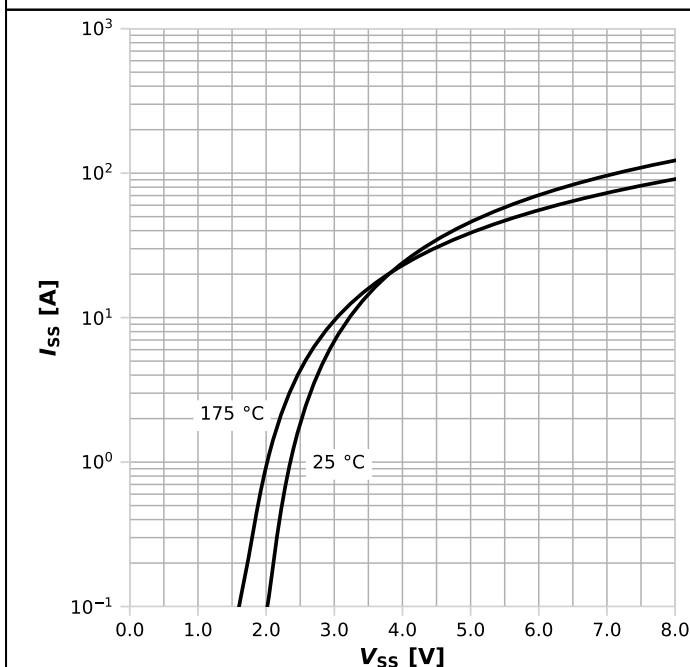
$I_{SS} = f(V_{GS})$; $V_{SS} = 20 \text{ V}$; parameter: T_j

Diagram 10: Typ. gate charge



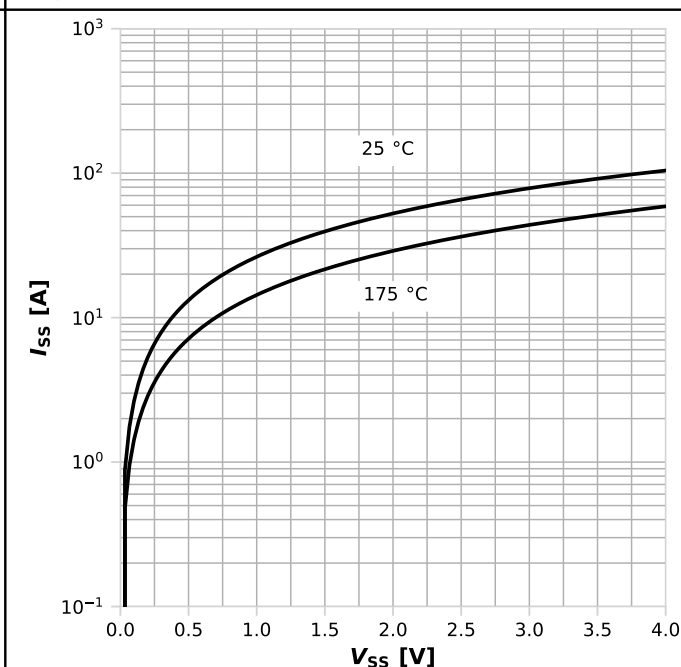
$V_{GS} = f(Q_{gate})$; $I_{SS} = 44.7 \text{ A pulsed}$; parameter: V_{DD}

Diagram 11: Typ. reverse current characteristics



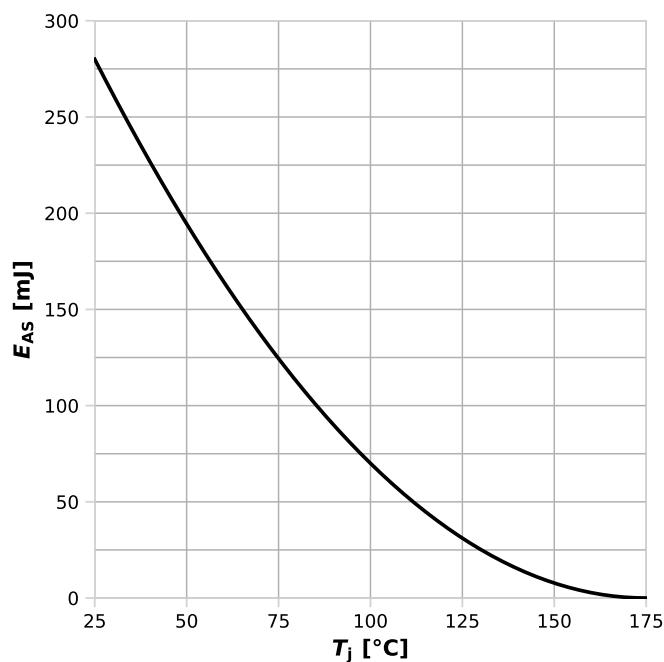
$I_{SS} = f(V_{SS})$; $V_{GSx} = 18 \text{ V}$; $V_{GSy} = 0 \text{ V}$; parameter: T_j

Diagram 12: Typ. reverse current characteristics



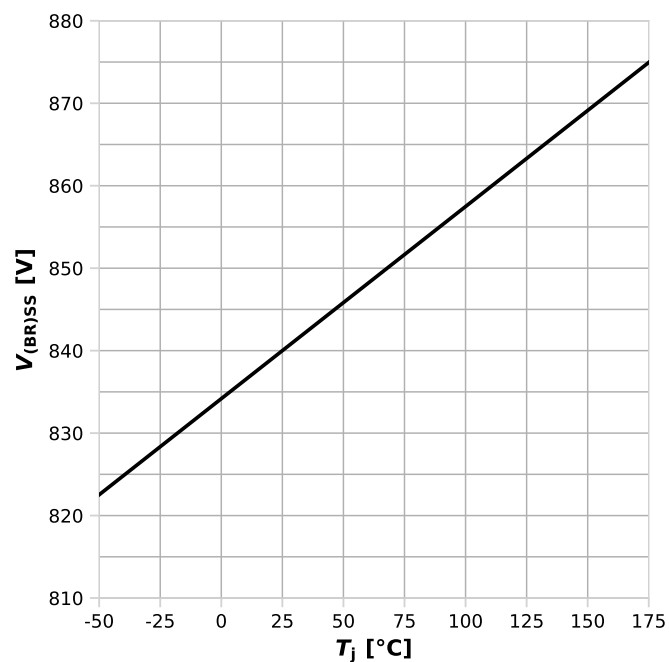
$I_{SS} = f(V_{SS})$; $V_{GSx} = 18 \text{ V}$; $V_{GSy} = 18 \text{ V}$; parameter: T_j

Diagram 13: Avalanche energy



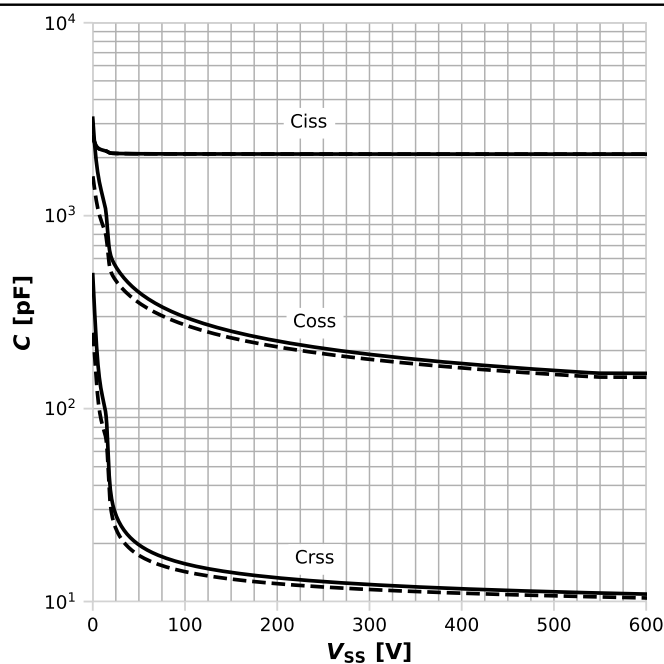
$E_{AS} = f(T_j); I_{SS} = 10.5 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 14: Drain-source breakdown voltage



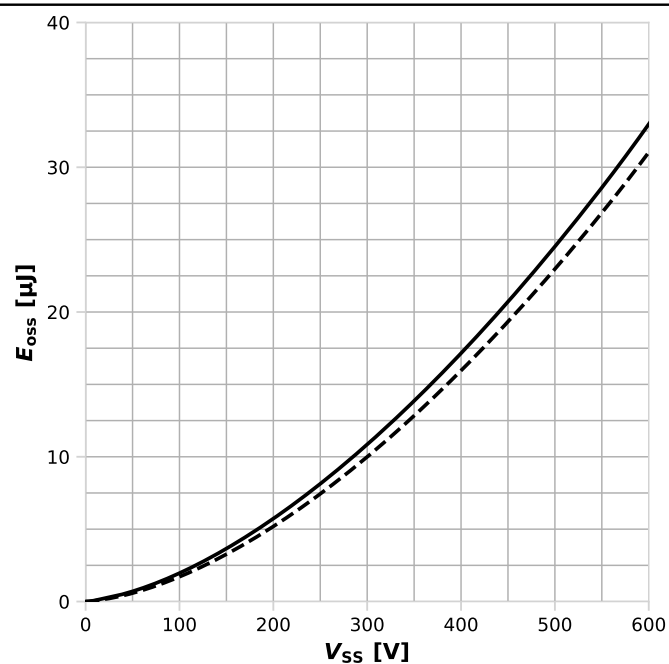
$V_{(BR)SS} = f(T_j); I_{SS} = 0.98 \text{ mA}$

Diagram 15: Typ. capacitances



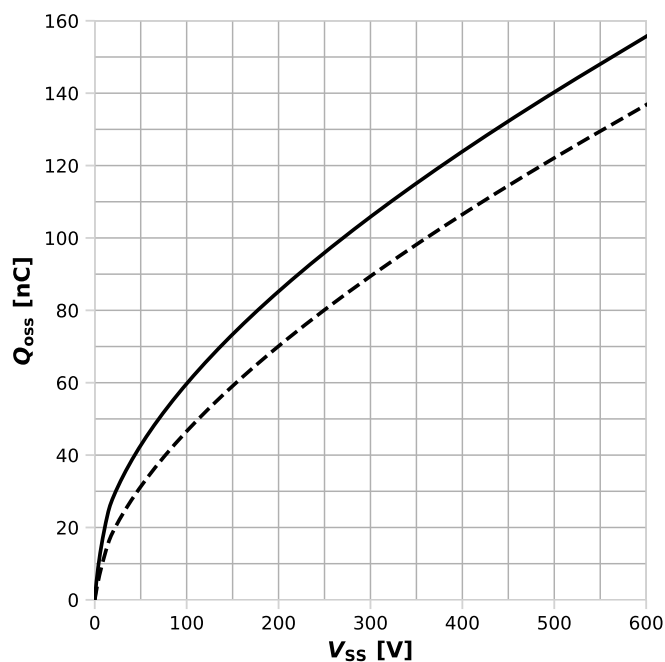
$C = f(V_{SS}); f = 250 \text{ kHz}$
solid: $V_{GSx} = 0 \text{ V}, V_{GSy} = 18 \text{ V}$; dashed: $V_{GSx} = 0 \text{ V}, V_{GSy} = 0 \text{ V}$

Diagram 16: Typ. Coss stored energy



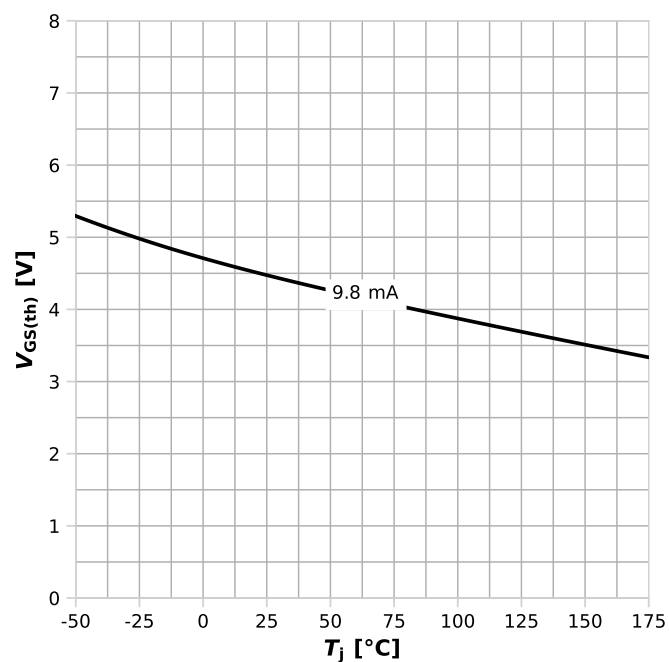
$E_{oss} = f(V_{SS})$
solid: $V_{GSx} = 0 \text{ V}, V_{GSy} = 18 \text{ V}$; dashed: $V_{GSx} = 0 \text{ V}, V_{GSy} = 0 \text{ V}$

Diagram 17: Typ. Qoss output charge



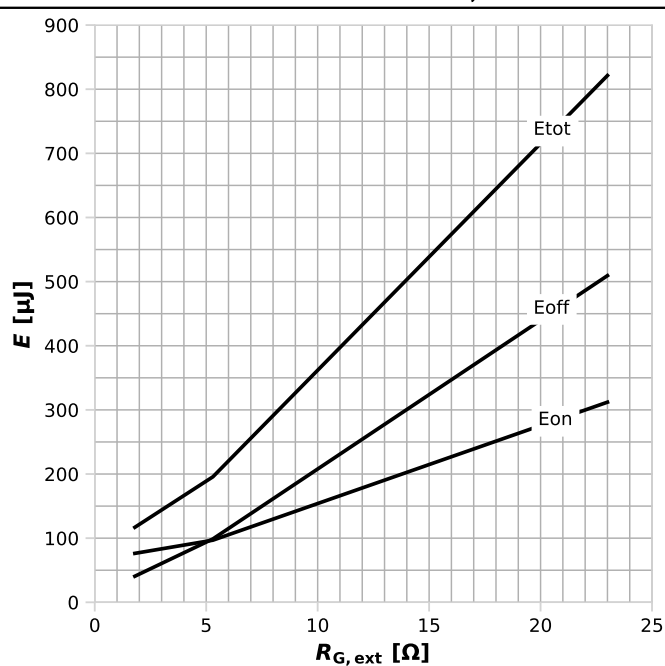
$Q_{oss} = f(V_{ss})$
 solid: $V_{GSx} = 0 \text{ V}$, $V_{GSy} = 18 \text{ V}$; dashed: $V_{GSx} = 0 \text{ V}$, $V_{GSy} = 0 \text{ V}$

Diagram 18: Typ. gate threshold voltage



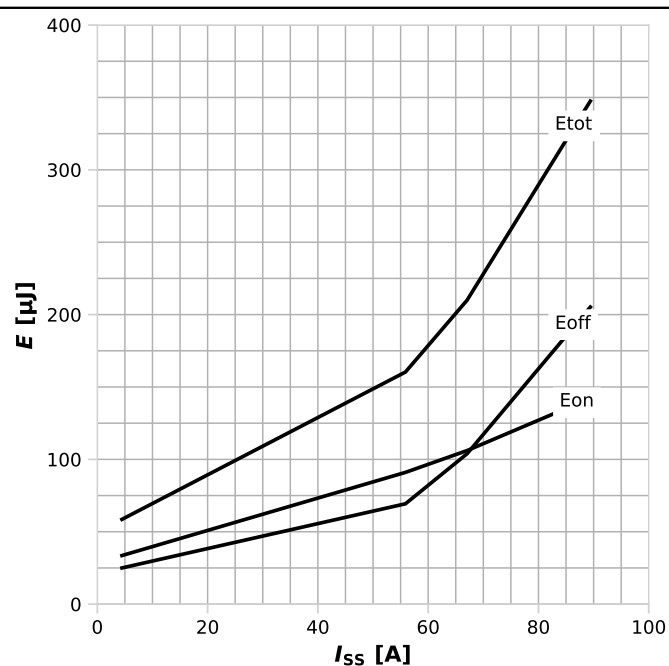
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{SS}$; parameter: I_{SS}

Diagram 19: Typ. Switching Losses vs $R_{G,ext}$

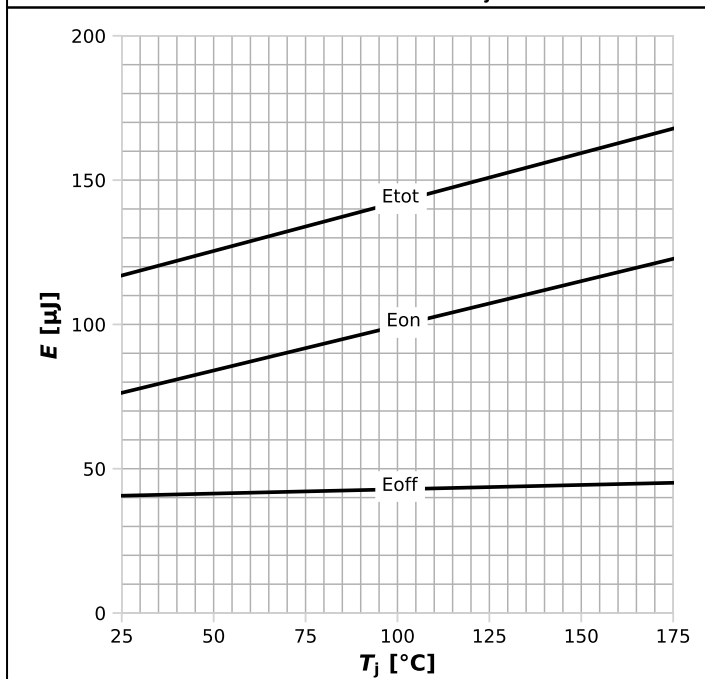


$V_{DD} = 500 \text{ V}$; $I_{SS} = 44.7 \text{ A}$; $T_j = 25^\circ\text{C}$

Diagram 20: Typ. Switching Losses vs switching current



$V_{DD} = 500 \text{ V}$; $R_{G,ext} = 1.8 \Omega$; $T_j = 25^\circ\text{C}$

Diagram 21: Typ. Switching Losses vs T_j 

$V_{DD} = 500 \text{ V}$; $R_{G,ext} = 1.8 \text{ } \Omega$; $I_{SS} = 44.7 \text{ A}$

6 Test circuits

Table 9 Body diode characteristics

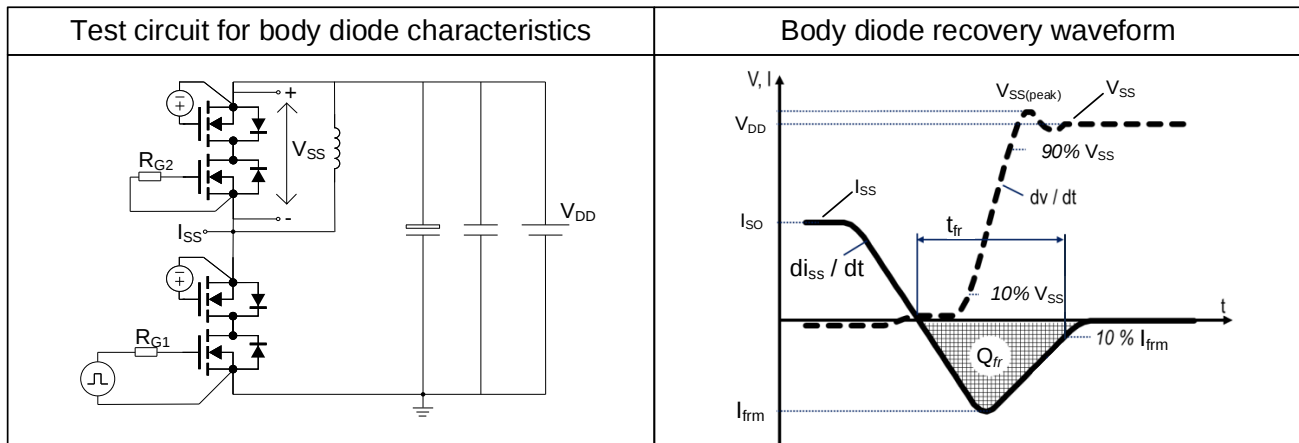


Table 10 Switching times

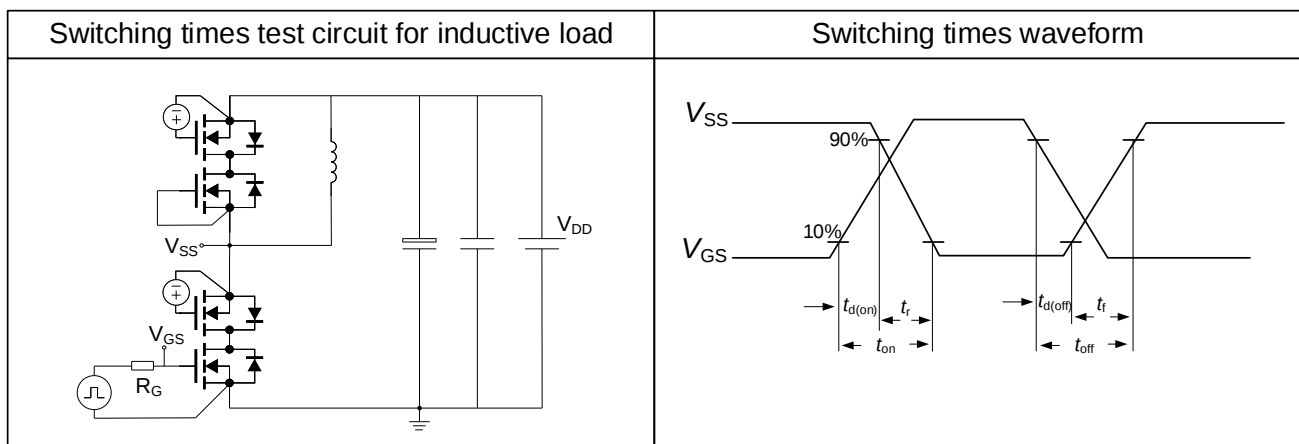
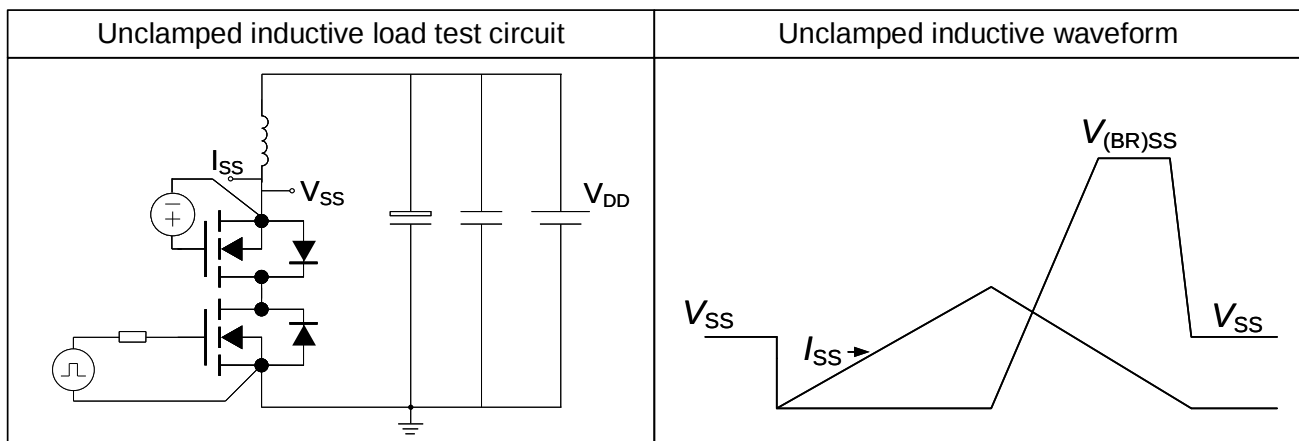


Table 11 Unclamped inductive load



7 Package outlines

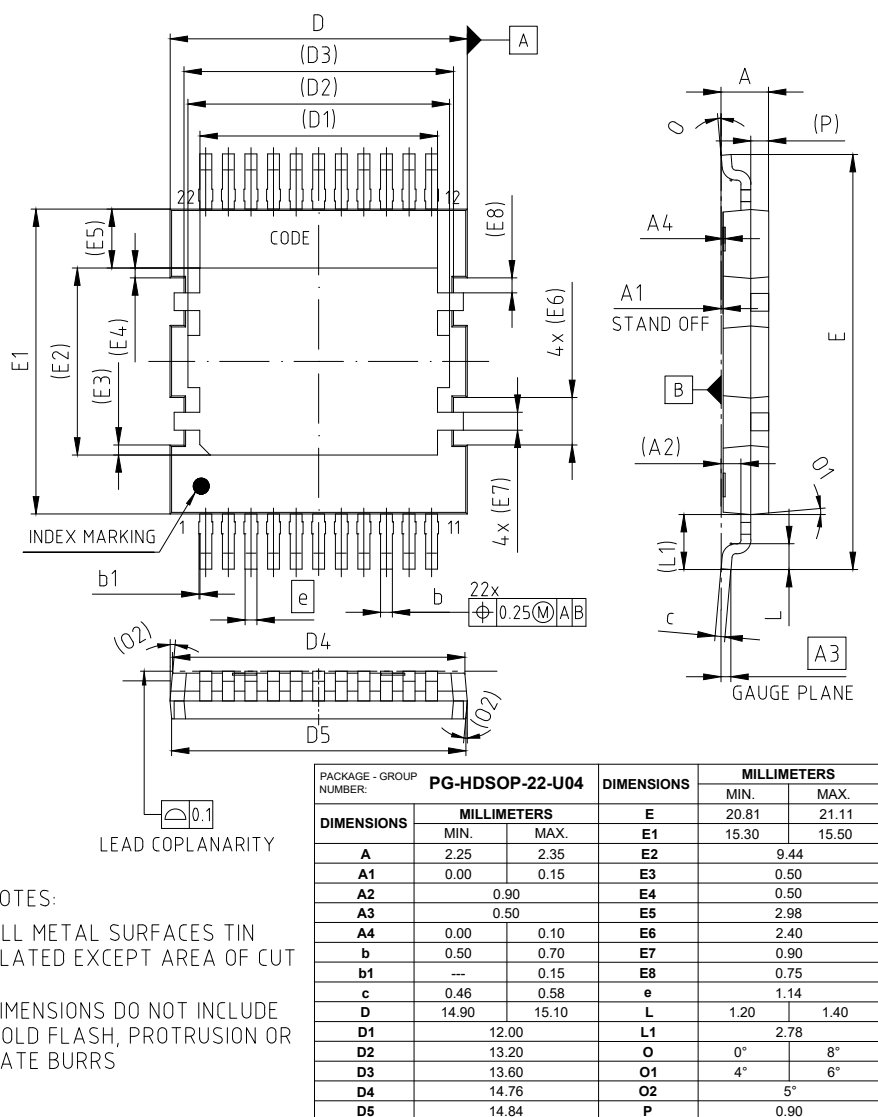


Figure 1 Outline PG-HDSOP-22, dimensions in mm

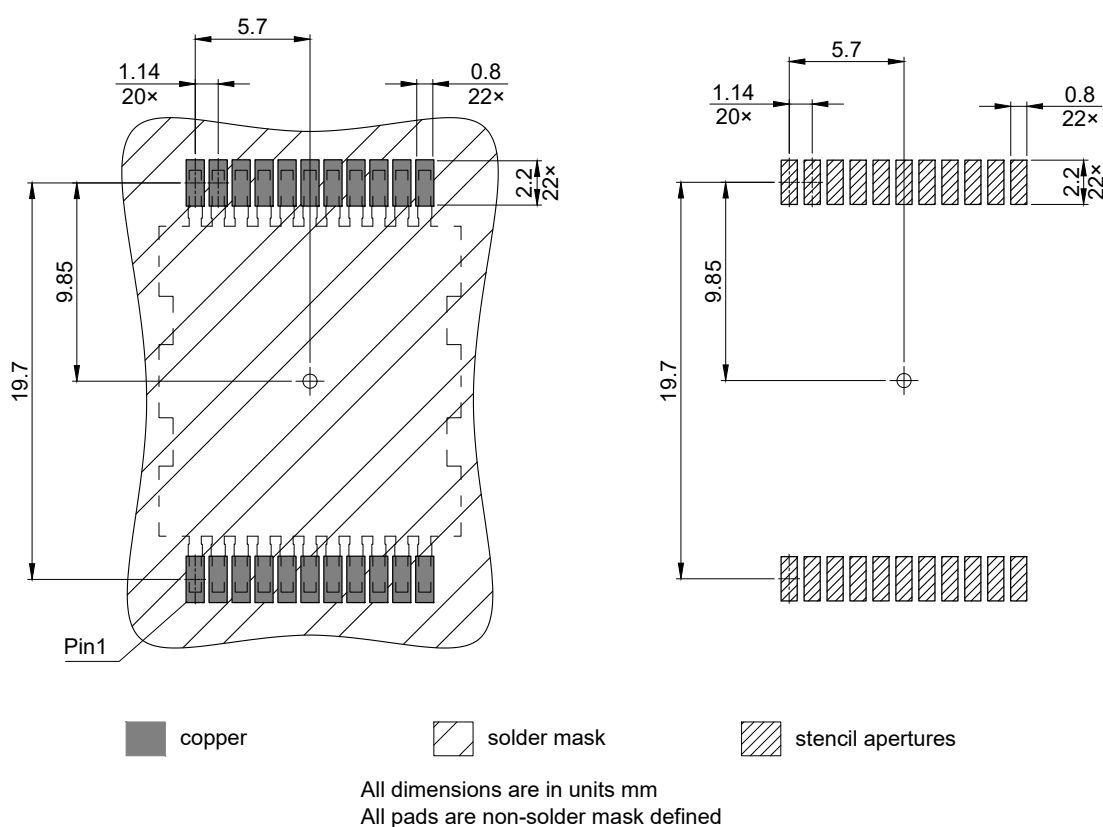
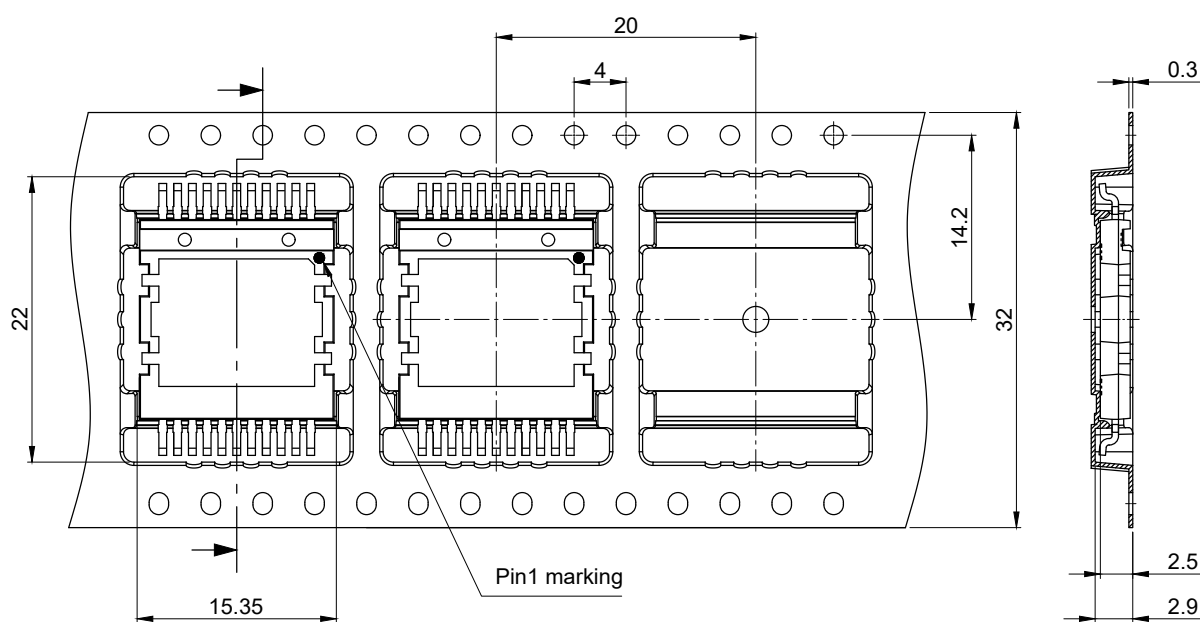


Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

8 Appendix A

Table 12 **Related links**

- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Webpage](#)
- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 application note](#)
- [IFX CoolSiC CoolSiC™ MOSFET 750 V G2 simulation model](#)
- [IFX Design tools](#)

Revision history

IMDQ75B040M2H

Revision 2026-09-07, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-09-07	Release of final version

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