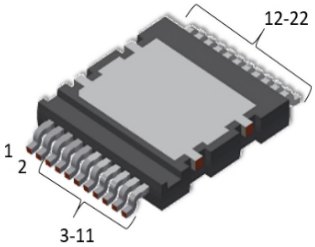
Final datasheet
CoolSiC™ 1200 V SiC MOSFET G2 : Q-DPAK top-side cooling



Halogen-free
Green
Lead-free
RoHS

Features

- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 138 A at T_c = 25°C
- $R_{DS(on)}$ = 10 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Overload operation up to T_{vj} = 200°C
- Short circuit withstand time 2 µs
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance
- Suitable Infineon gate drivers can be found under https://www.infineon.com/gdfinder

Potential applications

- Solid-state circuit breaker / Solid-state relay
- EV Charging
- Online UPS / Industrial UPS
- String inverter
- General purpose drives (GPD)
- CAV
- Servo drives

Product validation

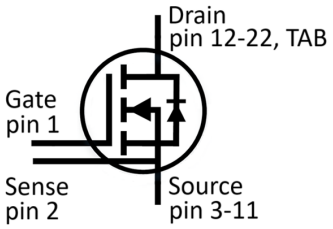
- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

Pin definition:

- Pin 1 – Gate
- Pin 2 – Kelvin sense contact
- Pin 3-11 – Source
- Pin 12-22, Tab – Drain

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction



Type	Package	Marking
IMCQ120R010M2H	PG-HDSOP-22-U03	12M2H010

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	Reflow soldering (MSL1 according to JEDEC J-STD-020)			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.13	0.17	K/W
Comparative Tracking Index	*CTI*	IEC 60112 (material group 1 according to IEC 60664-1)	600			V

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	195	A
			$T_c = 100$ °C	138	
Peak drain current, t_p limited by $T_{vj(max)}$ [1)]	I_{DM}	$V_{GS} = 18$ V		690	A
Gate-source voltage, max. transient voltage [2)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage	V_{GS}			-7...23	V
Avalanche energy, single pulse	E_{AS}	$I_D = 69$ A, $V_{DD} = 50$ V, $L = 0.4$ mH		868	mJ
Avalanche energy, repetitive	E_{AR}	$I_D = 69$ A, $V_{DD} = 50$ V, $L = 1.8$ µH		4.34	mJ
Short-circuit withstand time	t_{SC}	$V_{DD} \leq 800$ V, $V_{DS,peak} < 1200$ V, $V_{GS(on)} = 15$ V, $T_{vj(start)} = 25$ °C		2	µs
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	880	W
			$T_c = 100$ °C	440	

1) Verified by the design/characterization.
2) **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 69 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		10		mΩ
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		12.5		
			T_{vj} = 150 °C, $V_{GS(on)}$ = 18 V		20.4	26	
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		23.7		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 21.7 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.1	V
			T_{vj} = 175 °C		3.2		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			35	µA
			T_{vj} = 175 °C		10.2		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = -10 V			-120	nA
			V_{GS} = 23 V			120	
Forward transconductance	g_{fs}	I_D = 69 A, V_{DS} = 20 V			23.2		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			2		Ω
Input capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			6.32		nF
Output capacitance	C_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			214		pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			19		pF
C_{oss} stored energy	E_{oss}	Calculated based on C_{oss} = f(V_{DD})			90		µJ
Output charge	Q_{oss}	Calculated based on C_{oss} = f(V_{DD})			335		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on E_{oss}			281		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on Q_{oss}			419		pF
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 69 A, V_{GS} = -2/18 V, turn-on pulse			150		nC

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 69 A, V_{GS} = -2/18 V, turn-on pulse			36		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = -2/18 V, turn-on pulse			35		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		13.6		ns
			T_{vj} = 175 °C		10.4		
Rise time	t_r	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		9		ns
			T_{vj} = 175 °C		8		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		27.5		ns
			T_{vj} = 175 °C		32.1		
Fall time	t_f	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		12		ns
			T_{vj} = 175 °C		14.1		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		648		µJ
			T_{vj} = 175 °C		1153		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		451		µJ
			T_{vj} = 175 °C		550		
Total switching energy[1)]	E_{tot}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		1412		µJ
			T_{vj} = 175 °C		2758		

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Turn-on energy at -5 V	E_{on}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		648		µJ
			T_{vj} = 175 °C		1174		
Turn-off energy at -5 V	E_{off}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		250		µJ
			T_{vj} = 175 °C		274		
Total switching energy at -5 V[1)]	E_{tot}	V_{DD} = 800 V, I_D = 69 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		1211		µJ
			T_{vj} = 175 °C		2532		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[2)]				200	°C

1) Including E_{fr}
2) Up to 5000 cycles. Maximum ΔT limited to 100 K.

***Note**: The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.*
Characteristics at T_{vj} = 25°C, unless otherwise specified.

3 Body diode (MOSFET)

Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} ≥ 25 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	155	A
			T_c = 100 °C	88	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	V_{GS} = 0 V		414	A

Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 69 A, V_{GS} = 0 V	T_{vj} = 25 °C		4.2	5.5	V
			T_{vj} = 100 °C		4.1		
			T_{vj} = 175 °C		4		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 69 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		0.6		µC
			T_{vj} = 175 °C		1.6		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 69 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		80		A
			T_{vj} = 175 °C		130		
MOSFET forward recovery energy	E_{fr}	V_{DD} = 800 V, I_{SD} = 69 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		313		µJ
			T_{vj} = 175 °C		1055		
MOSFET forward recovery energy at -5 V	E_{fr}	V_{DD} = 800 V, I_{SD} = 69 A, V_{GS} = -5 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		313		µJ
			T_{vj} = 175 °C		1084		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[1)]				200	°C

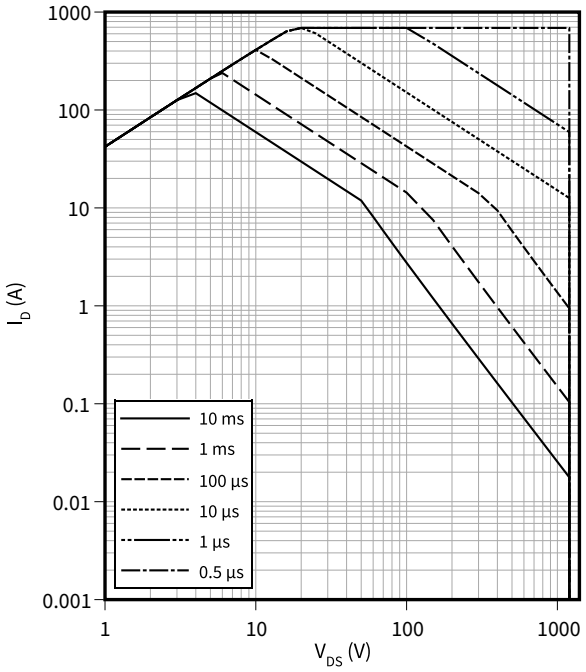
1) Up to 5000 cycles. Maximum ΔT limited to 100 K.

4 Characteristics diagrams

Safe operating area (SOA)

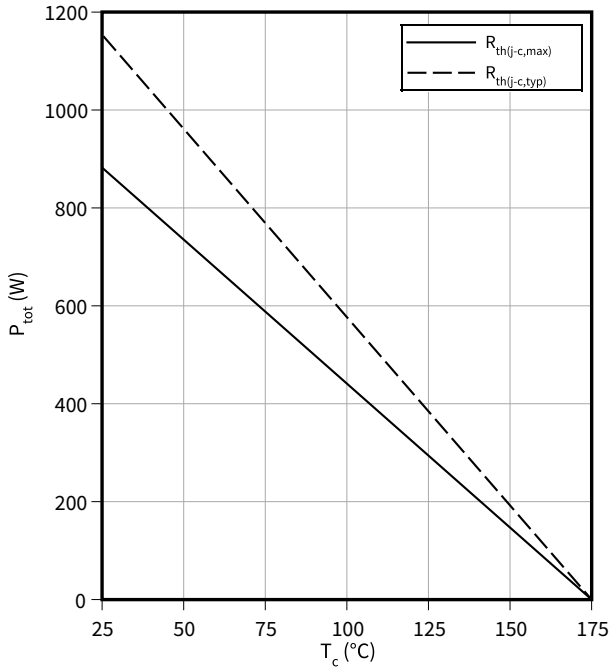
$I_D = f(V_{DS})$

$T_{vj} \leq 175\ °C$, $T_c = 25\ °C$



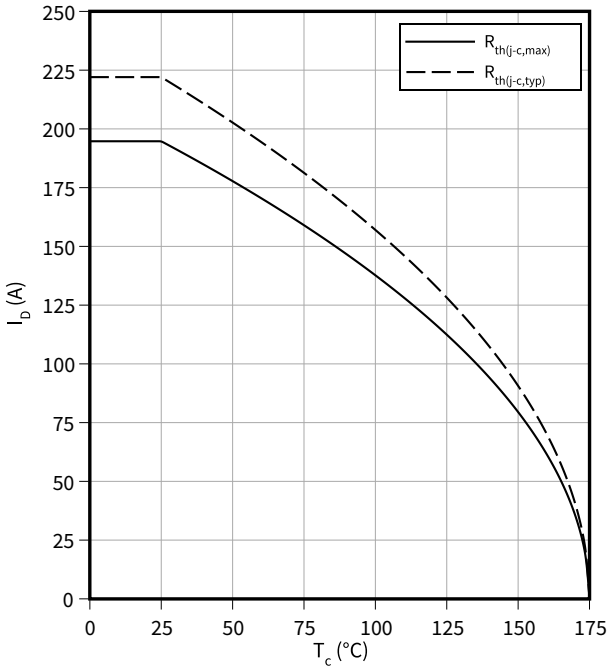
Power dissipation as a function of case temperature

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

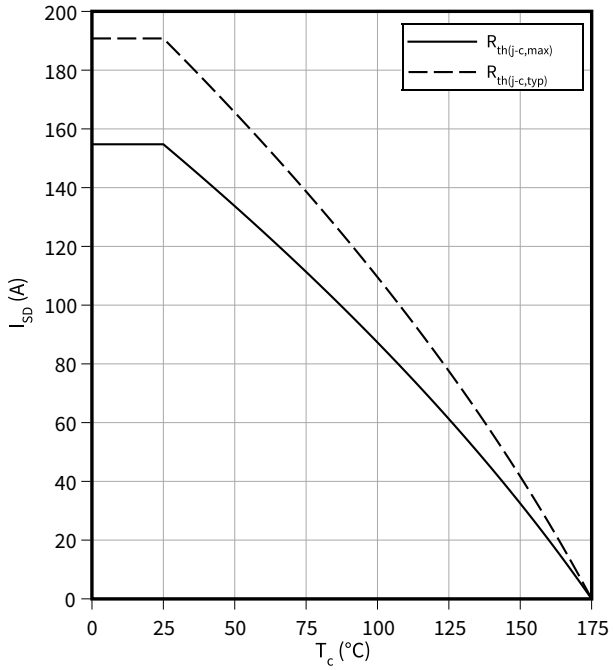
$I_D = f(T_c)$



Maximum source to drain current as a function of case temperature limited by bond wire

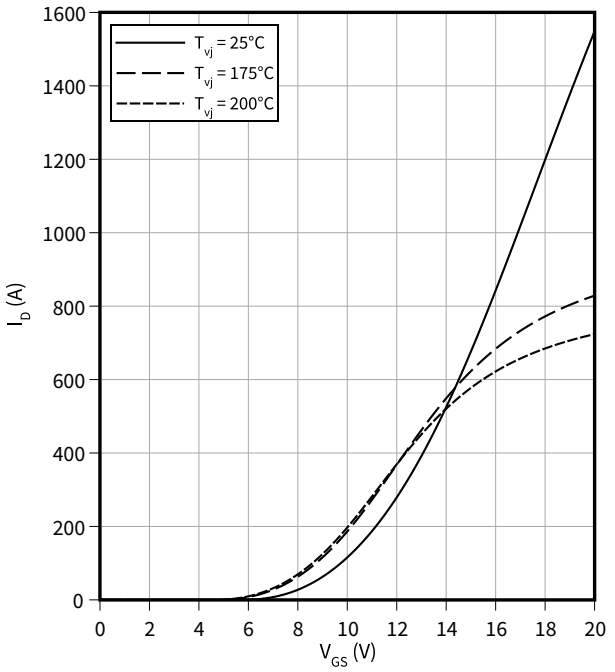
$I_{SD} = f(T_c)$

$V_{GS} = 0\ V$



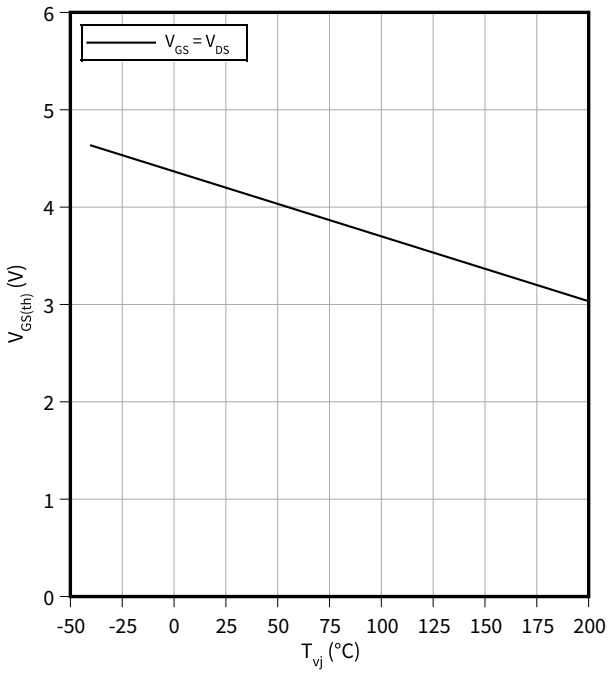
Typical transfer characteristic

$I_D = f(V_{GS})$
$V_{DS} = 20$ V, $t_p = 20$ µs



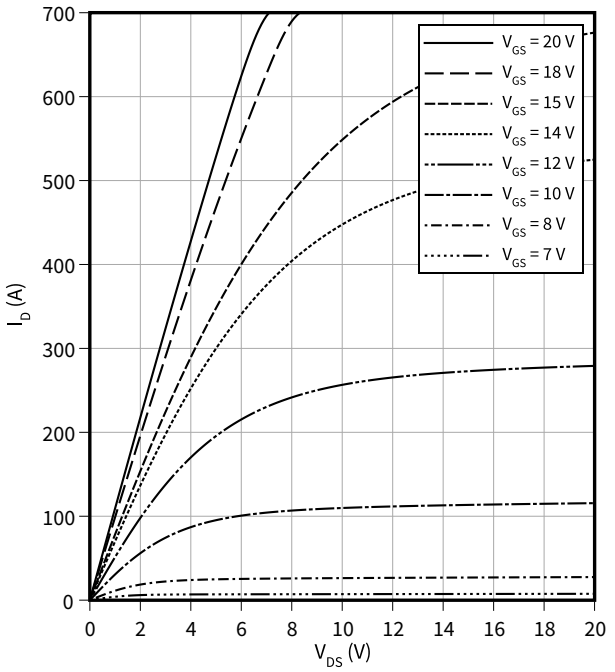
Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$
$I_D = 21.7$ mA



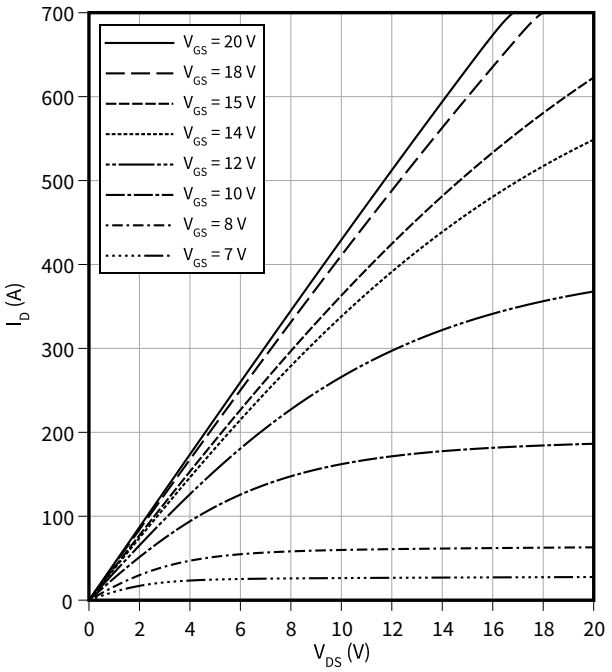
Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$
$T_{vj} = 25$ °C, $t_p = 20$ µs



Typical output characteristic, V_{GS} as a parameter

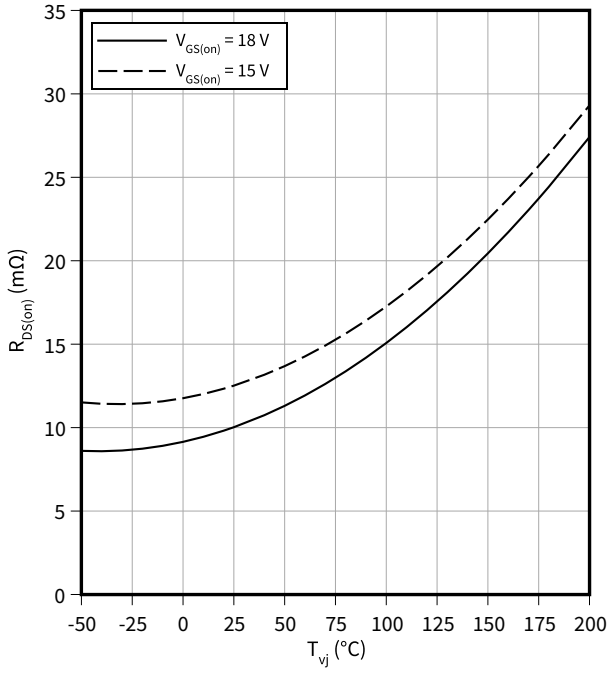
$I_D = f(V_{DS})$
$T_{vj} = 175$ °C, $t_p = 20$ µs



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$

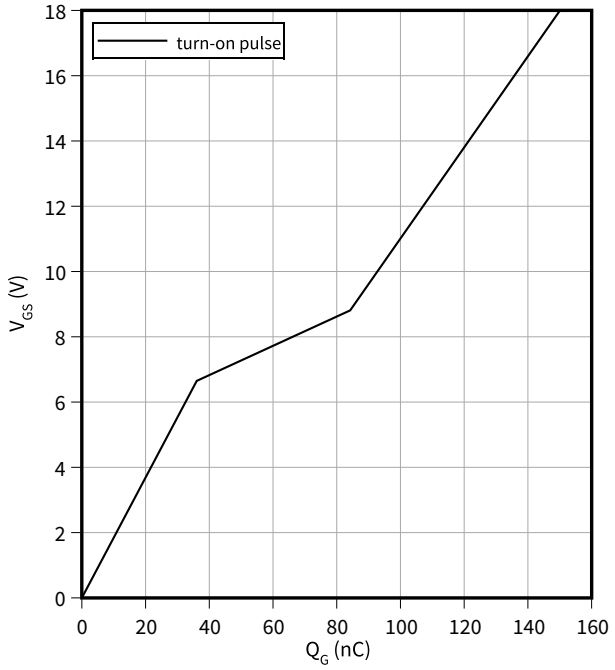
$I_D = 69$ A



Typical gate charge

$V_{GS} = f(Q_G)$

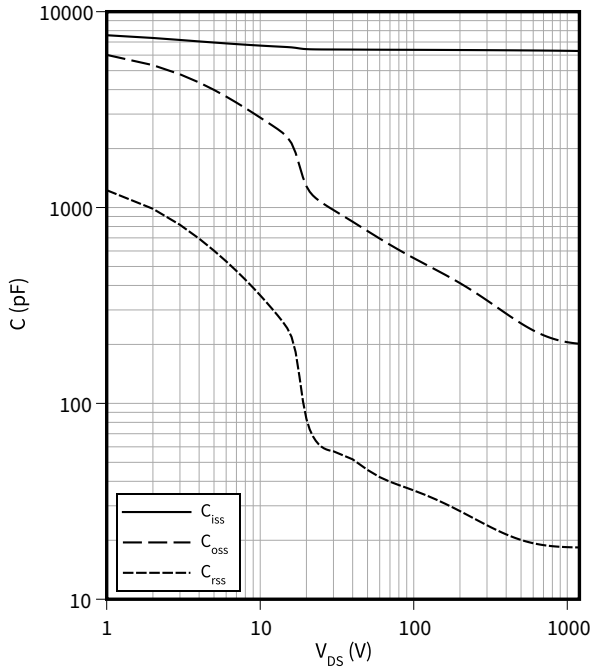
$I_D = 69$ A, $V_{DS} = 800$ V



Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$

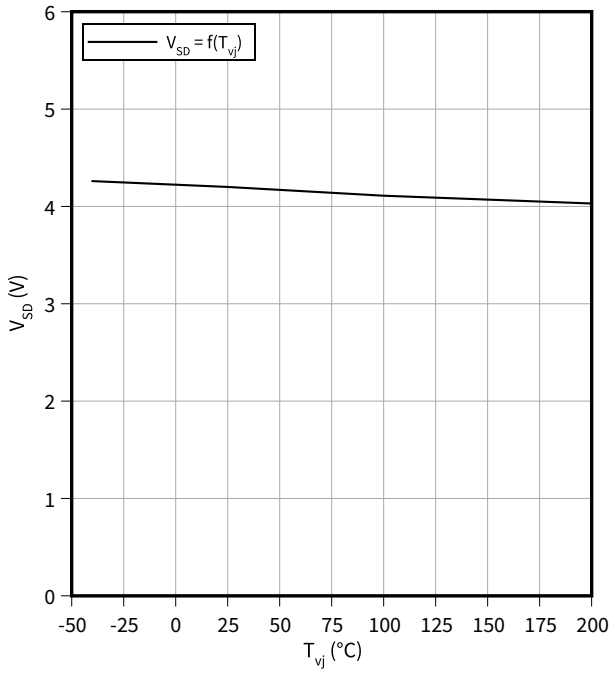
$f = 100$ kHz, $V_{GS} = 0$ V



Typical reverse drain voltage as a function of junction temperature

$V_{SD} = f(T_{vj})$

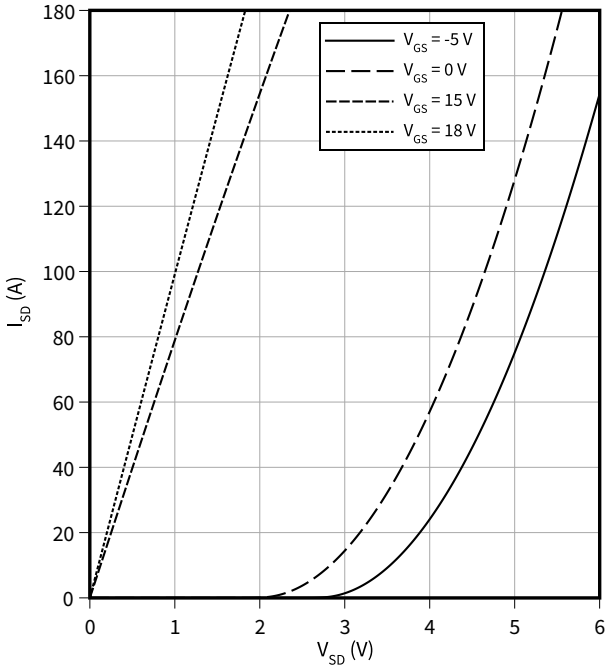
$I_{SD} = 69$ A, $V_{GS} = 0$ V



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

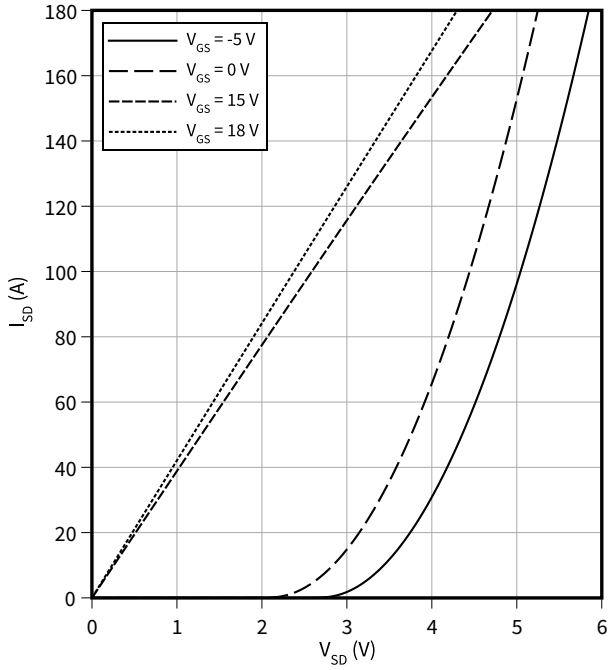
$T_{vj} = 25\ °C$, $t_p = 20\ \mu s$



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

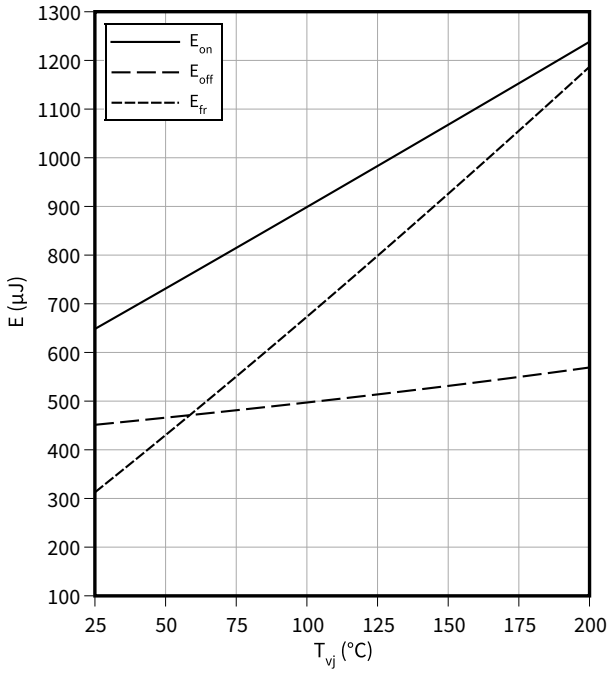
$T_{vj} = 175\ °C$, $t_p = 20\ \mu s$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(T_{vj})$

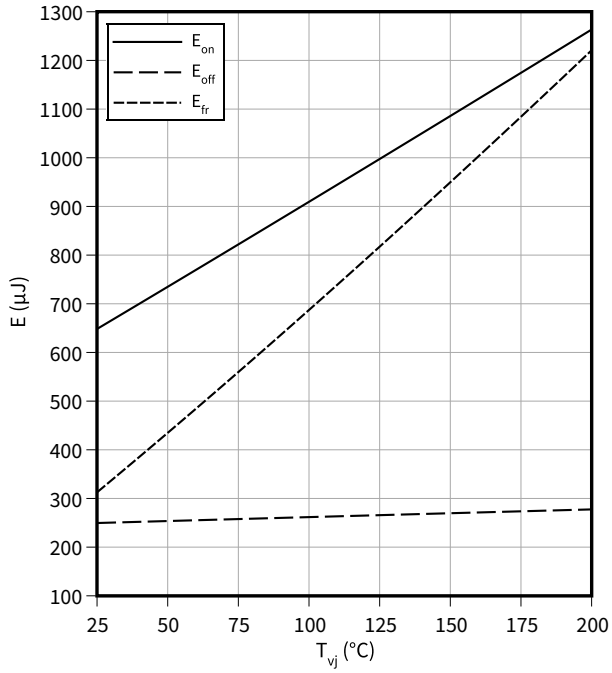
$V_{GS} = 0/18\ V$, $I_D = 69\ A$, $R_{G,ext} = 2.3\ \Omega$, $V_{DD} = 800\ V$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(T_{vj})$

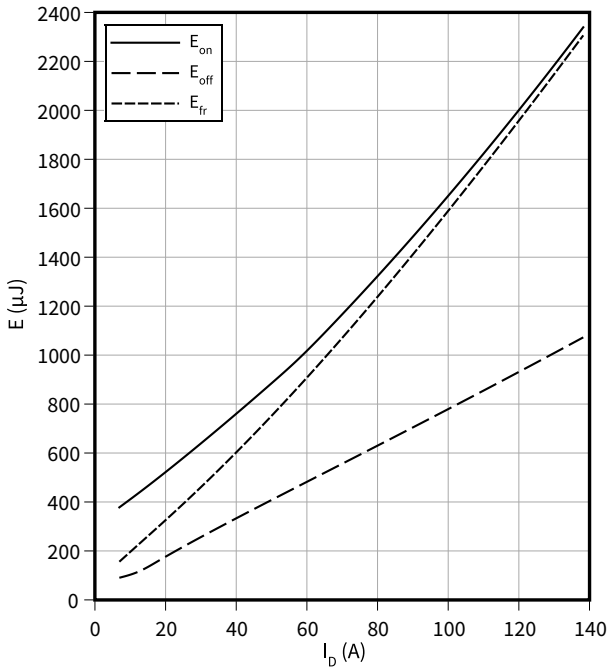
$V_{GS} = -5/18\ V$, $I_D = 69\ A$, $R_{G,ext} = 2.3\ \Omega$, $V_{DD} = 800\ V$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(I_D)$

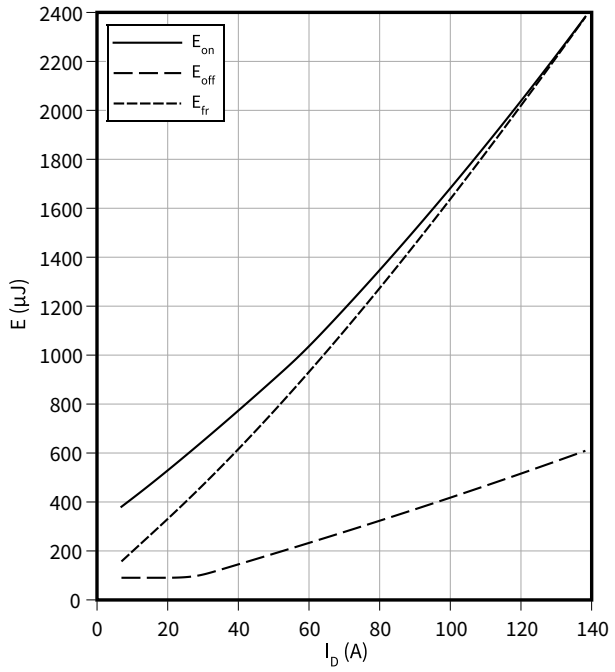
V_{GS} = 0/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(I_D)$

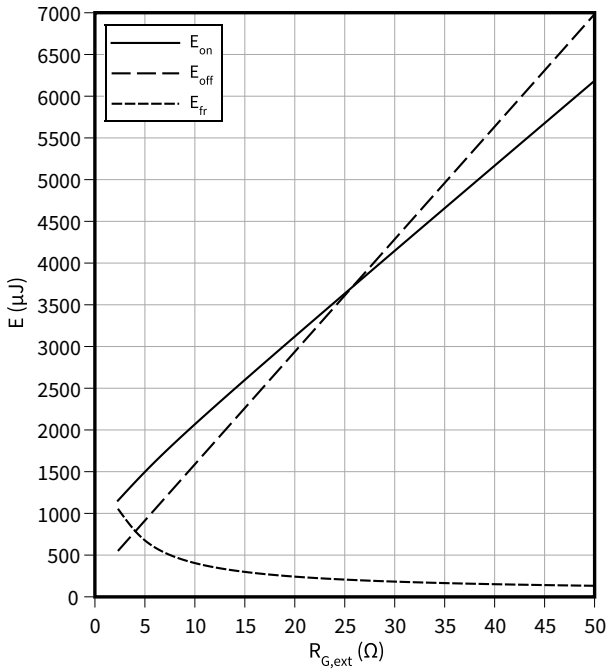
V_{GS} = -5/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

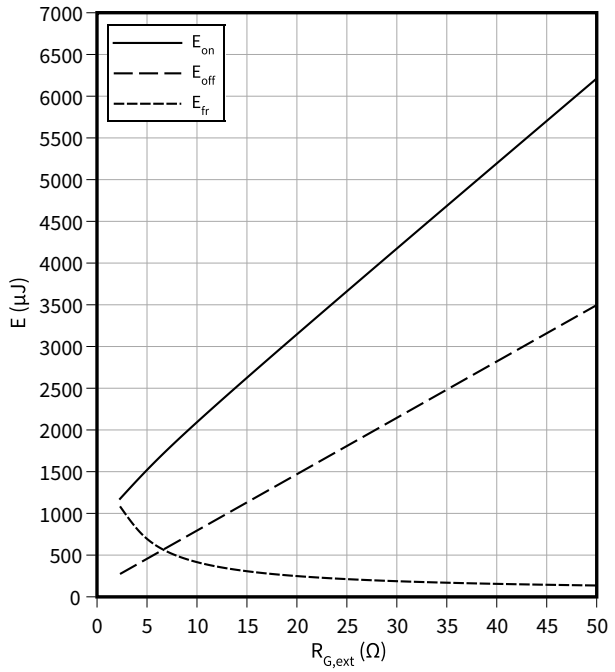
V_{GS} = 0/18 V, I_D = 69 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(R_{G,ext})$

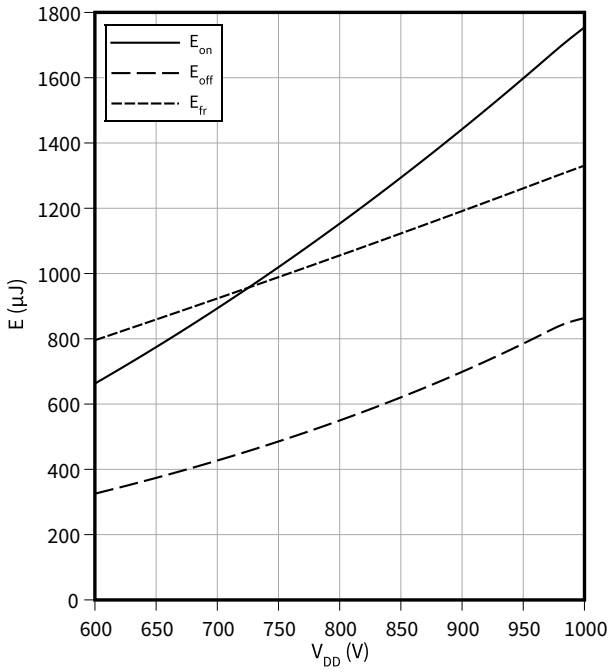
V_{GS} = -5/18 V, I_D = 69 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(V_{DD})$

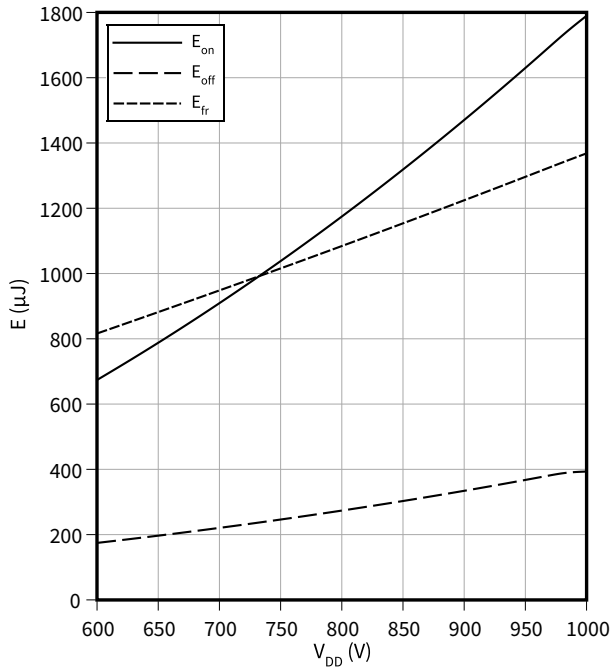
V_{GS} = 0/18 V, I_D = 69 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(V_{DD})$

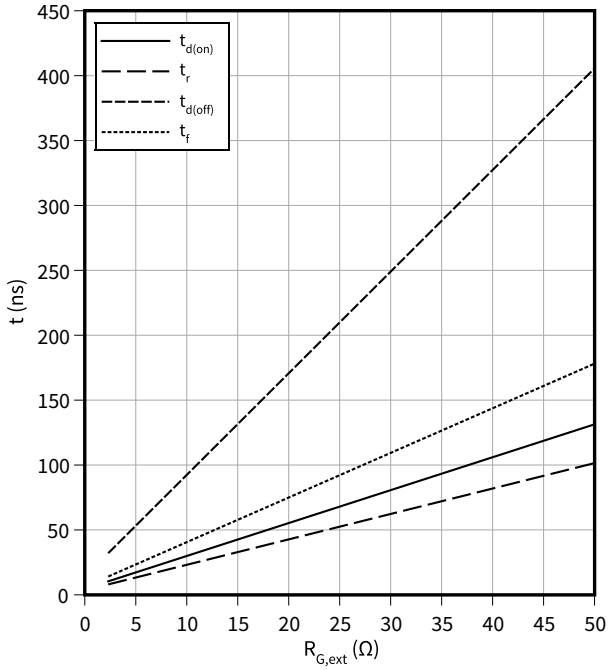
V_{GS} = -5/18 V, I_D = 69 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$t = f(R_{G,ext})$

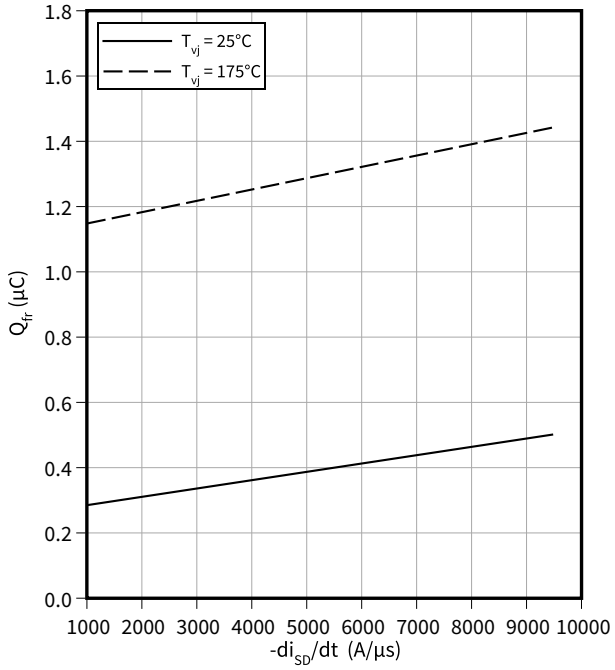
V_{GS} = 0/18 V, I_D = 69 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$Q_{fr} = f(-di_{SD}/dt)$

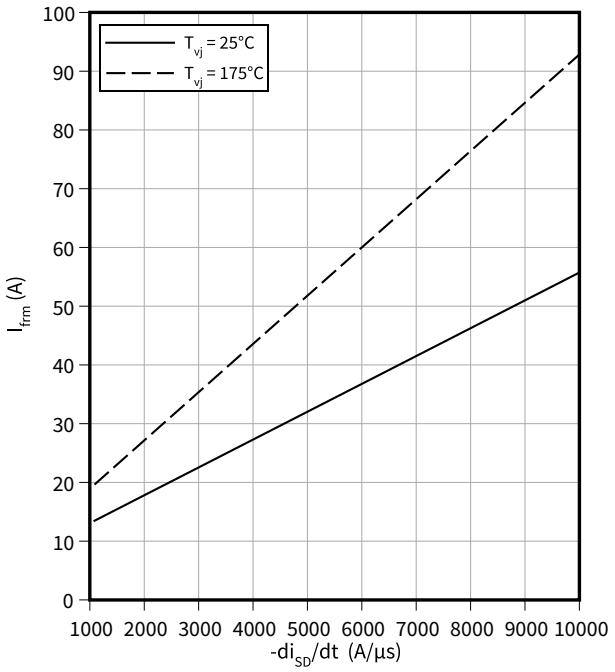
V_{GS} = 0/18 V, I_{SD} = 69 A, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$I_{frm} = f(-di_{SD}/dt)$

V_{GS} = 0/18 V, I_{SD} = 69 A, V_{DD} = 800 V

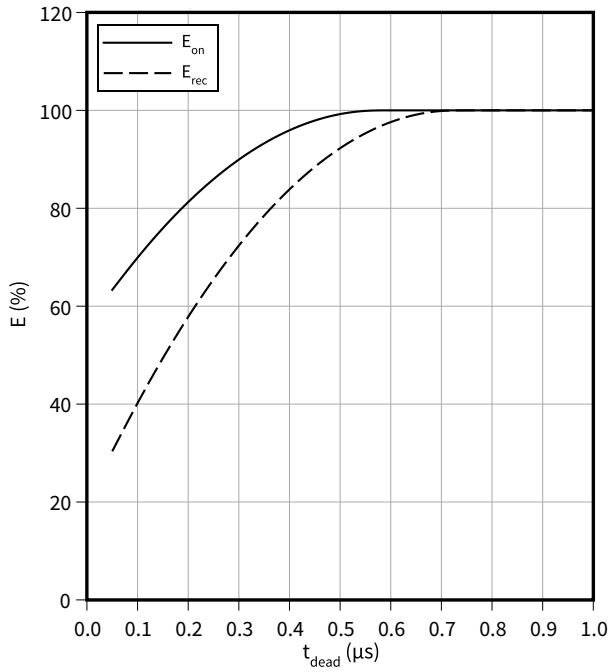


Typical switching energy as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(t_{dead})$

V_{GS} = 0/18 V, I_D = 69 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω

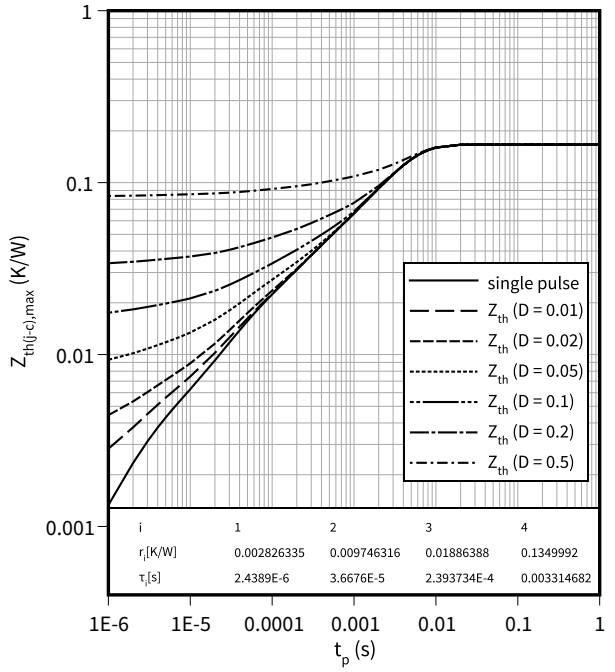
V_{DD} = 800 V



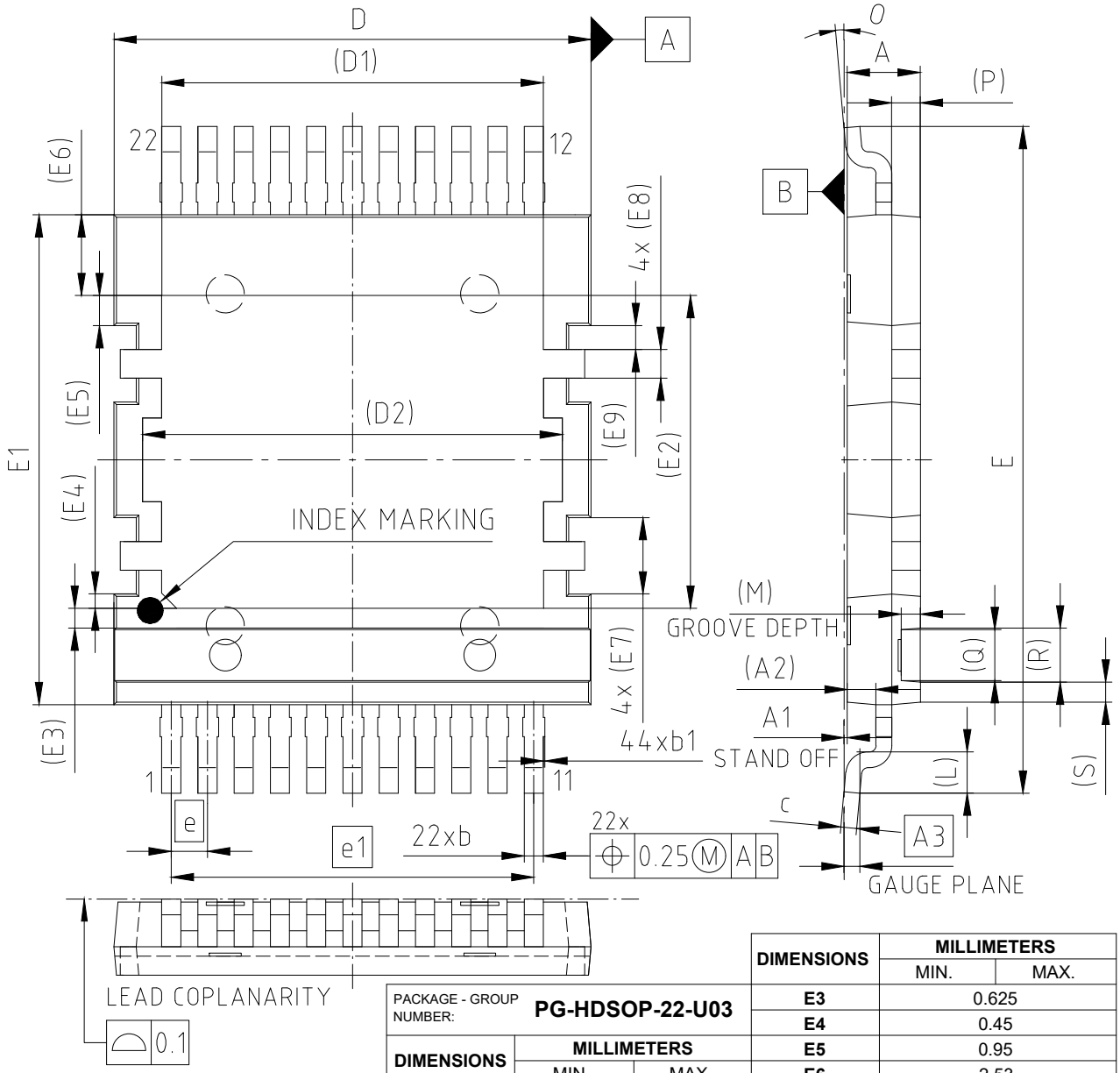
Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



5 Package outlines



NOTES:

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER:	PG-HDSOP-22-U03	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.90	
A3	0.50	
b	0.50	0.70
b1	---	0.15
c	0.46	0.58
D	14.90	15.10
D1	12.00	
D2	13.20	
E	20.81	21.11
E1	15.30	15.50
E2	9.83	

DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
E3	0.625	
E4	0.45	
E5	0.95	
E6	2.53	
E7	2.40	
E8	0.90	
E9	0.75	
e	1.14	
e1	11.4	
L	1.30	
M	0.60	
N	22	
O	0°	8°
P	0.90	
Q	1.60	
R	1.70	
S	0.631	

Figure 1

6 Testing conditions

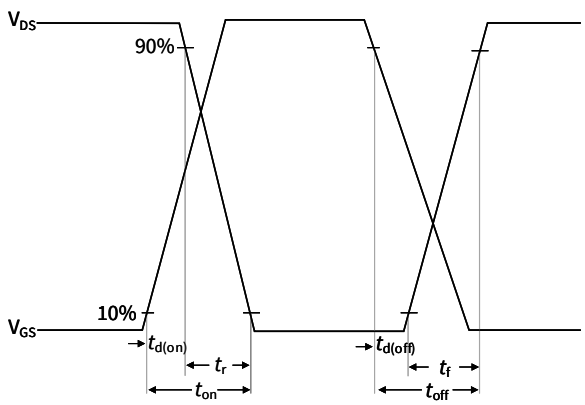


Figure A. **Definition of switching times**

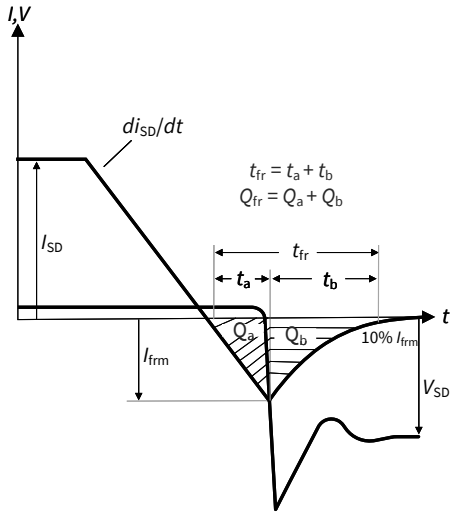


Figure B. **Definition of body diode switching characteristics**

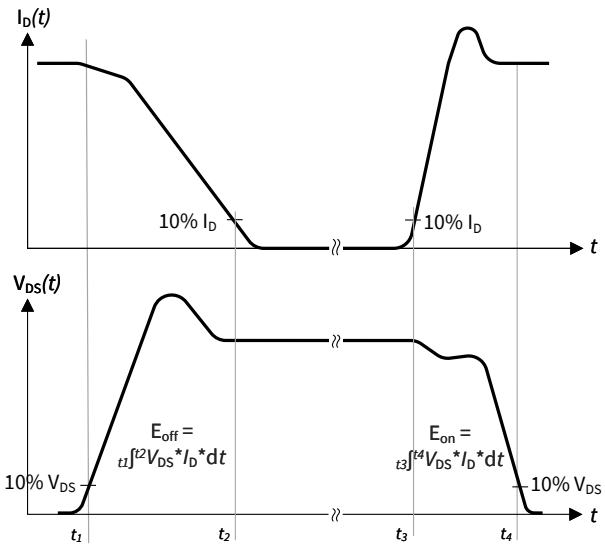


Figure C. **Definition of switching losses**

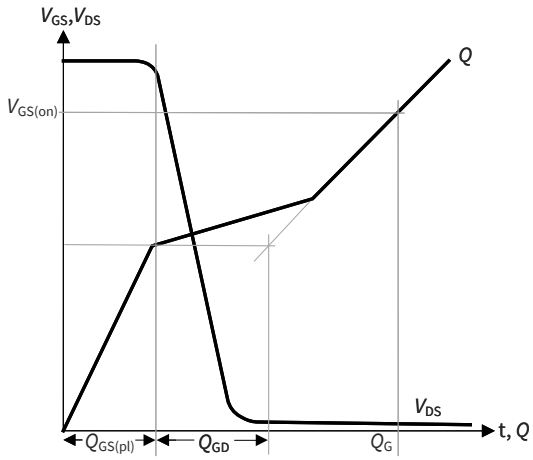


Figure D. **Definition of QGD**

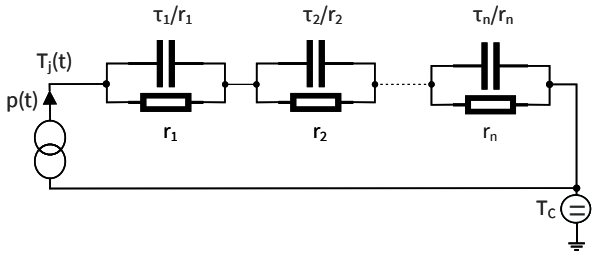


Figure E. **Thermal equivalent circuit**

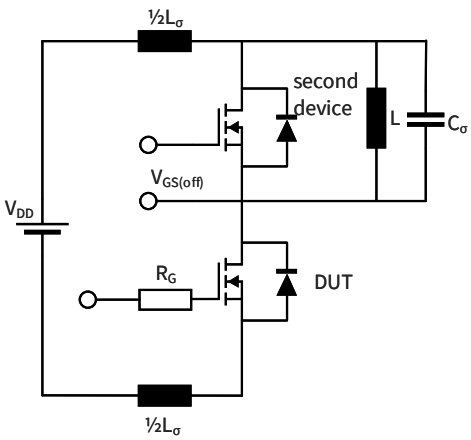


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2024-06-05	Target datasheet
0.20	2024-11-20	Preliminary datasheet
1.00	2024-12-12	Final datasheet
1.10	2025-11-13	Added CTI in Table 1 Increased I_{DM} in Table 2 Added switching information for V_{GS} = -5/18 V in Table 4 and 6 and corresponding diagrams Added I_{SDC} in Table 5 Corrected test conditions and adapt values of the body diode in Table 6 Added SOA diagram on page 8 Added diagram E = f(V_{DD}) @ V_{GS} = 0/18 V Added diagram E = f(V_{DD}) @ V_{GS} = -5/18 V Editorial changes
1.20	2026-07-27	Correction of the internal gate resistance in Table 4 Correction of switching times and energies in Table 4 and corresponding diagrams Correction of Q_{fr}, I_{frm} and E_{fr} in Table 6 and corresponding diagrams Updated I_{DSS} max in Table 4

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Edition 2026-07-27

Published by

Infineon Technologies AG

81726 Munich, Germany

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IFX-ABI273-005

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