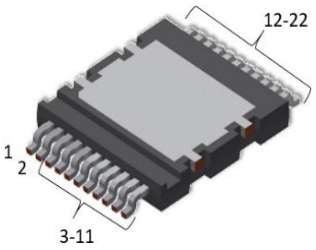
Final datasheet

英飞凌 CoolSiC™ 1200 V SiC MOSFET G2： Q-DPAK 顶部冷却

特性



- T_{vj} = 25°C 时 V_{DSS} = 1200 V
- T_C = 100°C 时 I_{DDC} = 242 A
- $R_{DS(on)}$ = 5 mΩ (V_{GS} = 18 V、 T_{vj} = 25°C时)
- 开关损耗非常低
- 过载运行最高结温可达 T_{vj} = 200°C
- 基准栅极阈值电压，$V_{GS(th)}$ = 4.2 V
- 具有抗寄生导通能力，可应用 0 V 关断栅极电压
- 坚固的体二极管，适用于硬换向
- .XT 互连技术，实现行业领先的热性能
- 合适的英飞凌栅极驱动器可在 https://www.infineon.com/gdfinder 找到

Halogen-free
Green
Lead-free
RoHS

潜在应用

- 固态断路器/固态继电器
- 电动汽车充电桩
- 在线式UPS/工业UPS
- 组串式逆变器
- 通用驱动器（GPD）
- CAV
- 伺服驱动器

产品验证

- 符合 JEDEC47/20/22 相关测试的工业应用要求

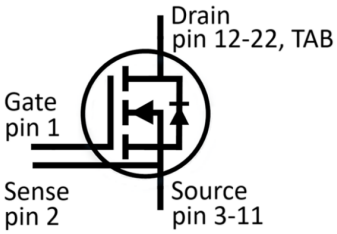
描述

引脚定义：

- Pin 1 – 栅极
- Pin 2 – 开尔文检测触点
- 引脚 3-11 – 源极
- 引脚 12-22，TAB – 漏极

注：源极引脚和检测引脚不可互换，互换可能会导致故障

Type	Package	Marking
IMCQ120R005M2H	PG-HDSOP-22-U03	12M2H005



本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

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1 封装

表 1 特征值

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	Reflow soldering (MSL2 according to JEDEC J-STD-020)			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.08	0.11	K/W
Comparative Tracking Index	*CTI*	IEC 60112 (material group 1 according to IEC 60664-1)	600			V

2 MOSFET

表 2 最大额定值

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	342	A
			$T_c = 100$ °C	242	
Peak drain current, t_p limited by $T_{vj(max)}$ [1)]	I_{DM}	$V_{GS} = 18$ V		1210	A
Gate-source voltage, max. transient voltage	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage [2)]	V_{GS}			-7...23	V
Avalanche energy, single pulse	E_{AS}	$I_D = 69$ A, $V_{DD} = 50$ V, $L = 0.4$ mH, $T_{vj(start)} = 25$ °C		868	mJ
Avalanche energy, repetitive	E_{AR}	$I_D = 69$ A, $V_{DD} = 50$ V, $L = 1.8$ µH, $T_{vj(start)} = 25$ °C		4.34	mJ
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	1364	W
			$T_c = 100$ °C	682	

1) 已通过设计验证。
2) 应用设计中的最大栅源电压应符合 IPC-9592B 的规定。

表 3　　推荐值

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

表 4　　特征值

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 138.2 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		5		mΩ
			T_{vj} = 150 °C, $V_{GS(on)}$ = 18 V		10.2	13.6	
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		11.9		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		6.3		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 43.4 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.1	V
			T_{vj} = 175 °C		3.2		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			1200	µA
			T_{vj} = 175 °C		20.4		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			120	nA
			V_{GS} = -10 V			-120	
Forward transconductance	g_{fs}	I_D = 138.2 A, V_{DS} = 20 V			91		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			2.55		Ω
Input capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			9.76		nF
Output capacitance	C_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			428		pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			37.3		pF
C_{oss} stored energy	E_{oss}	Calculated based on C_{oss} = f(V_{DD})			181		µJ
Output charge	Q_{oss}	Calculated based on C_{oss} = f(V_{DD})			670		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on E_{oss}			564		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{DS} = 0...800 V, V_{GS} = 0 V, Calculated based on Q_{oss}			838		pF
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, turn-on pulse			261		nC

（表格续下页……）

表 4　　（续）特征值

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, turn-on pulse			57.3		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, turn-on pulse			64.2		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		32		ns
			T_{vj} = 175 °C		24.4		
Rise time	t_r	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		21.3		ns
			T_{vj} = 175 °C		19		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		64.4		ns
			T_{vj} = 175 °C		75.3		
Fall time	t_f	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		28.2		ns
			T_{vj} = 175 °C		33.3		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		2.38		mJ
			T_{vj} = 175 °C		3.3		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		2.53		mJ
			T_{vj} = 175 °C		3.04		
Total switching energy[1)]	E_{tot}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		5.52		mJ
			T_{vj} = 175 °C		8.44		

（表格续下页……）

表 4　　（续）特征值

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Turn-on energy at -5 V	E_{on}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		2.36		mJ
			T_{vj} = 175 °C		3.27		
Turn-off energy at -5 V	E_{off}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		1.46		mJ
			T_{vj} = 175 °C		1.56		
Total switching energy at -5 V[1)]	E_{tot}	V_{DD} = 800 V, I_D = 138.2 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		4.43		µJ
			T_{vj} = 175 °C		6.98		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[2)]				200	°C

1)　包括 E_{fr}
2)　最多 5000 次循环。最大Δ T 限制为 100 K。

注： *芯片技术的特征是高达200 kV/µs。测量的dV/dt 受到测量测试设置和封装的限制。*

除非另有规定，特性均在 T_{vj} = 25°C 的条件下测得。

3　体二极管（MOSFET）

表 5　　最大额定值

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} ≥ 25 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	250	A
			T_c = 100 °C	153.1	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	V_{GS} = 0 V		725	A

表 6　　特征值

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 138.2 A, V_{GS} = 0 V	T_{vj} = 25 °C		4.2	5.5	V
			T_{vj} = 100 °C		4.1		
			T_{vj} = 175 °C		4		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 138.2 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		0.74		µC
			T_{vj} = 175 °C		2.56		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 138.2 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		95		A
			T_{vj} = 175 °C		162		
MOSFET forward recovery energy	E_{fr}	V_{DD} = 800 V, I_{SD} = 138.2 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		0.6		mJ
			T_{vj} = 175 °C		2.1		
MOSFET forward recovery energy at -5 V	E_{fr}	V_{DD} = 800 V, I_{SD} = 138.2 A, V_{GS} = -5 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		0.61		µJ
			T_{vj} = 175 °C		2.1		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[1)]				200	°C

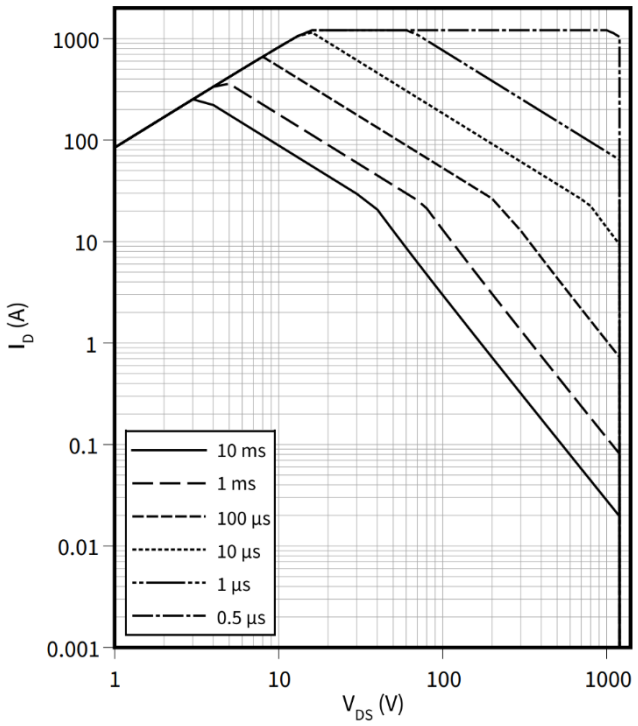
1)　最多 5000 次循环。最大Δ T 限制为 100 K。

4 特性图

Safe operating area (SOA)

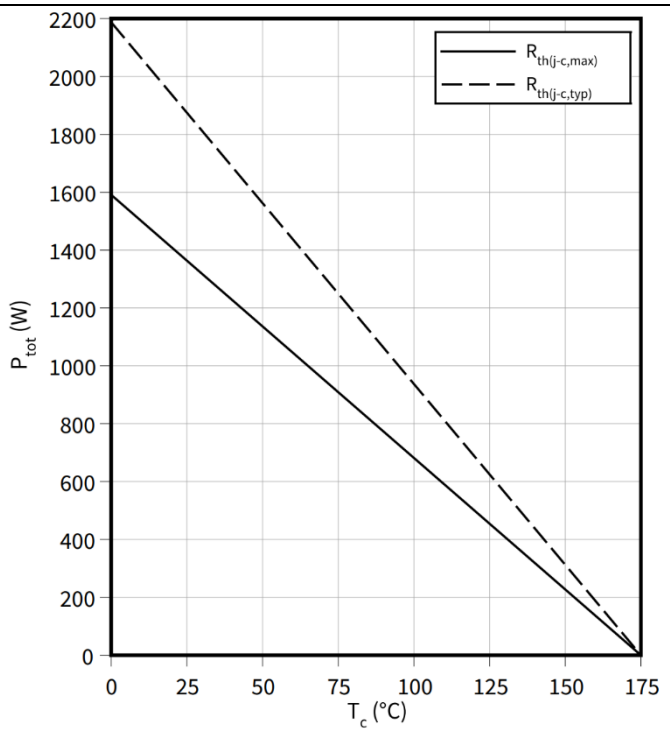
$I_D = f(V_{DS})$

$T_{vj} \leq 175\ °C$, $T_c = 25\ °C$



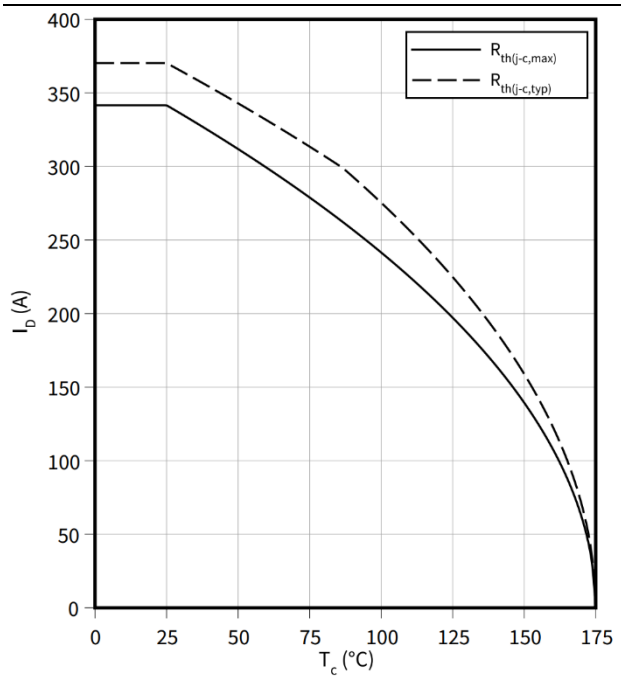
Power dissipation as a function of case temperature

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

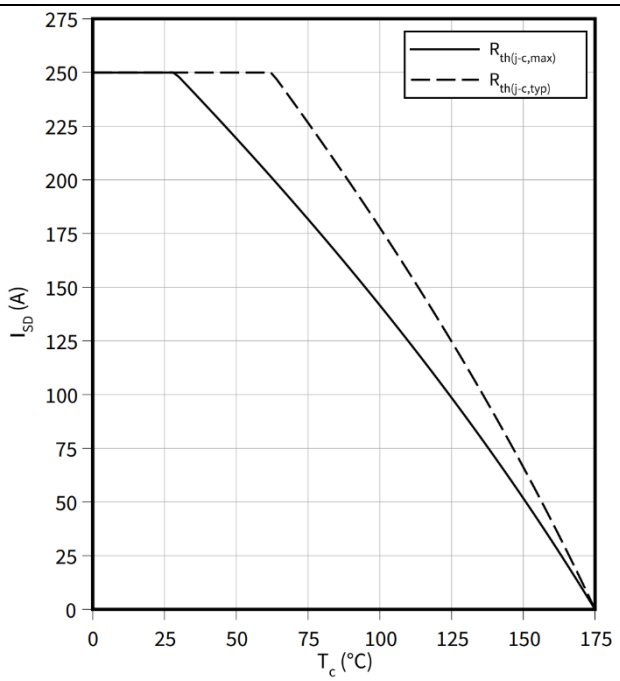
$I_D = f(T_c)$



Maximum source to drain current as a function of case temperature limited by bond wire

$I_{SD} = f(T_c)$

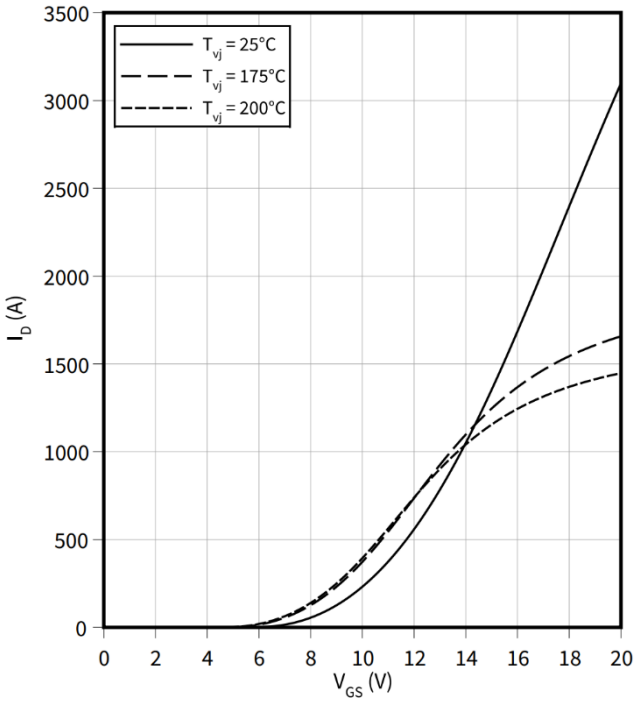
$V_{GS} = 0\ V$



Typical transfer characteristic

$I_D = f(V_{GS})$

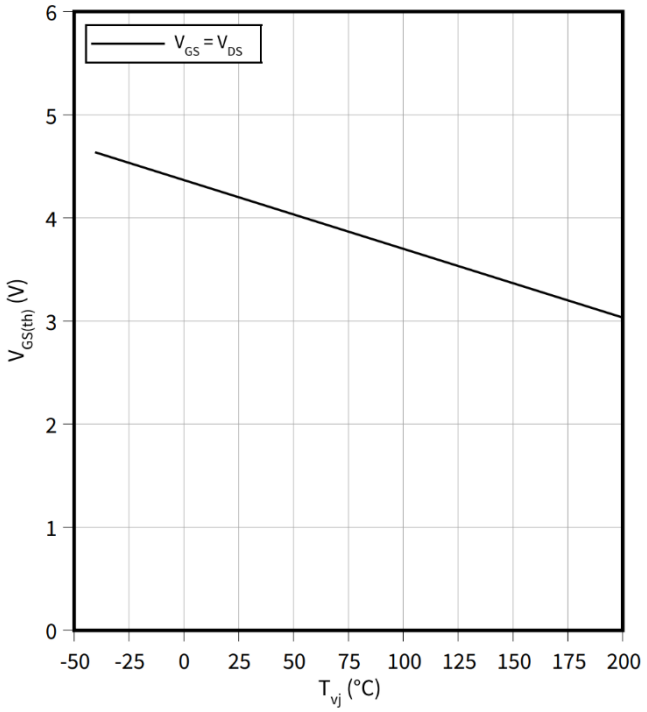
V_{DS} = 20 V, t_p = 20 µs



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

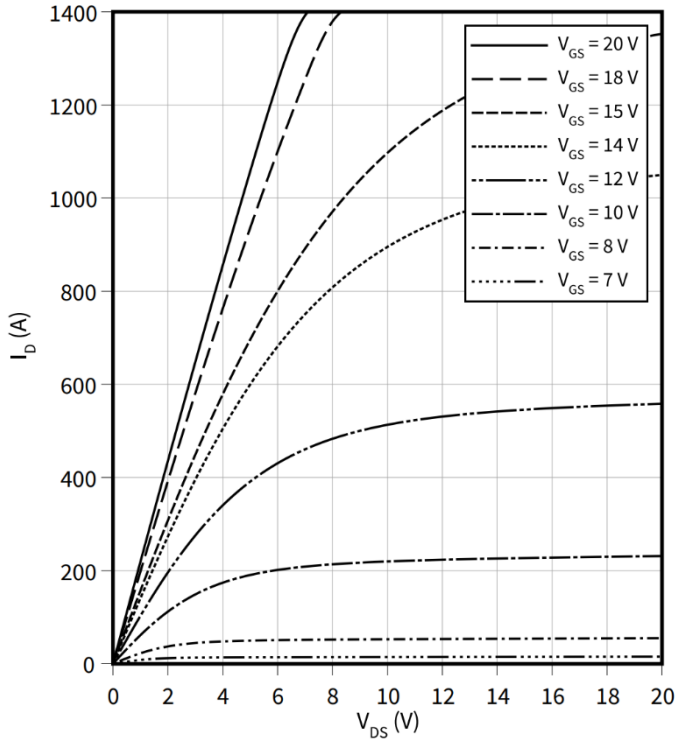
I_D = 43.4 mA



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

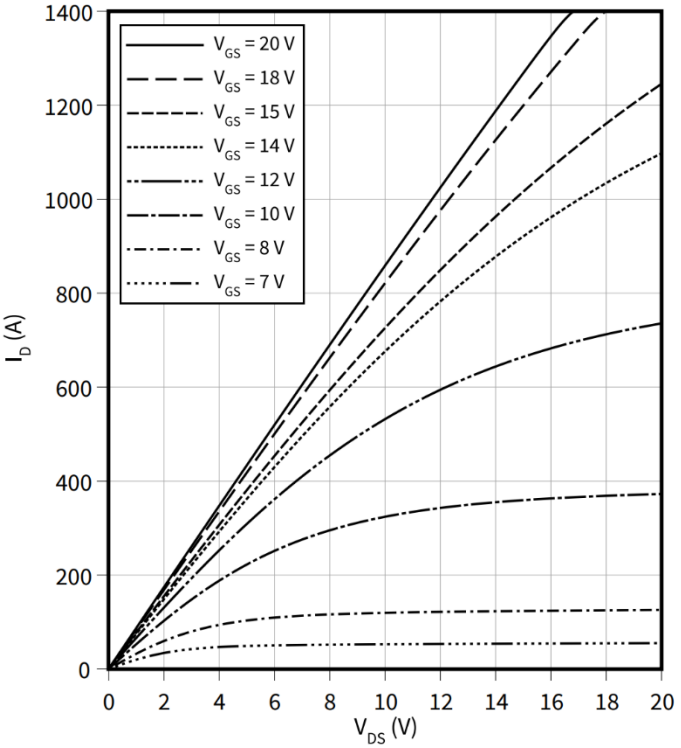
T_{vj} = 25 °C, t_p = 20 µs



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

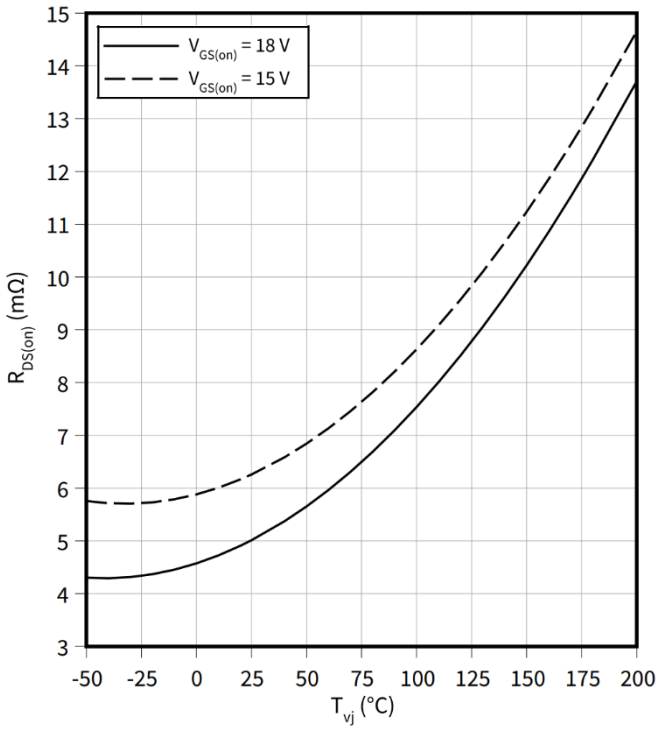
T_{vj} = 175 °C, t_p = 20 µs



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$

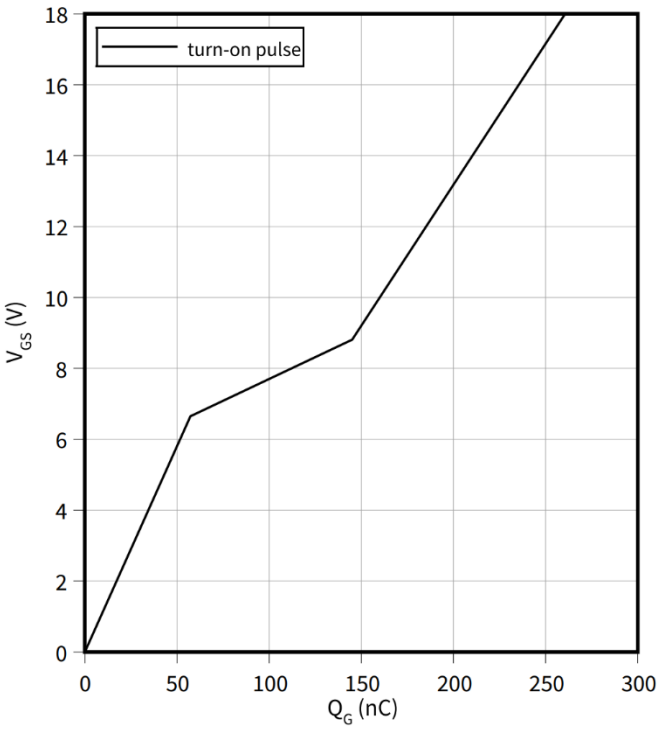
$I_D = 138.2$ A



Typical gate charge

$V_{GS} = f(Q_G)$

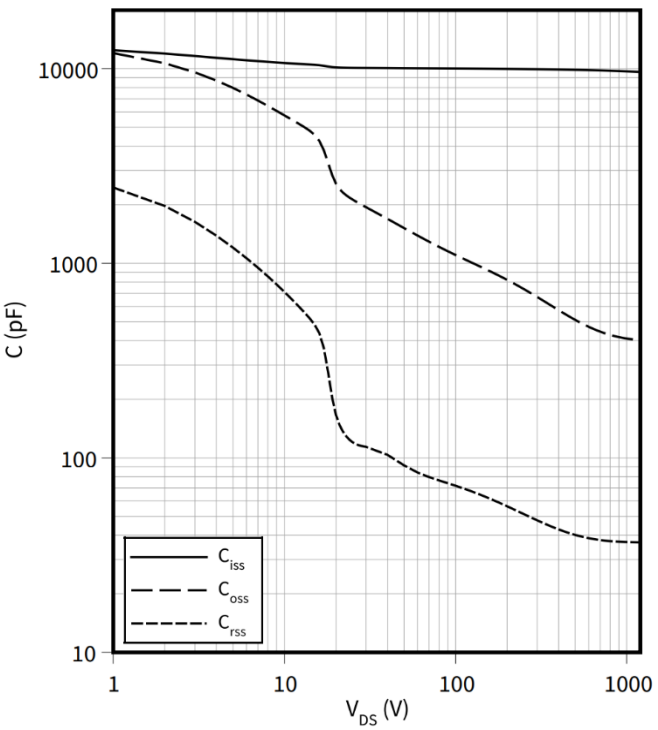
$I_D = 138.2$ A, $V_{DS} = 800$ V



Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$

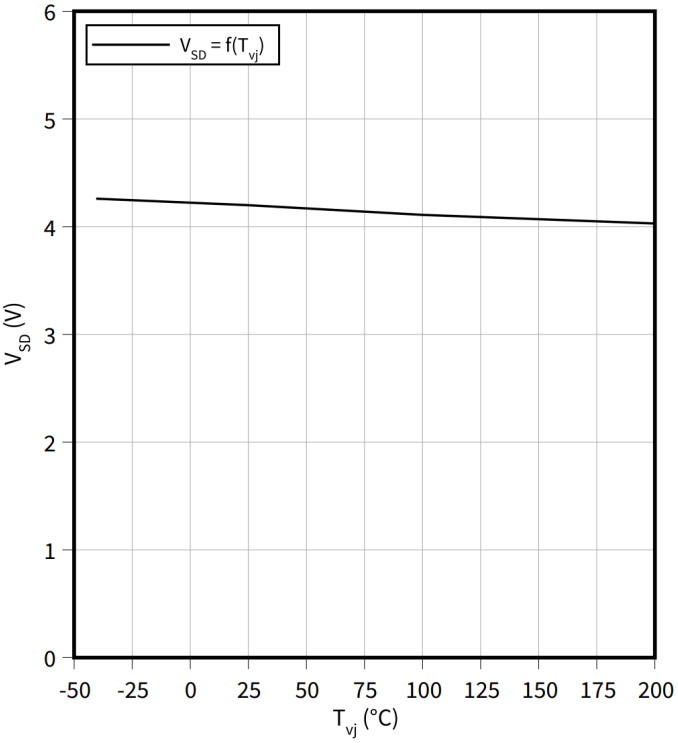
$f = 100$ kHz, $V_{GS} = 0$ V



Typical reverse drain voltage as a function of junction temperature

$V_{SD} = f(T_{vj})$

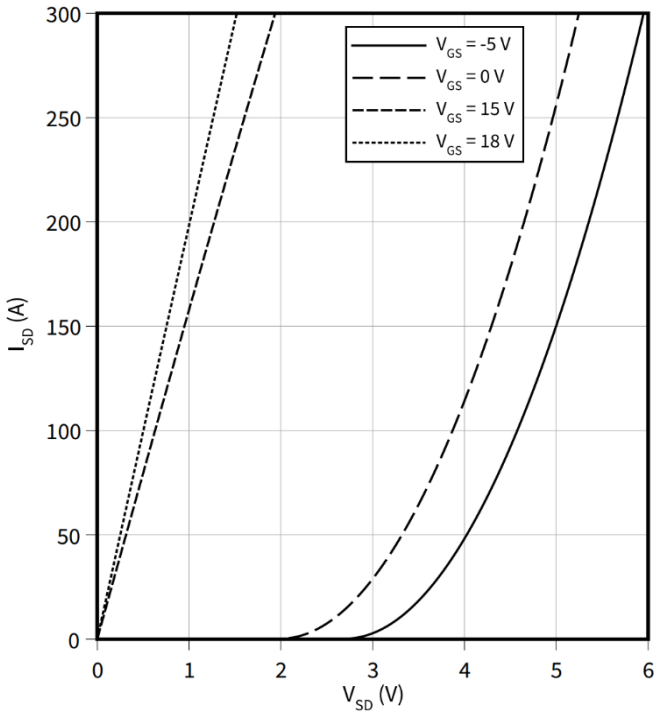
$I_{SD} = 138.2$ A, $V_{GS} = 0$ V



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

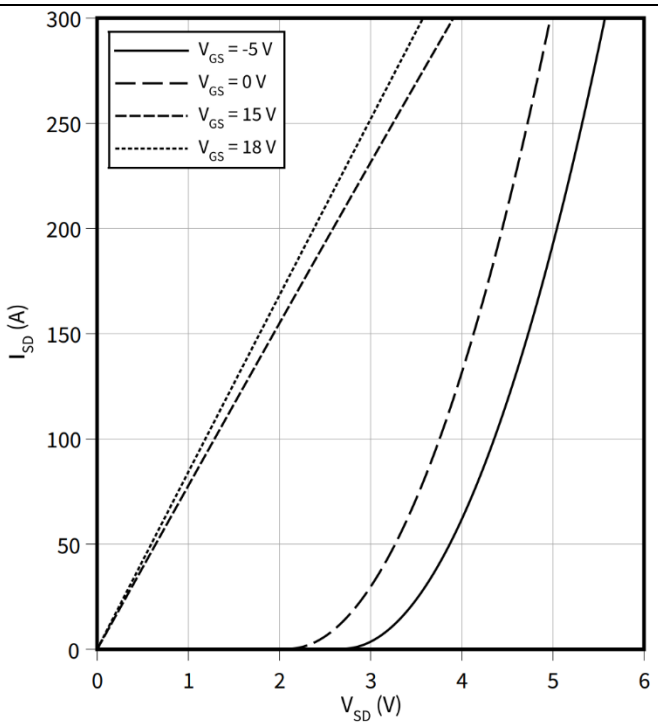
$T_{vj} = 25\ °C$, $t_p = 20\ µs$



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

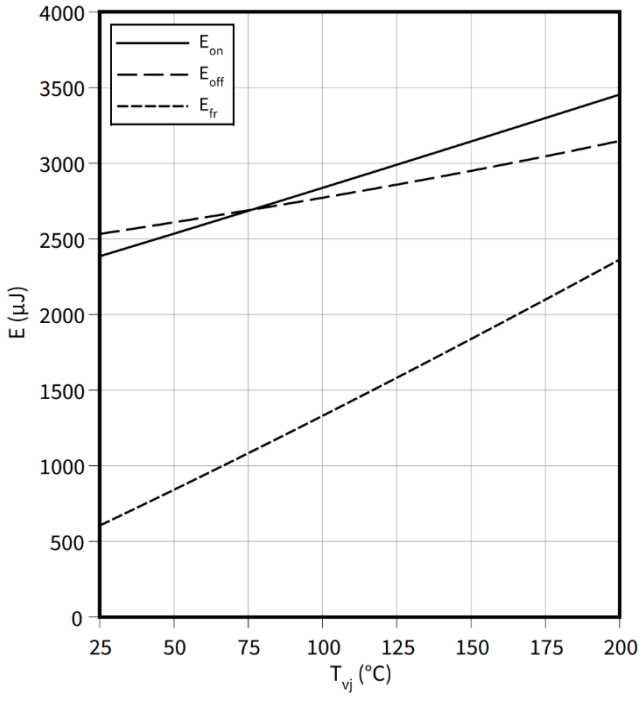
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(T_{vj})$

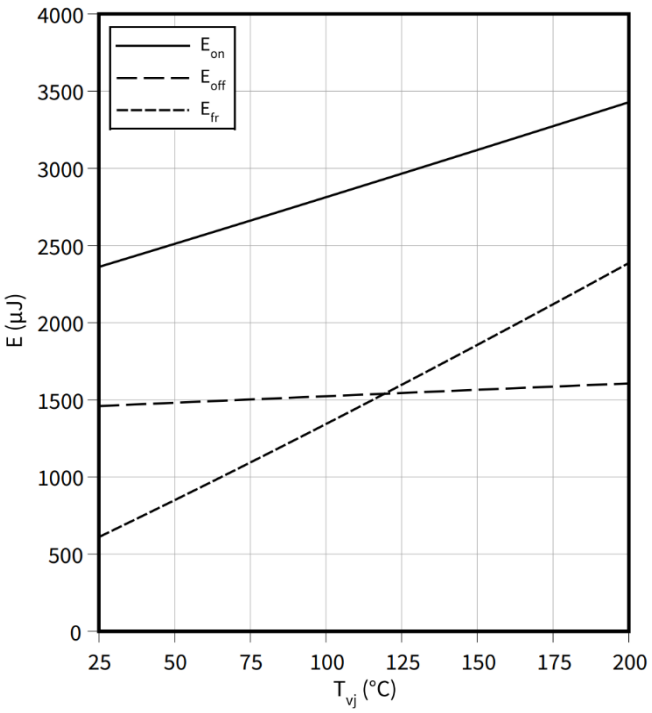
V_{GS} = 0/18 V, I_D = 138.2 A, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(T_{vj})$

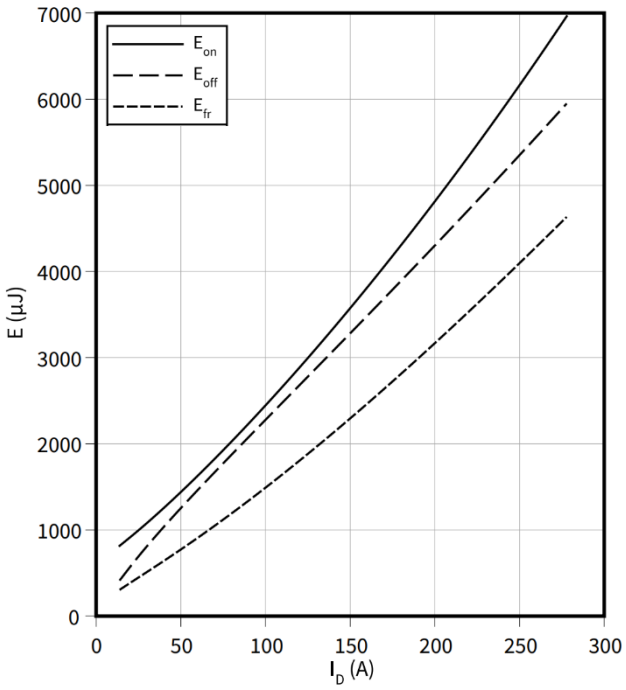
V_{GS} = -5/18 V, I_D = 138.2 A, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

E = f(I_D)

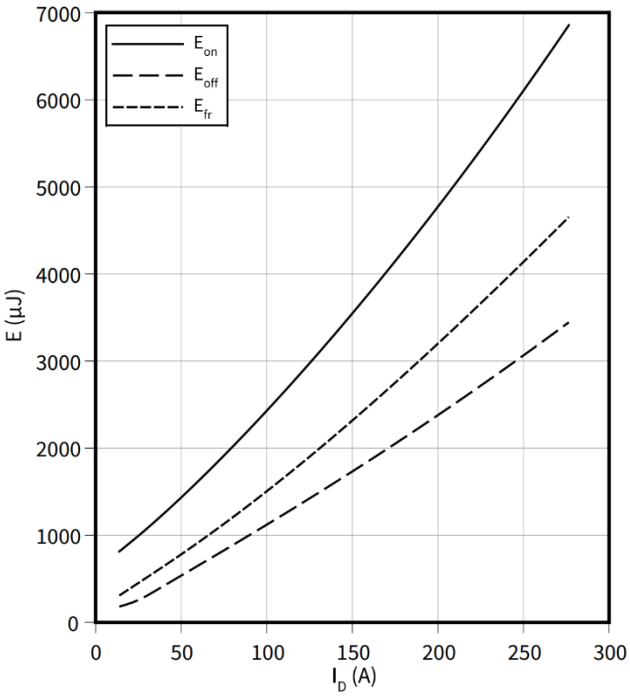
V_{GS} = 0/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

E = f(I_D)

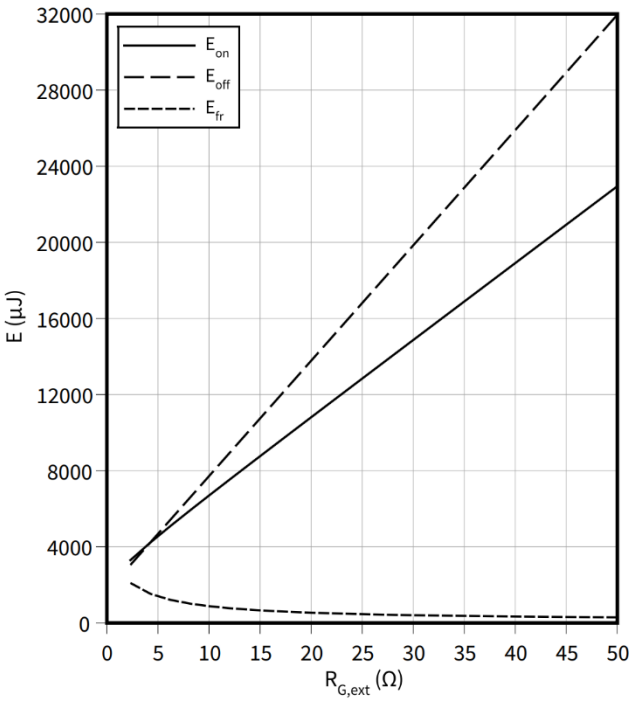
V_{GS} = -5/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

E = f($R_{G,ext}$)

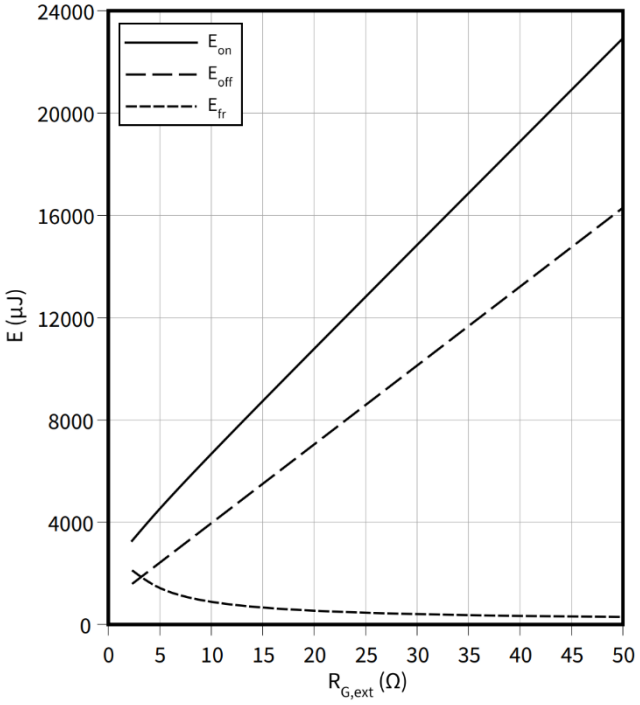
V_{GS} = 0/18 V, I_D = 138.2 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

E = f($R_{G,ext}$)

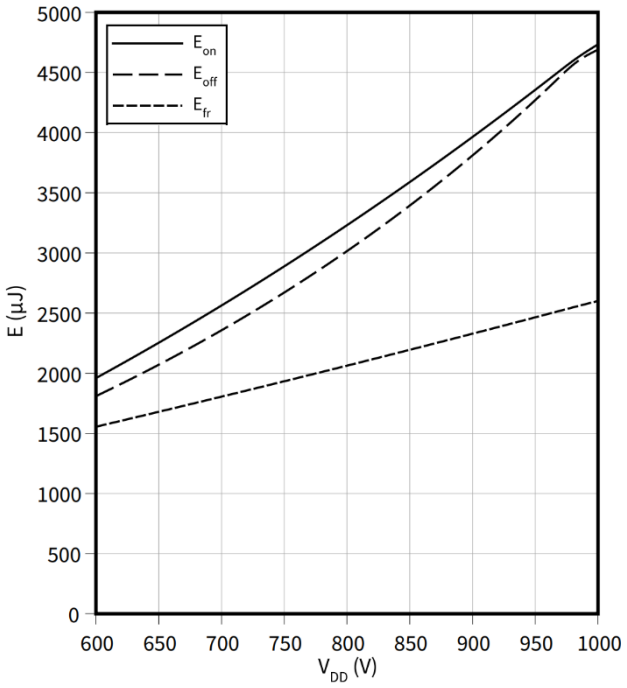
V_{GS} = -5/18 V, I_D = 138.2 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

E = f(V_{DD})

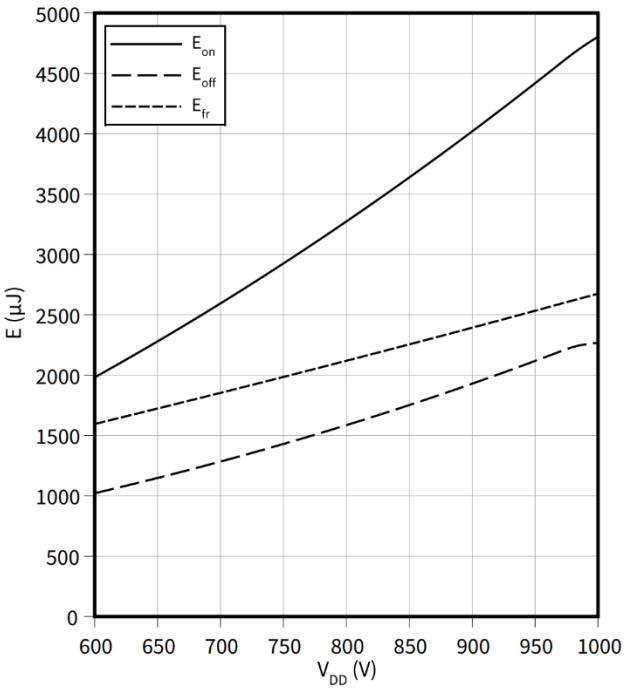
V_{GS} = 0/18 V, I_D = 138.2 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

E = f(V_{DD})

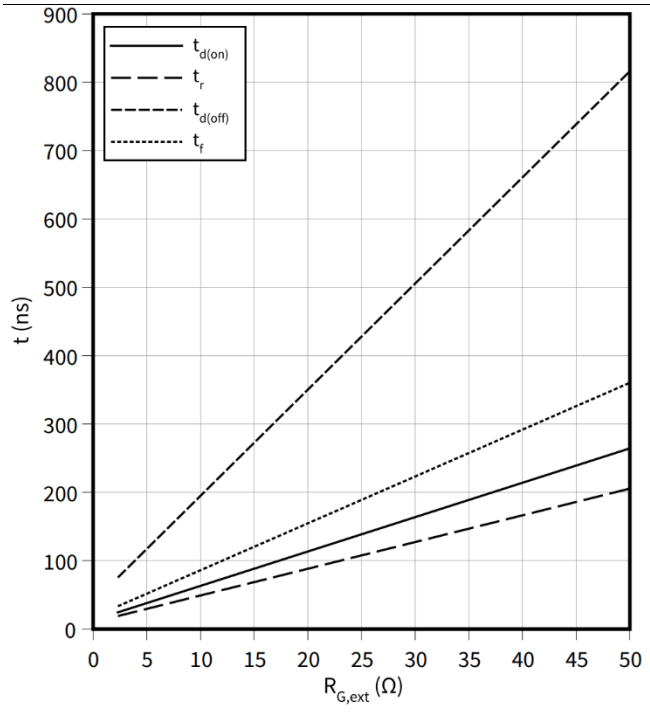
V_{GS} = -5/18 V, I_D = 138.2 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

t = f($R_{G,ext}$)

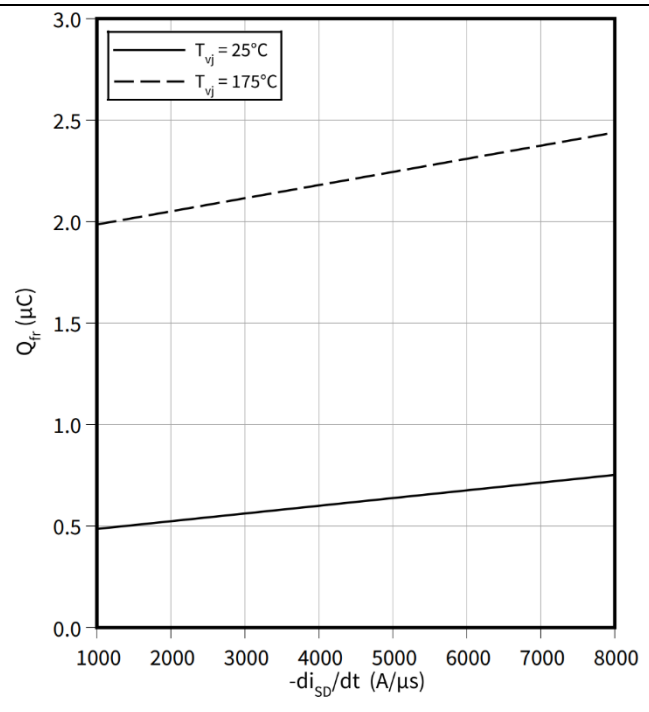
V_{GS} = 0/18 V, I_D = 138.2 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of revere drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

Q_{fr} = f(-di_{SD}/dt)

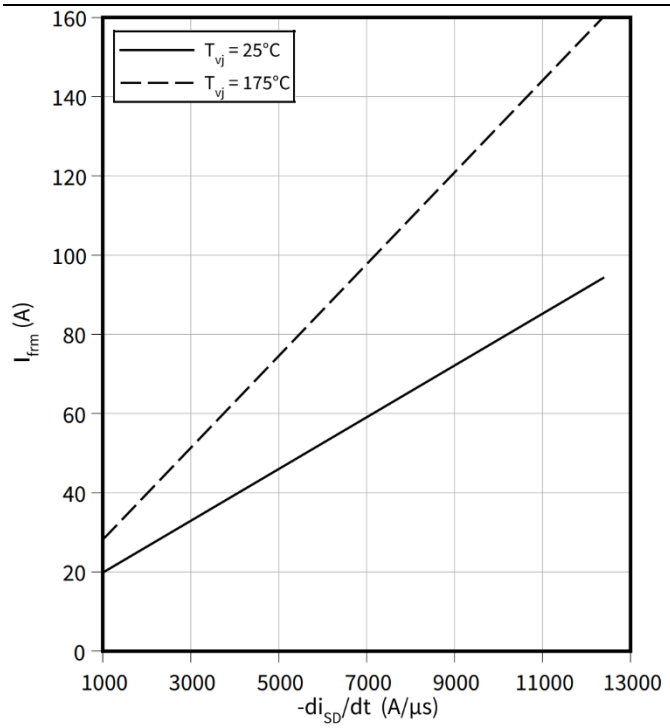
V_{GS} = 0/18 V, I_{SD} = 138.2 A, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$I_{frm} = f(-di_{SD}/dt)$

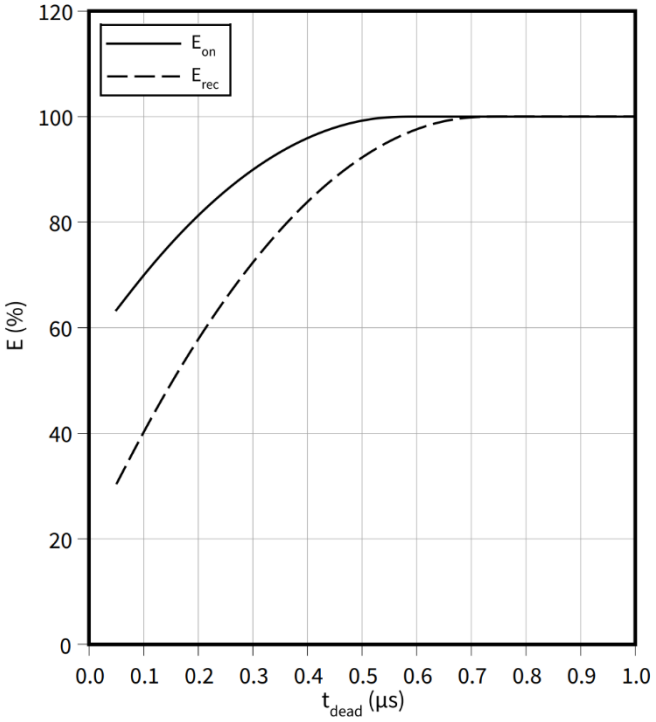
V_{GS} = 0/18 V, I_{SD} = 138.2 A, V_{DD} = 800 V



Typical switching energy as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(t_{dead})$

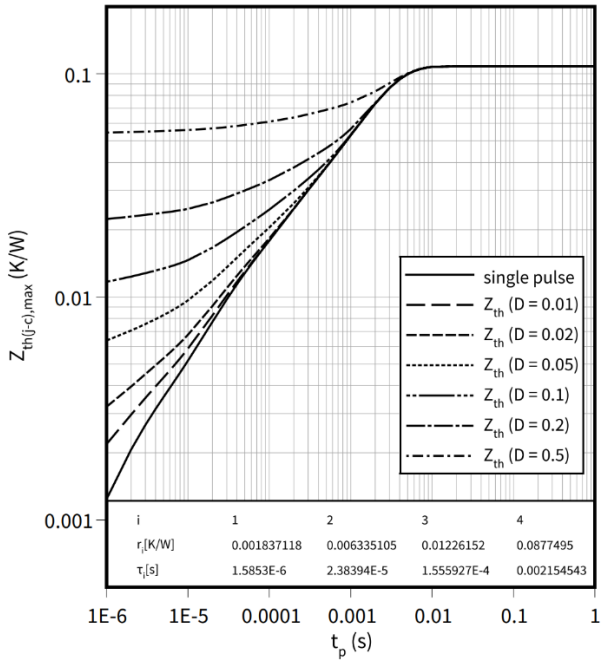
V_{GS} = 0/18 V, I_D = 138.2 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω V_{DD} = 800 V



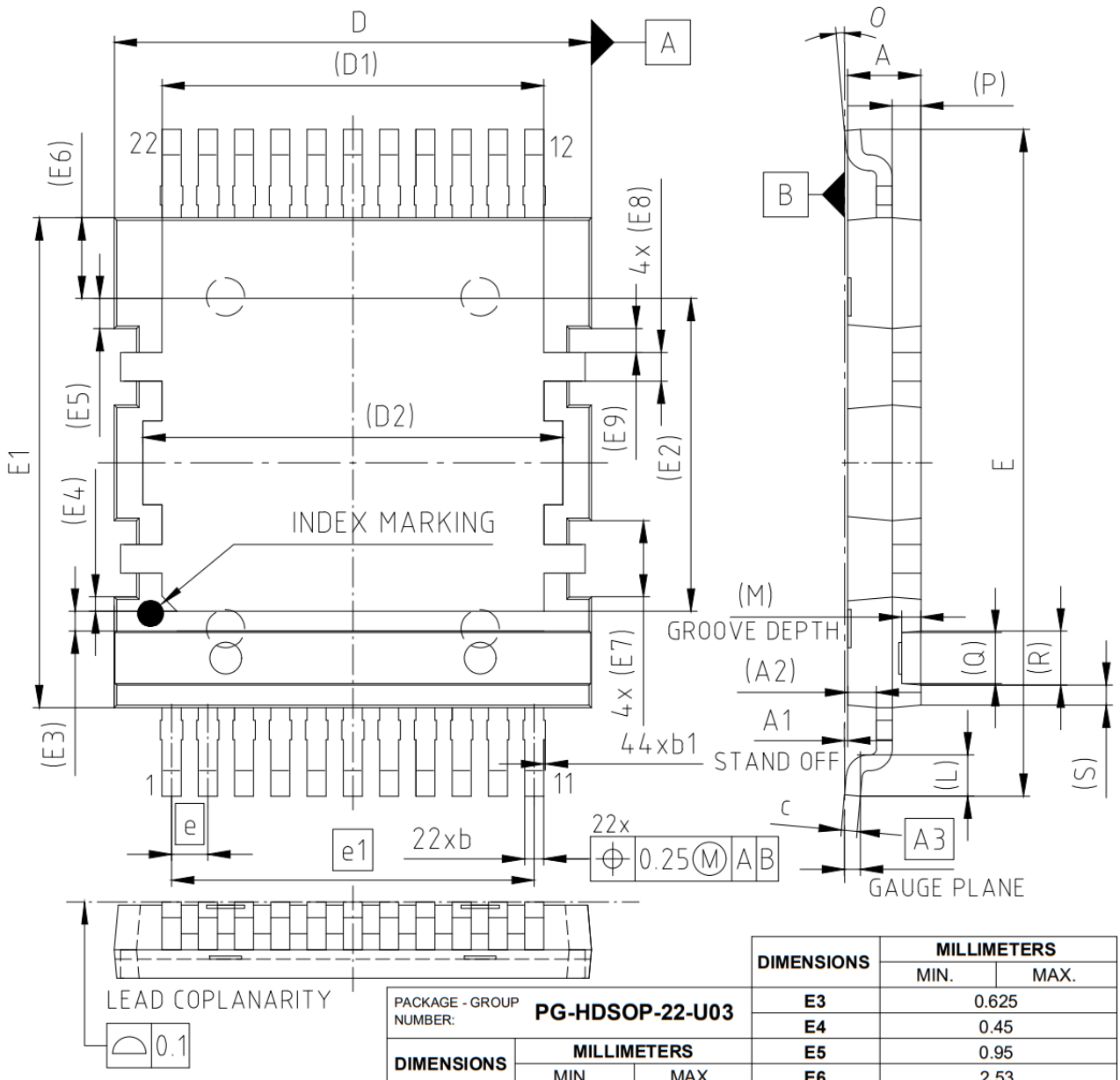
Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



5 封装外形



PACKAGE - GROUP NUMBER: **PG-HDSOP-22-U03**

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.90	
A3	0.50	
b	0.50	0.70
b1	---	0.15
c	0.46	0.58
D	14.90	15.10
D1	12.00	
D2	13.20	
E	20.81	21.11
E1	15.30	15.50
E2	9.83	

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
E3	0.625	
E4	0.45	
E5	0.95	
E6	2.53	
E7	2.40	
E8	0.90	
E9	0.75	
e	1.14	
e1	11.4	
L	1.30	
M	0.60	
N	22	
O	0°	8°
P	0.90	
Q	1.60	
R	1.70	
S	0.631	

NOTES:

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

图 1

6 测试条件

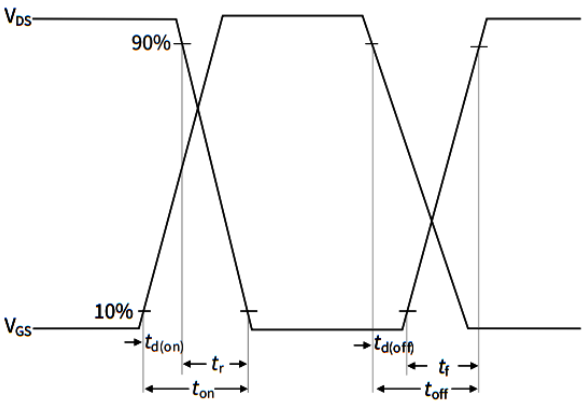


Figure A. **Definition of switching times**

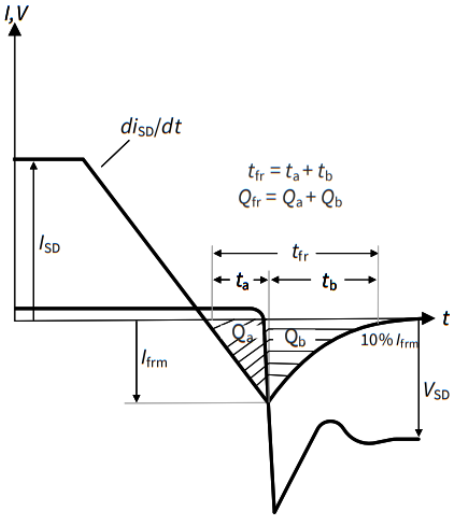


Figure B. **Definition of body diode switching characteristics**

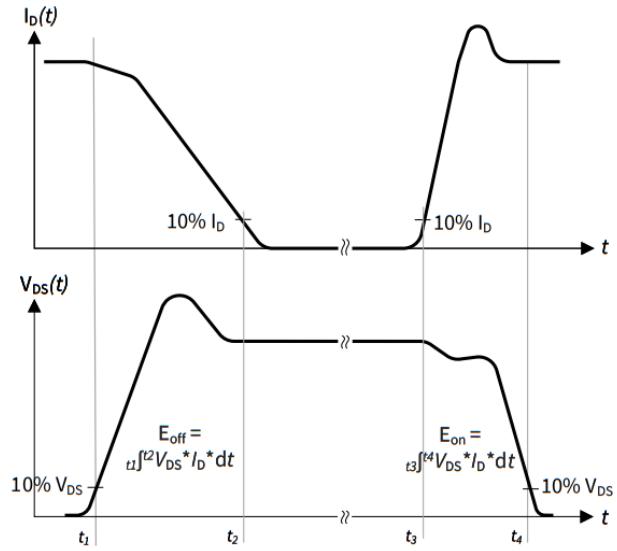


Figure C. **Definition of switching losses**

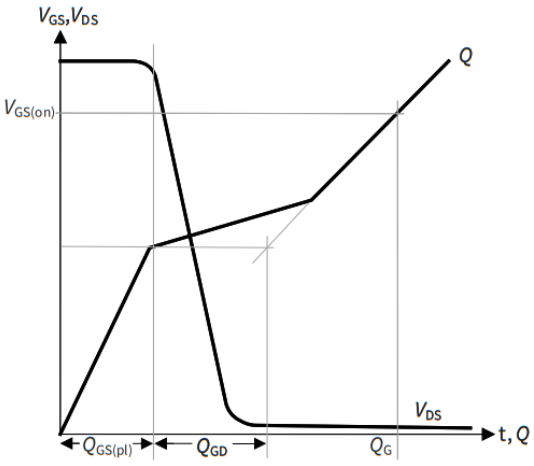


Figure D. **Definition of QGD**

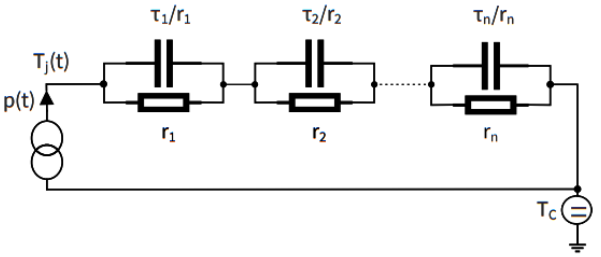


Figure E. **Thermal equivalent circuit**

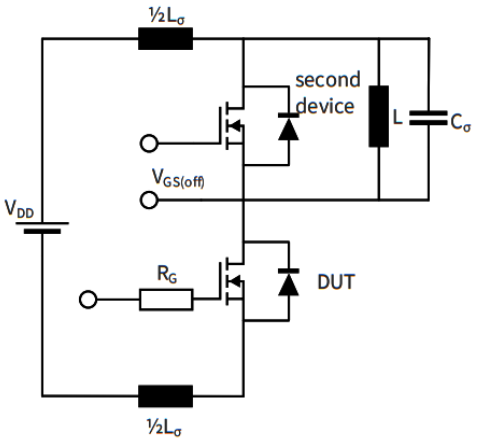


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

图 2

修订记录

Document revision	Date of release	Description of changes
0.10	2024-06-05	Target datasheet
0.20	2024-10-08	Preliminary datasheet
1.00	2025-07-04	Final datasheet
1.10	2025-10-13	Added CTI in Table 1 Increased I_{DM} in Table 2 Added switching information for V_{GS} = -5/18 V in Table 4 and 6 and corresponding diagrams Added I_{SDC} in Table 5 Corrected test conditions and adapt values of the body diode in Table 6 Added SOA diagram on page 8 Added diagram E = f(V_{DD}) @ V_{GS} = 0/18 V Added diagram E = f(V_{DD}) @ V_{GS} = -5/18 V Editorial changes

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