AEC-Q103 qualified high performance digital XENSIV™ MEMS microphone

Features

RoHS

AEC Qualified

Halogen-free

- Automotive qualification
- Flat frequency response down to 7 Hz for best ANC performance
- Close sensitivity and phase matching for optimum beam forming
- Extended availability to match automotive design cycles
- Digital PDM output
- Active THD compensation to reduce distortions at high SPL levels
- Small 3.5 x 2.65 x 0.98mm^3 surface-mount package
- Environmental robust up to IP57

Potential applications

- Active noise cancellation / Road noise cancellation (ANC/RNC)
- Hands free calling / Voice control
- Emergency call
- Siren detection
- Road condition detection

Product validation

Qualified for automotive applications by product validation according to AEC-Q103-003.

Description

The device is designed for applications where low self-noise (high SNR), wide dynamic range, low distortions and a high acoustic overload point are required. The low cut-off frequency (LFRO) makes it a well suited device for active noise cancelling (ANC) applications.

Infineon's MEMS technology is based on a miniaturized microphone design and results in high linearity of the output signal within a high dynamic range. With its low equivalent noise floor the microphone is no longer the limiting factor in the audio signal chain and enables higher performance of voice recognition algorithms.

The digital microphone ASIC contains a microphone specifc THD compensation algorithm for optimal performance at high sound pressure levels (SPL), an extremely low-noise preamplifier and a high-performance sigma-delta analog-to-digital converter (ADC).

The tight manufacturing tolerance, combined with the fact that each device is calibrated with an advanced Infineon calibration algorithm, results in small sensitivity and phase matching tolerances. This makes it well suited for beam forming arrays and multi-microphone applications.

Table 1 Product summary

Parameter	Value	Customer benefit
SNR	66 dB(A)	Improved speech quality and higher speech intelligibility
THD 1%	114 dB SPL	Clear speech up to high SPL levels
AOP (THD 10%)	120 dB SPL	Optimized dynamic range for 16-bit audio codecs
LFRO	7 Hz	Flat frequency response for best ANC performance
T_A	-40°C ... +105°C	Flexible placement inside and outside the car

Table 2 Order information

Product name	Package	Marking	Ordering code
IM66D120A	PG-TLGA-5-6	IA66D2	SP005926392

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1 Block diagram

The device contains two different dies combined inside one package.

The MEMS picks up the sound waves and converts them into an electrical signal. The ASIC contains all needed circuitry for biasing the MEMS and amplifying the MEMS signal to a stable and calibrated microphone output.

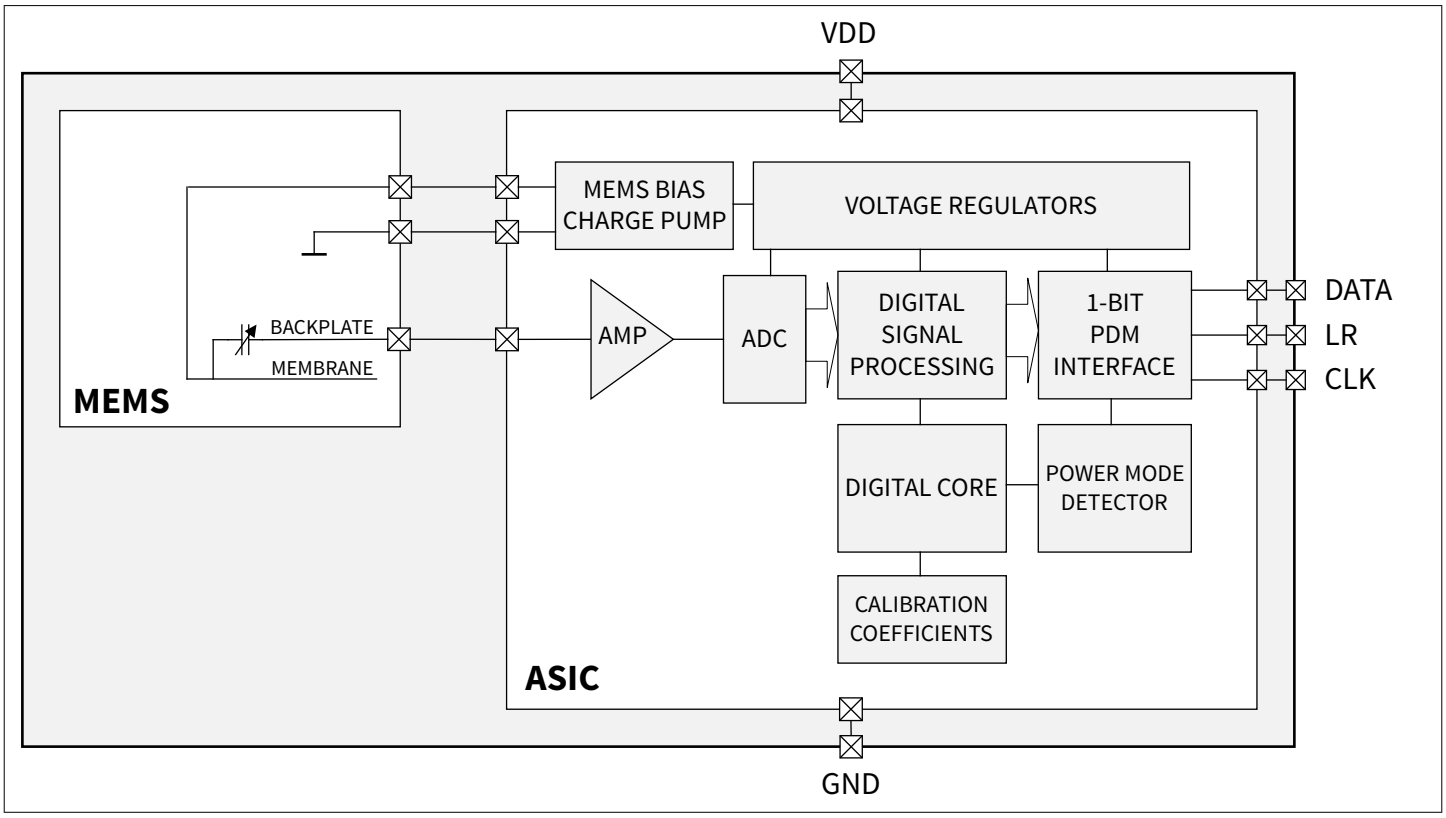


Figure 1 Block diagram

2 Pin configuration

The figure below shows the pin configuration of the device

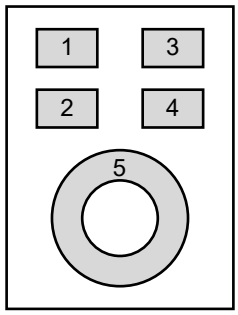


Figure 2 Pin configuration

Table 3 Pin configuration

Pin number	Name	Description
1	VDD	Power supply
2	CLK	PDM clock input
3	DATA	PDM data output
4	LR	PDM left/right select
5	GND	Ground

3 General product characteristics

3.1 Electrical parameters and characteristics

3.1.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Storage temperature	T_S	-40	–	125	°C	
Supply voltage	V_{DD}	-0.3	–	4.0	V	
ESD robustness all pins (HBM)	V_{ESD_HBM}	-2	–	2	kV	according EIA/JESD22/A114

Attention: ***Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the section "Functional range" of this datasheet is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device.***
Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on VDD pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings.
Lifetime statements are an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. Lifetime statements shall in no event extend the agreed warranty period.

3.1.2 Functional range

The following functional range shall not be exceeded in order to ensure correct operation of the device. All parameters specified in the following sections refer to these operating conditions unless otherwise indicated.

Table 5 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.62	1.8	3.6	V	A 100nF bypass capacitor should be placed close to the microphone's VDD pin to ensure best SNR performance
Ambient operating temperature	T_A	-40	–	+105	°C	
VDD ramp-up Time	V_{DD_ru}	0.01	–	10	ms	Time until $V_{DD} \geq V_{DD_min}$
PDM Clock Frequency	f_{CLK}	0.45	–	5.2	MHz	Frequency response and performance can change with f_{CLK}

(table continues...)

Table 5 (continued) Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock Frequency Range - HPM	f_{CLK_HPM}	2.9	3.072	3.3	MHz	
Clock Frequency Range - Standby mode	f_{CLK_sb}	–	–	320	kHz	DATA = high-Z
Clock Duty Cycle	CLK_{duty}	45	–	55	%	
Clock Rise/Fall Time	t_{CR} / t_{CF}	–	–	13	ns	
Input Logic Low Level	V_{IL}	-0.3	–	$0.28xV_{DD}$	V	
Input Logic High Level	V_{IH}	$0.65xV_{DD}$	–	$V_{DD}+0.3$	V	
Hysteresis	V_{hys}	0.08	–	–	V	
Output Load Capacitance on DATA	C_{load}	–	–	200	pF	

4 Product features

4.1 Electrical characteristics

The values in the table "Electrical characteristics" are valid under the following conditions (unless otherwise specified in the table): V_{DD} = 1.8V ± 0.1V, T_A = 25°C ± 5°C

Table 6 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current Consumption - HPM	I_{DD_HPM}	–	1100	1400	µA	No load on DATA
Current Consumption - Standby mode	$I_{standby}$	–	1	5	µA	No load on DATA; CLK pulled to GND
Short Circuit Current	I_{short}	1	–	20	mA	Grounded DATA pin
Power Supply Rejection - Sine	PSR_{1k_NM}	–	-84	–	dBFS	100mV$_{pp}$ sine wave on V_{DD}, measurement at 1kHz
Power Supply Rejection - Square	PSR_{217_NM}	–	-84	–	dBFS(A)	100mVpp, 217Hz square wave on V_{DD}, A-weighted
Startup Time, ±0.5dB sensitivity accuracy	$t_{start\text{-}up}$	–	–	20	ms	Time to start up in all operating modes after V_{DD_min} and CLOCK have been applied
Startup Time, ±0.2dB sensitivity accuracy	$t_{start\text{-}up_HP}$	–	–	50	ms	Time to start up in all operating modes after V_{DD_min} and CLOCK have been applied
Mode Switch Time, ±0.5dB sensitivity accuracy	$t_{mode\text{-}switch}$	–	–	20	ms	Time to switch between operating modes. V_{DD} remains on during the mode switch
Mode Switch Time, ±0.2dB sensitivity accuracy	$t_{mode\text{-}switch_HP}$	–	–	50	ms	Time to switch between operating modes. V_{DD} remains on during the mode switch
Output Logic Low Level	V_{OL}	–	–	0.3xV_{DD}	V	I_{out} ≤ 2mA
Output Logic High Level	V_{OH}	0.7xV_{DD}	–	–	V	I_{out} ≤ 2mA
Delay Time for DATA Driven	t_{DD}	28	–	–	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA driven
Delay Time for DATA High-Z	t_{HZ}	14	–	26	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA high impedance state [1)]
Delay Time for DATA Valid	t_{DV}	–	–	100	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA valid (<0.3xV_{DD} or >0.7xV_{DD}) [2)]

1) t_{HZ} is dependent upon C_{load}

2) Load on DATA: C_{load} = 50pF, R_{load} = 100kΩ

4.1.1 Timing diagram

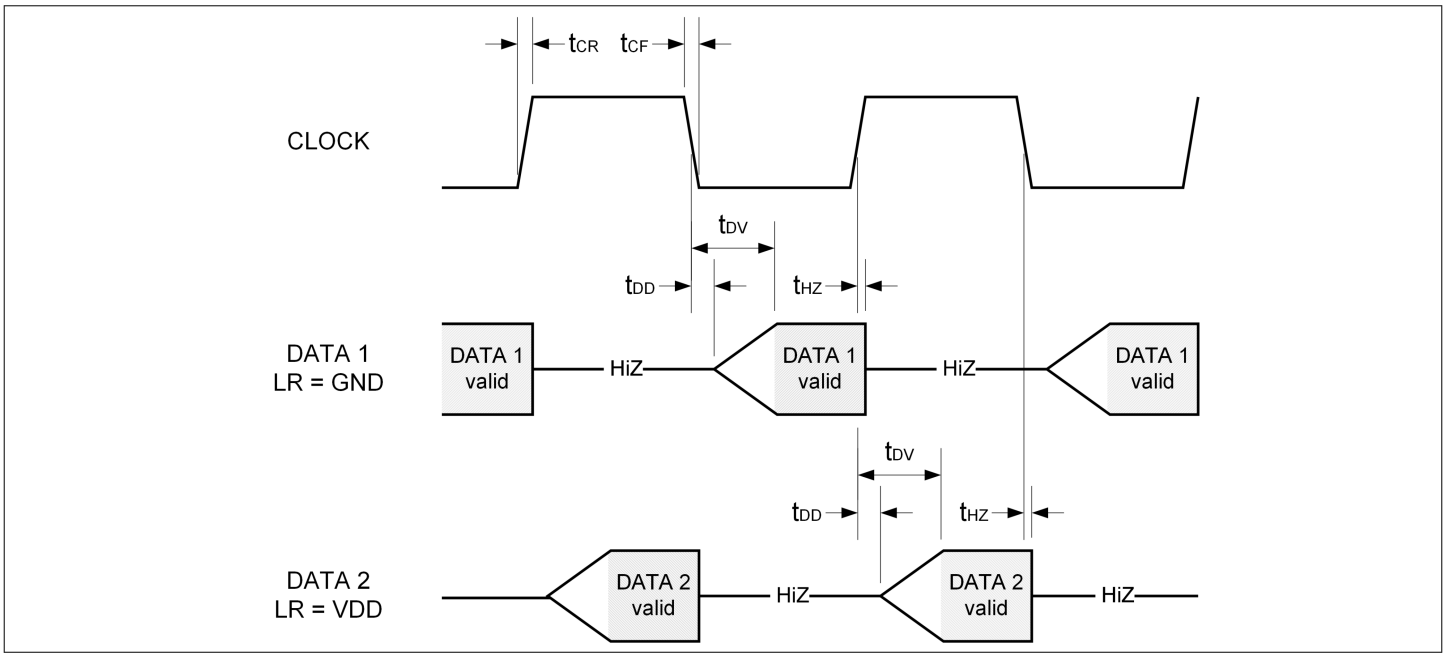


Figure 3 Timing diagram

4.2 Acoustic characteristics

The values in the table "Acoustic characteristics" are valid under the following conditions (unless otherwise specified in the table): V_{DD} = 1.8V ± 0.1V, T_A = 25°C ± 5°C, audio bandwidth 20Hz to 20kHz, output unloaded

The accoustic performance is dependant on the CLK frequency. All values in the table below are given for the typical CLK frequency of the mode.

Table 7 Acoustic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High performance mode (HPM)						
Sensitivity	$Sens_{HPM}$	-27	-26	-25	dBFS	1kHz, 94 dBSPL
Signal to noise ratio	SNR_{HPM}	–	66	–	dB(A)	A-Weighted
Equivalent input noise	EIN_{HPM}	–	28	–	dBSPL	A-Weighted
Total harmonic distortion, 94dBSPL	THD_{94_HPM}	–	0.1	–	%	Measuring 2nd to 5th harmonics; 1kHz
Total harmonic distortion, 1%	$THD_{1\%_HPM}$	–	114	–	dBSPL	Measuring 2nd to 5th harmonics; 1kHz
Acoustic overload point (10% THD)	AOP_{HPM}	–	120	–	dBSPL	Measuring 2nd to 5th harmonics; 1kHz

(table continues...)

Table 7 (continued) Acoustic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
All power modes						
Low frequency roll-off point	*LFRO*	–	7	–	Hz	-3dB point relative to 1kHz
Phase response, 100Hz	*Φ100*	–	5	–	°	
Phase response, 1kHz	Φ_{1000}	–	-4	–	°	
Phase response, 3kHz	Φ_{3000}	–	-13	–	°	
Group delay, 250Hz	t_{gd_250}	–	38	–	µs	
Group delay, 600Hz	t_{gd_600}	–	17	–	µs	
Group delay, 1kHz	t_{gd_1000}	–	14	–	µs	
Group delay, 4kHz	t_{gd_4000}	–	13	–	µs	

Polarity: The device has a positive polarity. Positive pressure increases density of 1's, negative pressure decreases density of 1's in data output.

Directivity: The device has an omnidirectional pickup pattern.

4.2.1 Free field frequency response

The figure below shows the typical free field response of the device.

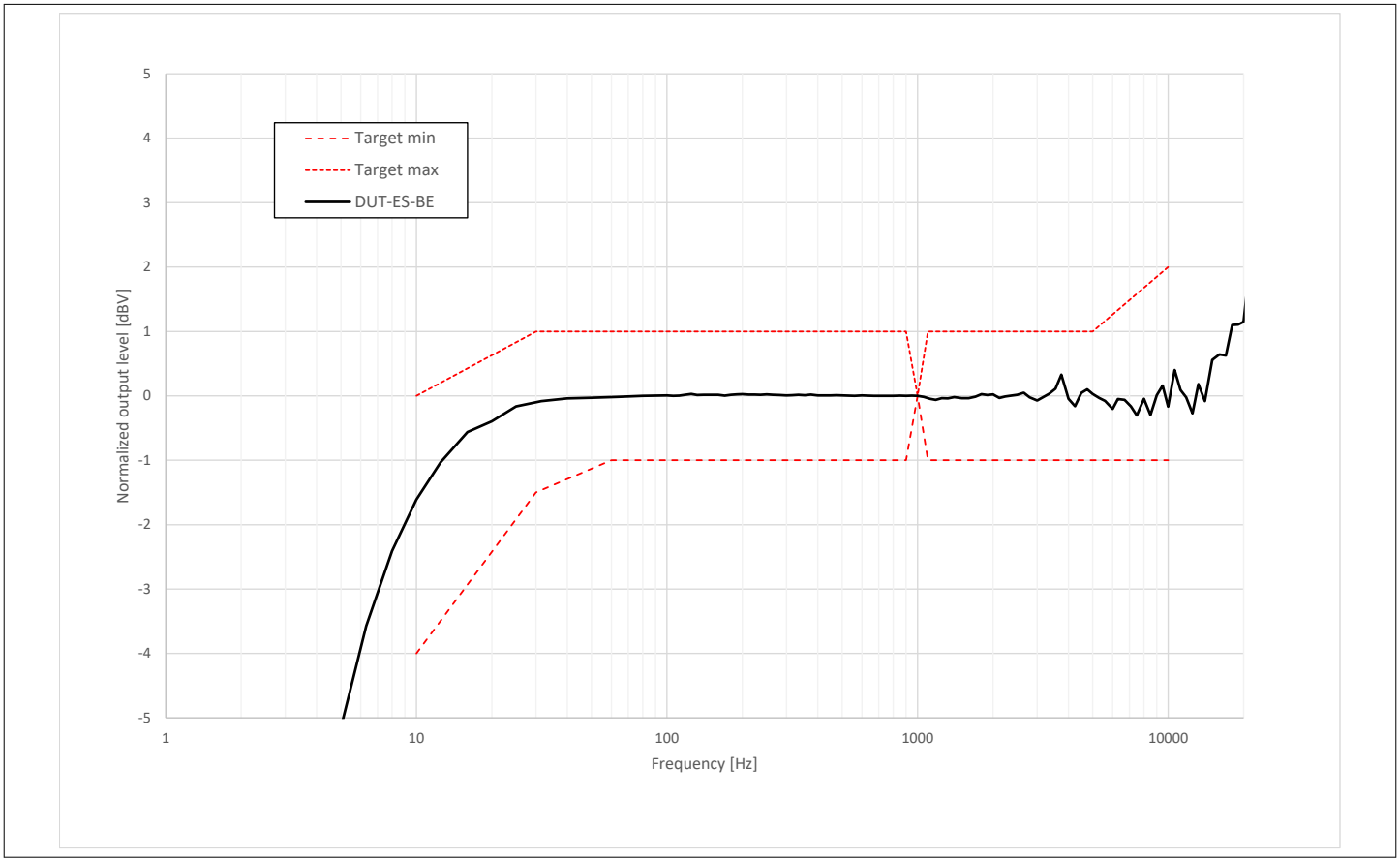


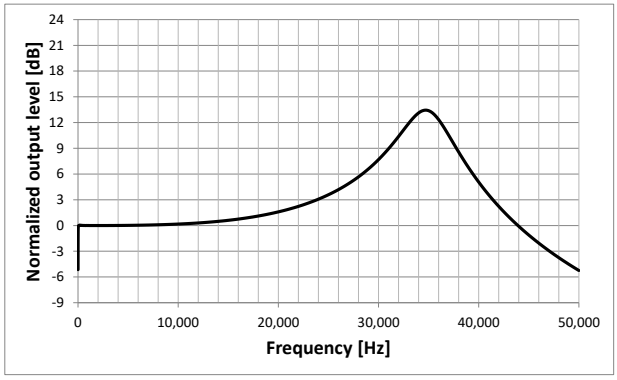
Figure 4 Free field frequency response

Table 8 Free field frequency response, normalized to 1kHz sensitivity value

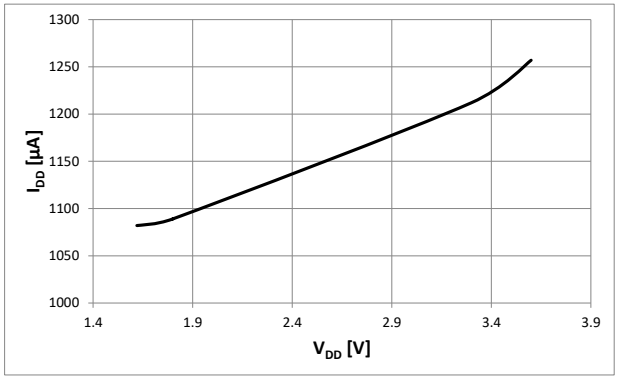
Frequency (Hz)	Lower limit (dB)	Upper limit (dB)
10	-4	0
30	-1.5	+1
60	-1	+1
100	-1	+1
1000	0	0
5000	-1	+1
10000	-1	+2

4.3 Typical performance characteristics

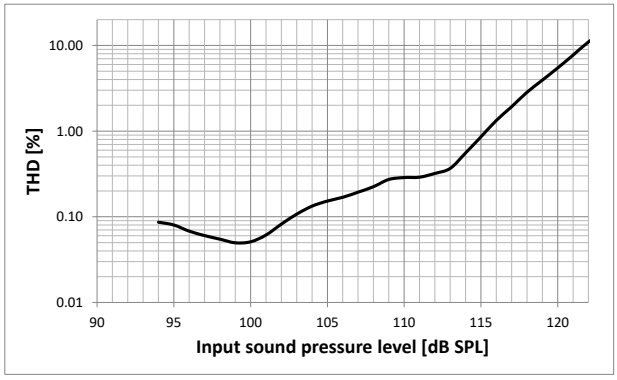
Conditions: V_{DD} = 1.8V ± 0.1V, T_A = 25°C ± 5°C, f_{CLK} = 3.072MHz, output unloaded



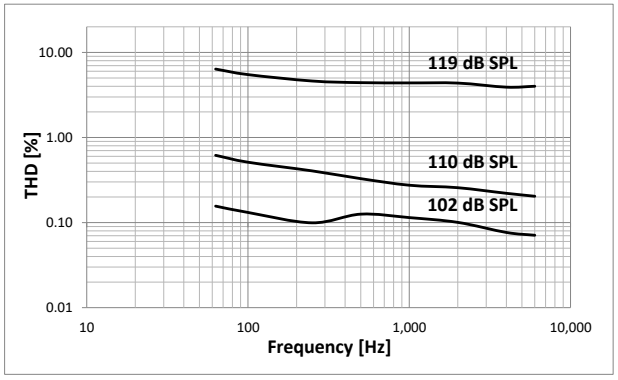
Plot 1: Typical free field response (ultrasonic)



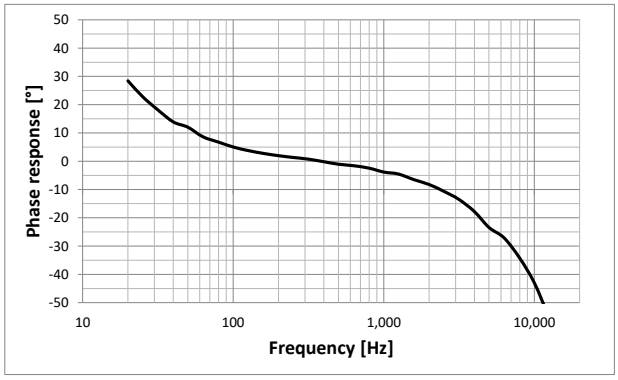
Plot 2: I_{DD} vs. V_{DD}



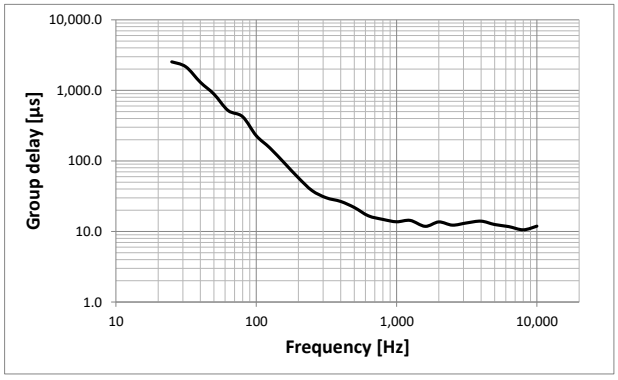
Plot 3: Typical THD vs. SPL @ 1kHz



Plot 4: Typical THD vs. frequency



Plot 5: Typical phase response vs. frequency



Plot 6: Typical group delay vs. frequency

Figure 5 Typical performance characteristics

5 Application information

***Note**: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

5.1 Use cases

- Flat frequency response with very low LFRO (low frequency roll off point) and small group delay
  - Best performance for active noise cancellation systems (ANC, RNC, ...)
  - Excellent speech quality over full frequency range
- Total harmonic distortion (THD) up to high sound pressure levels (SPL)
  - Clear speech in a wide dynamic range
  - Reliable voice commands even with high background noise
  - Improved ANC system performance in loud environments
- High acoustic overload point (AOP)
  - Distortion less output signal even in loud environments
- High signal to noise ratio (SNR)
  - Far field audio signal pick-up
  - Low volume audio and whispered voice capturing
  - Good performance with speech recognition algorithms
  - Microphone noise is no longer limiting the audio chain
- Close sensitivity and phase matching
  - Good performance in audio beamforming
  - High and precise attenuation of background noise
  - Full utilization of voice algorithms capability

5.2 Typical application circuit

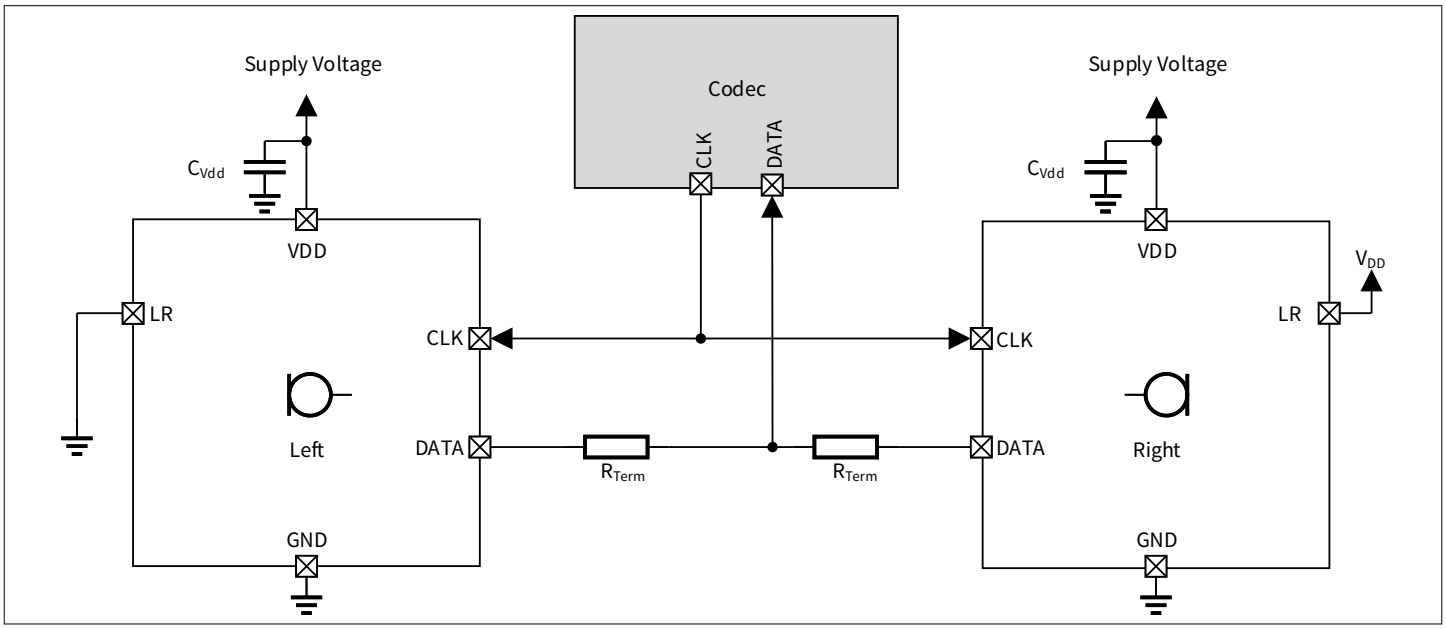


Figure 6 Typical application circuit

***Note**: For best performance it is strongly recommended to place a 100nF ($C_{VDD_typical}$) capacitor between VDD and ground. The capacitor should be placed as close to VDD as possible. A termination resistor (R_{TERM}) of about 100Ω may be added to reduce the ringing and overshoot on the output signal.*

***Note**: This figure is a simplified example of an application circuit. The function must be verified in the application.*

***Note**: When two microphones are connected to a shared PDM bus, it is strongly recommended to use the same clock signal and a common VDD supply to synchronize the power modes of both microphones.*

6 Package information

This product is compliant to RoHS

6.1 Package outline

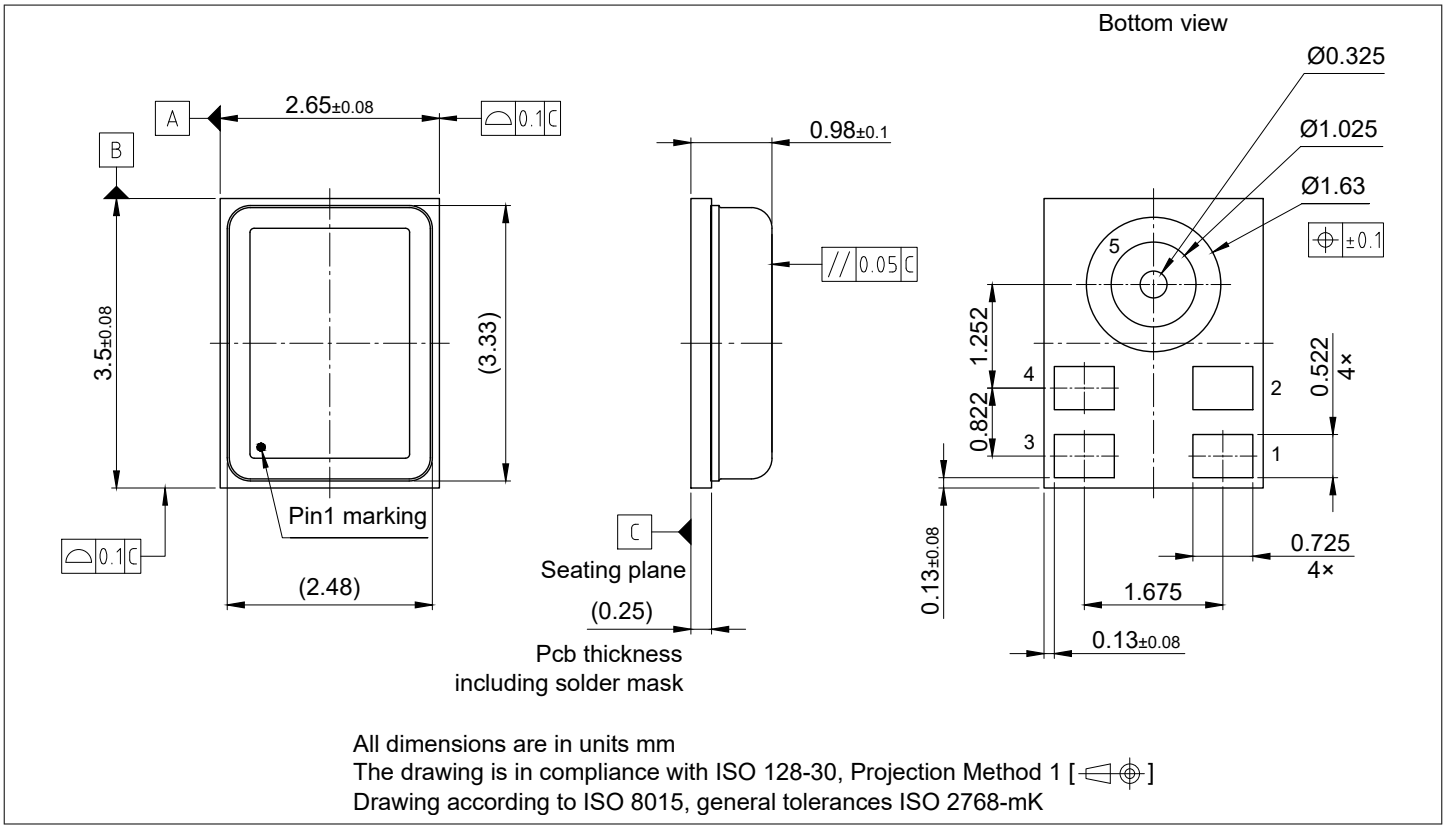


Figure 7 Package outline drawing

6.2 Footprint and stencil recommendation

The acoustic port hole diameter in the PCB should be larger than the acoustic port hole diameter of the MEMS microphone to ensure optimal performance. A PCB sound port size of radius 0.3 mm (diameter 0.6mm) is recommended.

The board pad and stencil aperture recommendations shown in the figure below are based on solder mask defined (SMD) pads. The specific design rules of the board manufacturer should be considered for individual design optimizations or adaptations.

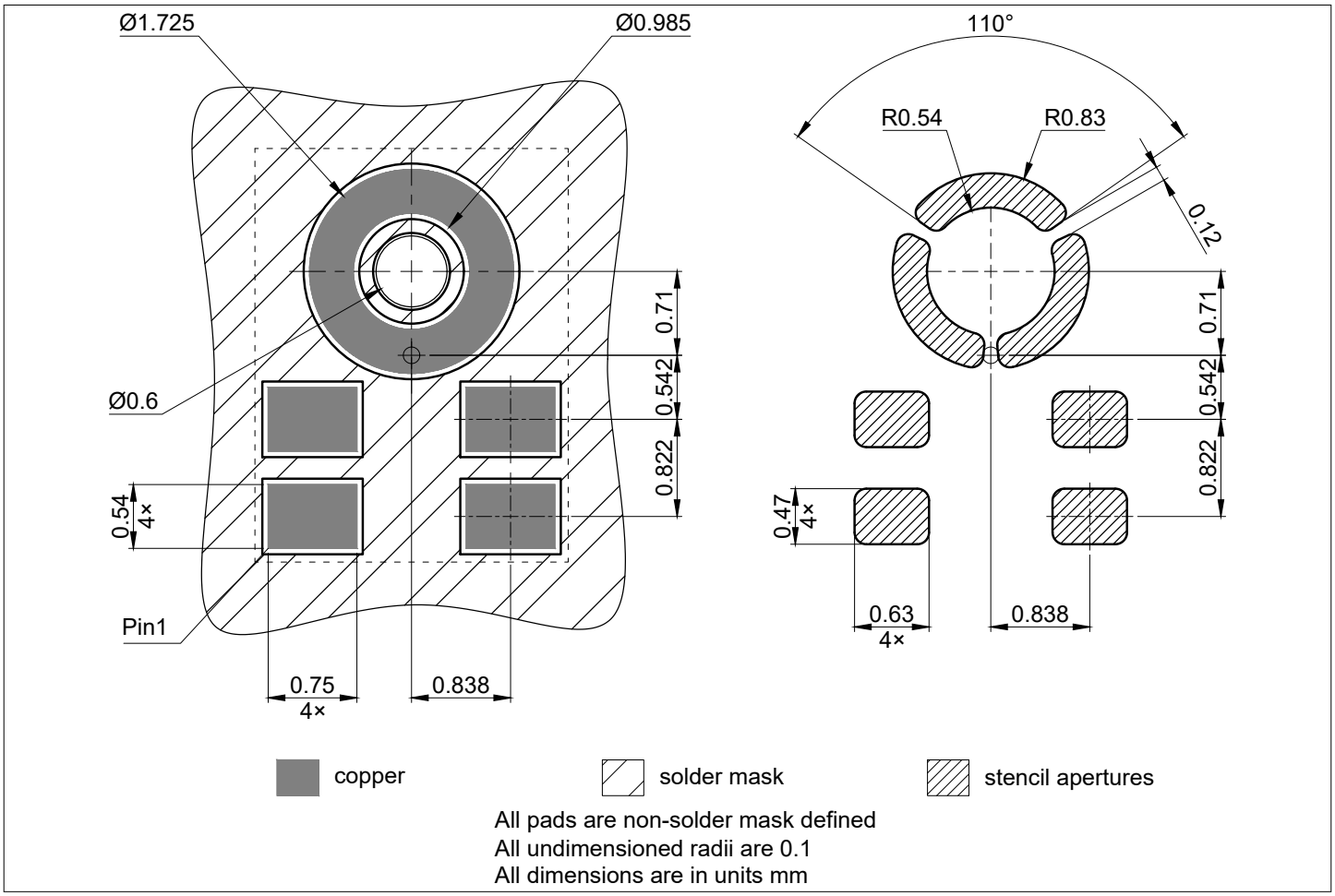


Figure 8 Foot print and stencil recommendation

6.3 Reflow soldering and board assembly

Infineon MEMS microphones are qualified in accordance with the IPC/JEDEC J-STD-020D-01. The moisture sensitivity level of MEMS microphones is rated as MSL1. For PCB assembly of the MEMS microphone the widely used reflow soldering, using a forced convection oven, is recommended.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to reach an optimal solder joint quality. The reflow profile shown in the figure below is recommended for board manufacturing with Infineon MEMS microphones.

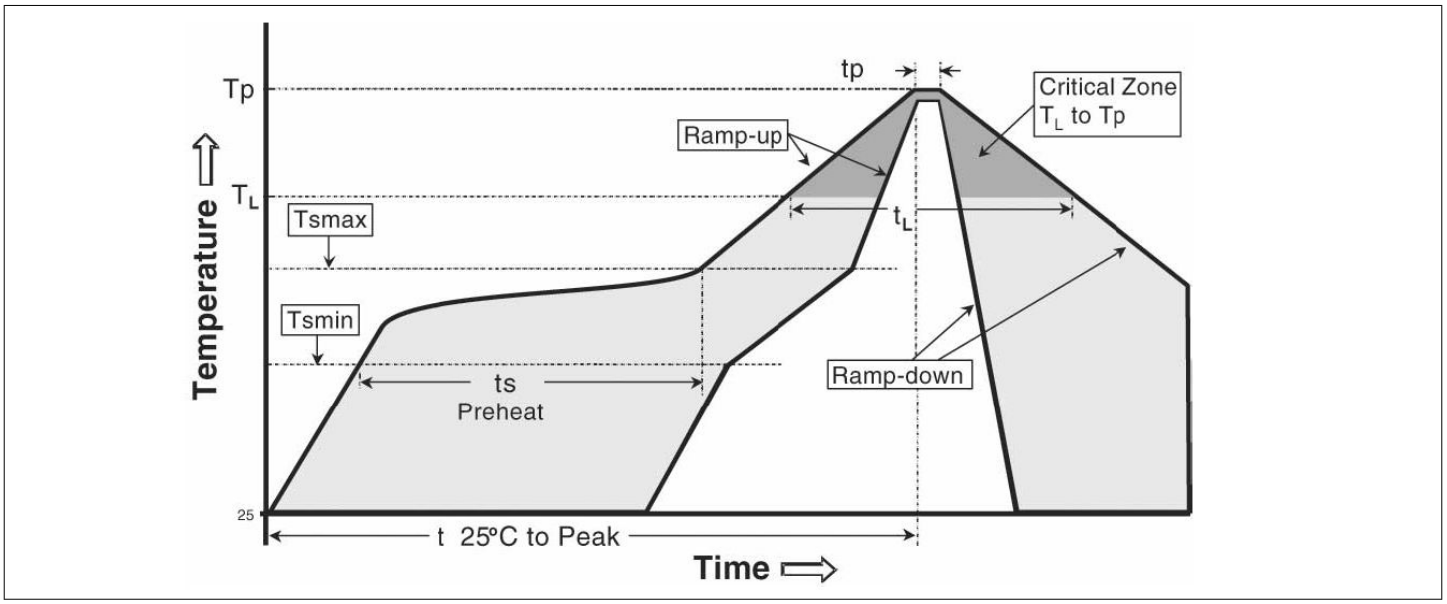


Figure 9 Recommended reflow profile

Table 9 Reflow profile limits

Profile feature	Symbol	Pb-free assembly	Sn-Pb Eutectic assembly
Preheat temperature min.	T_{smin}	150°C	100°C
Preheat temperature max.	T_{smax}	200°C	150°C
Preheat time (T_{smin} to T_{smax})	t_s	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)	–	3°C/second max.	3°C/second max.
Liquidous temperature	T_L	217°C	183°C
Time maintained above T_L	t_L	60-150 seconds	60-150 seconds
Peak temperature	T_P	260°C +0°C/-5°C	235°C +0°C/-5°C
Time within 5°C of actual peak temperature (see note below)	t_P	20-40 seconds	10-30 seconds
Ramp-down rate	–	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	t	8 minutes max.	6 minutes max.

***Note**: Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.*

The MEMS microphones can be handled using industry standard pick and place equipment. Care should be taken to avoid damage to the microphone structure as follows:

- Do not pick the microphone with vacuum tools which make contact with the microphone acoustic port hole.
- The microphone acoustic port hole should not be exposed to vacuum. This can destroy or damage the MEMS.
- Do not blow air into the microphone acoustic port hole. If an air blow cleaning process is used, the port hole must be sealed to prevent particle contamination.
- It is recommended to perform the PCB assembly in a clean room environment in order to avoid microphone contamination.
- Air blow and ultrasonic cleaning procedures shall not be applied to MEMS Microphones. A no-clean paste is recommended for the assembly to avoid subsequent cleaning steps. The microphone MEMS can be severely damaged by cleaning substances.
- To prevent the blocking or partial blocking of the sound port during PCB assembly, it is recommended to cover the sound port with protective tape during PCB sawing or system assembly.
- Do not use excessive force to place the microphone on the PCB. The use of industry standard pick and place tools is recommended in order to limit the mechanical force exerted on the package.

***Note**: For further information please consult the "General recommendation for assembly of Infineon packages" document, which is available on the Infineon Technologies web page.*

6.4 Packing

For shipping and assembly the Infineon microphones are packed in product specific tape-and-reel carriers. A detailed drawing of the carrier can be seen in the figure below.

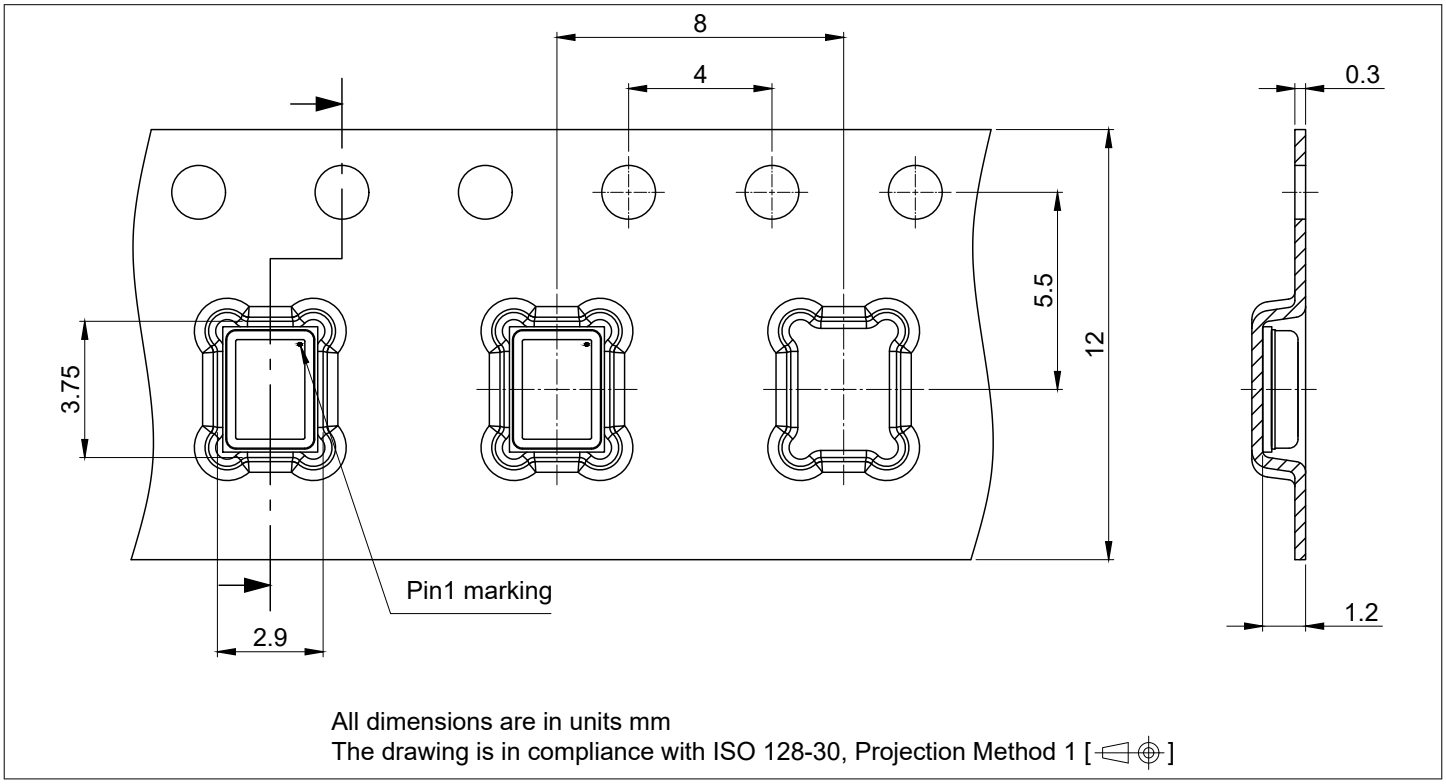


Figure 10 Tape dimensions

More information can be found on the Infineon website:
https://www.infineon.com/cms/en/product/packages/PG-TLGA/PG-TLGA-5-6/

7 Reliability specifications

The microphone sensitivity after stress and over temperature does not deviate by more than +/- 3dB from the initial value.

Table 10 Qualification tests according to AEC-Q103-003

Test	Stress condition	Standard
Temperature humidity bias (THB)	T_A = +85°C, R.H. = 85%, V_{DD} = 3.6V, cyclical bias, 1000 hours	JESD22-A101
Temperature humidity storage (THS)	T_A = +85°C, R.H = 85%, 1000 hours	JESD22-A101
Temperature cycling (TC)	T_A = -55°C ... +125°C, 30 min cycle time, 1000cycles	JESD22-A104
High temperature storage life (HTSL)	T_A = +125°C, 1000 hours	JESD22-A103
High temperature operating life (HTOL)	T_A = +125°C, V_{DD} = 3.6V, 1000 hours	JESD22-A108
Early life failure rate (ELFR)	T_A = +125°C, V_{DD} = 3.6V, 48 hours	AEC Q100-008
Mechanical shock (MS)	3 pulses, 0.2msec duration, 10,000g peak acceleration in x,y and z planes	JESD22-B104
Variable frequency vibration (VFV)	20Hz to 2kHz to 20Hz (logarithmic variation) in 12 minutes, 4x in each orientation, 20g peak acceleration	JESD22-B103
Package drop (DROP)	10x on each of 6 axes (60 drops total) from a height of 1.2m onto a concrete surface	AEC Q103-003
Humidity and temperature cycle (HTC)	5 cycles (24h/cycle)	AEC Q103-003, JESD22-A108, IEC 60068-2-38
Low temperature operating life (LTOL)	T_A = -40°C, V_{DD} = 3.6V, 1000 hours	JESD22-A108, IEC 60068-2-2, Test-AA
Low temperature storage (LTS)	T_A = -40°C, 1000 hours	JESD22-A108, IEC 60068-2-2, Test-AA
Endurance life test (ELT)	96 hours at 130dB continuous signal	AEC Q103-003
Maximum pressure test (MPT)	160 dBSPL	AEC Q103-003
Electrostatic discharge, Human body model (HBM)	all pins, V_{ESD} = ±2000V	AEC Q100-002
Electrostatic discharge, Charged device model (CDM)	all pins, V_{ESD} = ±500V	AEC Q100-011
Latch-up	T_A = 105°C, I = ±100mA	AEC Q100 Rev.H.
Electromagnetic compatibility (EMC)	IC strip line radiated emissions	SAE J1752/3 – Radiated Emissions

(table continues...)

Table 10 (continued) Qualification tests according to AEC-Q103-003

Test	Stress condition	Standard
Wire bond shear	–	AEC Q100-001, AEC Q003
Wire bond pull	–	MIL-STD-883, AEC Q003
Die shear	–	MIL-STD-883
Solderability	–	JESD22-B102
Physical dimensions	–	JESD22-B100 and B108, AEC Q003
Acoustic characterization	Measurement of acoustic parameters over full voltage and temperature range T_A = -40°C ... +105°C V_{DD} = 1.6 V ... 3.6 V	–

Table 11 Additional tests for use in automotive applications

Test	Stress condition	Standard
Electrostatic discharge, SLT - Contact discharge	3 contact discharges of ±6kV to lid while V_{DD} is supplied according to the operational modes; V_{DD} ground is separated from earth ground	IEC-61000-4-2
Electrostatic discharge, SLT - Air discharge	3 air discharges of ±8kV to lid while V_{DD} is supplied according to the operational modes; V_{DD} ground is separated from earth ground	IEC-61000-4-2
Environmental Robustness - IP57	Arizona dust A4 (ISO 12103-1) test and immersion in 1 meter of water for 30 minutes.	ISO-20653

8 Revision history

Table 12 Revision history

Document revision	Date of release	Description of changes
1.10	2024-05-17	• Update to the overall performance characteristics in Table 5 - Increased the maximum PDM clock frequency - Updated the min and max limits of the PDM clock frequency in High Performance Mode (HPM) • Update to the PSR sine and square test condition in Table 6 • Replaced the typical phase value at 75Hz with the typical phase value at 100Hz in Table 7 • Additional note on the stereo application in Chapter 5.2 • Update on the stress conditions in Table 10 • Addition of the IP57 stress test to Table 11 • Editorial changes
1.00	2023-11-17	• Initial release

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