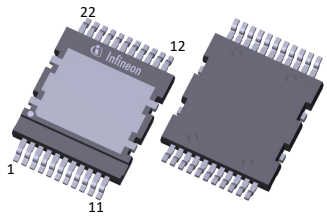
Silicon Carbide JFET

CoolSiC™ JFET 750 V J1 in QDPAK

PG-HDSOP-22



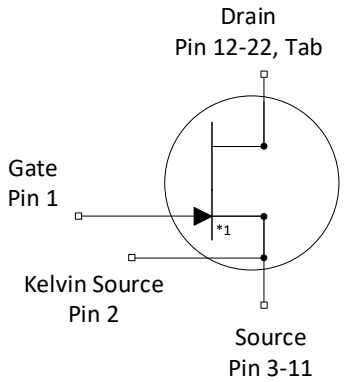
The CoolSiC™ junction-gate field-effect transistor (JFET) addresses the requirements of protection circuits in solid-state power distribution. It offers low on-state resistance and high ruggedness; additionally, the package enables fully automated assembly and flexible cooling path design.

Features

- Low on-state resistance $R_{DS(on)}$
- High-current avalanche ruggedness
- Surge current ruggedness
- Overload operation up to 200°C
- Compatible with automated assembly

Benefits

- Unique combination of high performance, high reliability and ease of use
- Ease of use and integration
- Higher robustness and system reliability
- Efficiency improvement
- Reduced system size leading to higher power density



**1: Internal gate diode*

Potential applications

- Solid-state circuit breaker
- Solid state relay
- Battery disconnect switch

Product validation

Qualified according to relevant JEDEC tests.

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS} over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	1.60	mΩ
I_{DM}	1769	A
i^2t	tbd	A^2s
I_{AS}	716	A

Hal Pb RoHS

Part number	Package	Marking	Related links
IJCQ75RM16J1	PG-HDSOP-22	75RM16J1	see Appendix A

Table of contents

1 Maximum ratings and recommendations

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 70% of the maximum rated V_{DS} stated in this datasheet. For applications with higher applied blocking voltage it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support by Infineon.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DS}	-	-	750	V	V_{GS} = -18 V, T_j = -55°C to 175°C
Continuous DC drain current [1]	I_{DDC}	-	-	628	A	T_c = 25°C, V_{GS} = 2 V
				499		T_c = 105°C, V_{GS} = 2 V
Peak drain current	I_{DM}	-	-	1769	A	T_c = 25°C, V_{GS} = 2 V, V_{DS} = 5 V, pulse width t_p limited by $T_{j,max}$
i^2t [2]	$\int i^2\,dt$	-	-	tbd	A^2s	V_{GS} = 2 V, T_j = 25°C, t_p = 10 ms (sine half wave)
						V_{GS} = 2 V, T_j = 25°C, t_p = 30 µs (rectangular)
Avalanche energy, single pulse [3]	E_{AS}	-	-	256	mJ	I_D = 716 A, V_{GS} = -18 V, L = 1 µH, T_j = 25°C
Avalanche current, single pulse	I_{AS}	-	-	716	A	V_{DD} = 100 V, V_{GS} = -18 V, L = 1 µH, T_j = 25°C
JFET dv/dt ruggedness [2]	dv/dt	-	-	20	V/ns	V_{DS} = 0...400 V
Gate-source voltage	V_{GS}	-20	-	2.2	V	static
		-30		10		I_{GF} = tbd A, transient
Power dissipation	P_{tot}	-	-	2419	W	T_c = 25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		
Operating junction temperature extended	$T_{j,ext}$	-	-	200	°C	Overload; cumulative max. 100 h and max. 5000 cycles with $\Delta T \leq$ 100 K

1) Limited by $T_{j,max}$.
2) Not subject to production test. Parameter verified by design/characterization.
3) It is always recommended to use an external clamping element (e.g. MOV).

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	0	2	-	V	Turn-on
		-	-18			Turn-off
Drain-source voltage	V_{DS}	-	-	525	V	-

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case [4]	$R_{th(j-c)}$	-	0.044	0.062	K/W	-
Soldering temperature	T_{sold}	-	-	260	°C	Reflow soldering (MSL1 according to JEDEC J-STD-020)

[4] Not subject to production test. Parameter verified by design.

3 Electrical characteristics

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage [5]	$V_{(BR)DSX}$	775	-	-	V	V_{GS} = -18 V, I_D = 5.55 mA, T_j = 25°C
Gate-source threshold voltage	$V_{GS(th)}$	-7	-5.3	-3	V	V_{DS} = 1 V; I_D = 8.3 mA, T_j = 25°C
		-8.6	-7	-4.4		V_{DS} = 525 V; I_D = 8.3 mA, T_j = 25°C
Drain cut-off current	$I_{D(off)}$	-	3.24	305	µA	V_{DS} = 750 V, V_{GS} = -18 V, T_j = 25°C
			15.1	-		V_{DS} = 750 V, V_{GS} = -18 V, T_j = 175°C
			0.2	6.1		V_{DS} = 525 V, V_{GS} = -18 V, T_j = 25°C
			0.76	-		V_{DS} = 525 V, V_{GS} = -18 V, T_j = 175°C
Reverse gate current	I_{GSS}	-	0.17	18.4	µA	V_{GS} = -18 V, T_j = 25°C
			1.72	-		V_{GS} = -18 V, T_j = 175°C
Forward gate current	I_{GF}	-	48	-	µA	V_{GS} = 2 V, T_j = 25°C
Drain-source on-state resistance	$R_{DS(on)}$	-	1.80	-	mΩ	V_{GS} = 0 V, I_D = 55.0 A, T_j = 25°C
			1.60	-		V_{GS} = 2 V, I_D = 55.0 A, T_j = 25°C
			2.70	-		V_{GS} = 0 V, I_D = 55.0 A, T_j = 105°C
			2.39	-		V_{GS} = 2 V, I_D = 55.0 A, T_j = 105°C
			3.47	4.51		V_{GS} = 0 V, I_D = 55.0 A, T_j = 150°C
			3.01	3.92		V_{GS} = 2 V, I_D = 55.0 A, T_j = 150°C
Internal gate resistance	$R_{G,int}$	-	0.4	-	Ω	f = 1 MHz

[5] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

Table 6 Dynamic characteristics

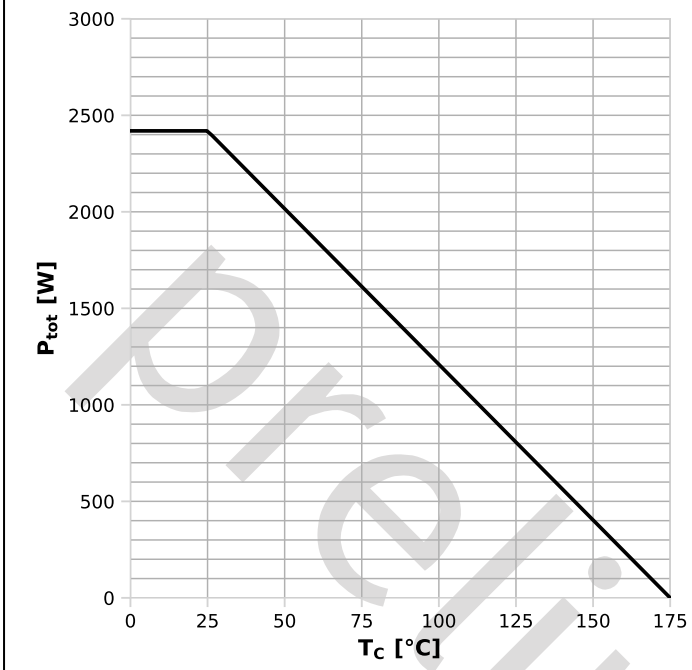
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	10100	-	pF	V_{GS} = -18 V, V_{DS} = 525 V, f = 250 kHz, T_j = 25°C
Reverse transfer capacitance	C_{rss}		890			
Output capacitance	C_{oss}		903			
Turn-on delay time	$t_{d(on)}$	-	tbd	-	ns	V_{DD} = 525 V, V_{GS} = -18/2 V, I_D = 55 A, $R_{G,ext}$ = 1.8 Ω, T_j = 25°C; tested in double pulse setup with SiC Diode for free wheeling phase
Rise time	t_r				ns	
Turn-off delay time	$t_{d(off)}$				ns	
Fall time	t_f				ns	
Turn-ON switching losses	E_{on}				µJ	
Turn-OFF switching losses	E_{off}				µJ	
Total switching losses	E_{tot}				µJ	

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source charge below plateau	$Q_{GS(pl)}$	-	133	-	nC	V_{DD} = 525 V, I_D = 55.0 A, V_{GS} = -18/2 V, T_j = 25°C
Gate-drain charge	Q_{GD}		749			
Total gate charge	Q_G		1341			

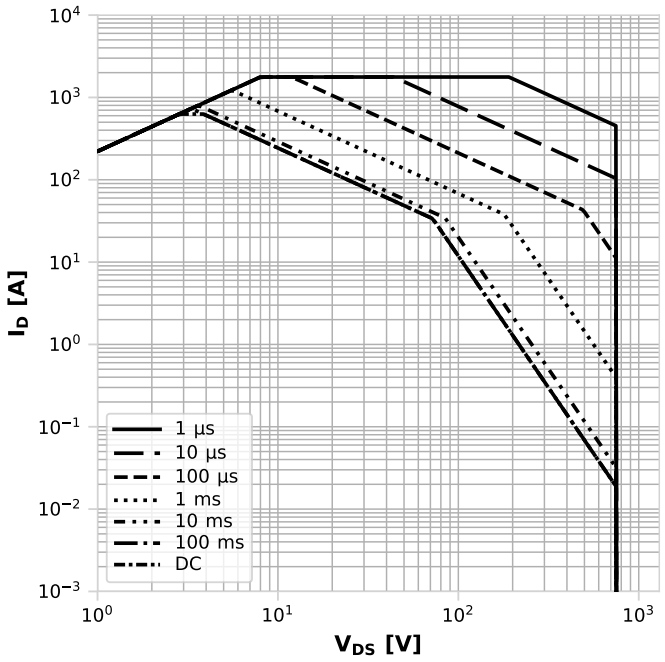
4 Electrical characteristics diagrams

Diagram 1: Max. power dissipation



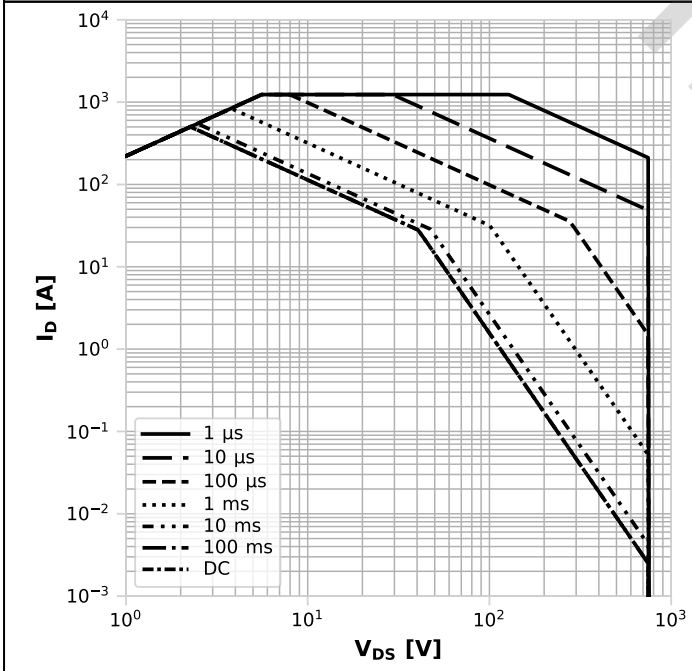
P_{tot}=f(T_C)

Diagram 2: Max. Safe operating area



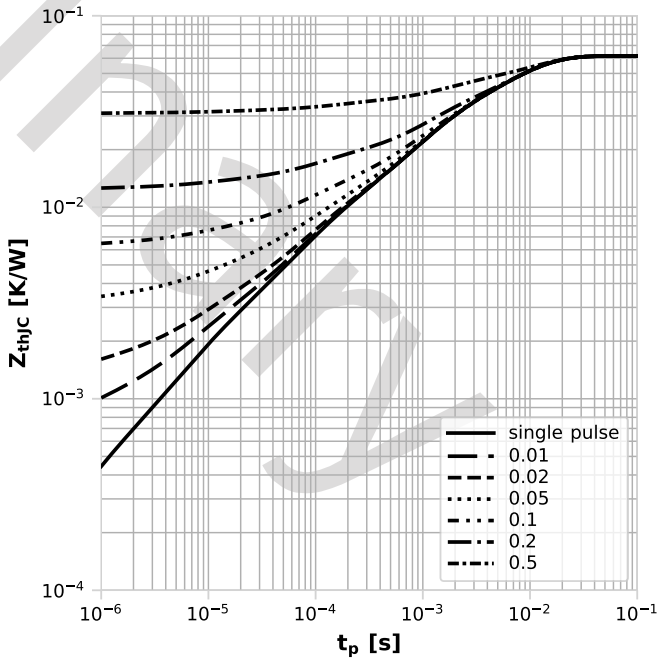
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Max. Safe operating area



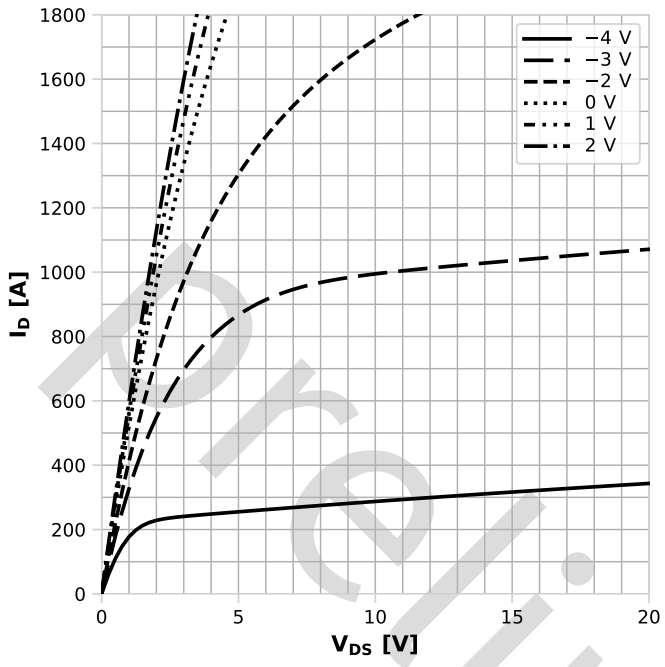
I_D=f(V_{DS}); T_C=105 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



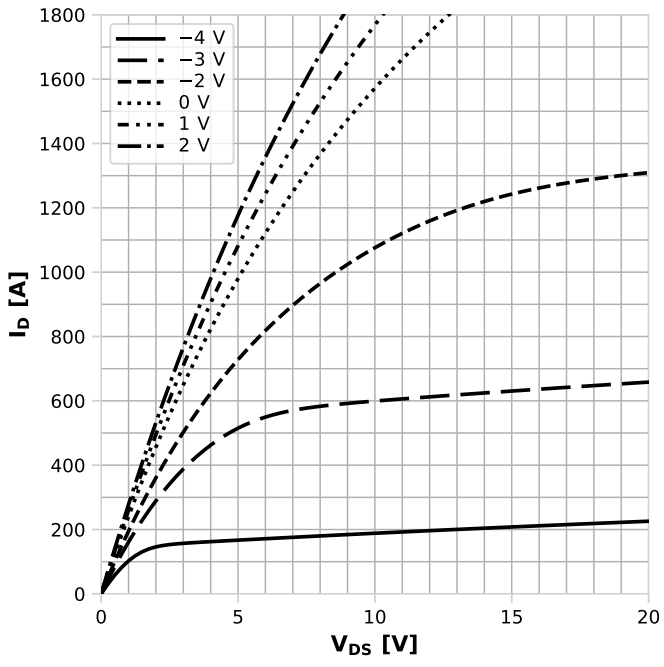
Z_{thJC} =f(t_P); parameter: D= t_p/T

Diagram 5: Typ. output characteristics



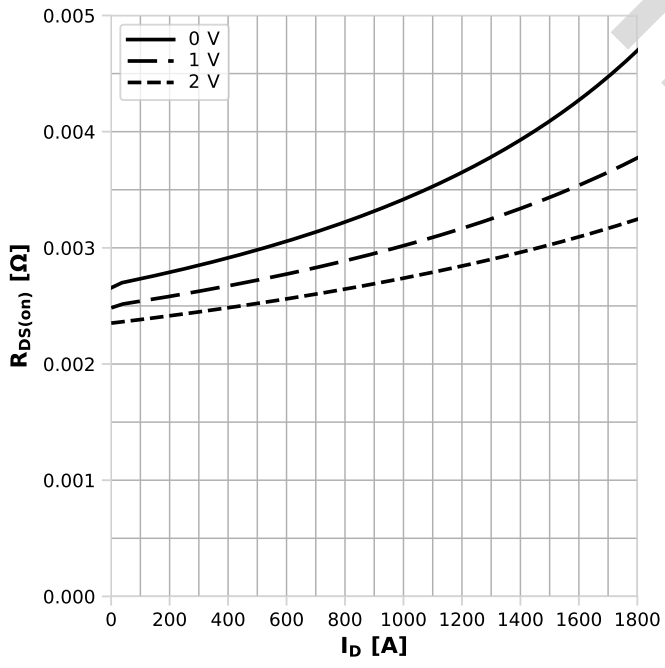
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



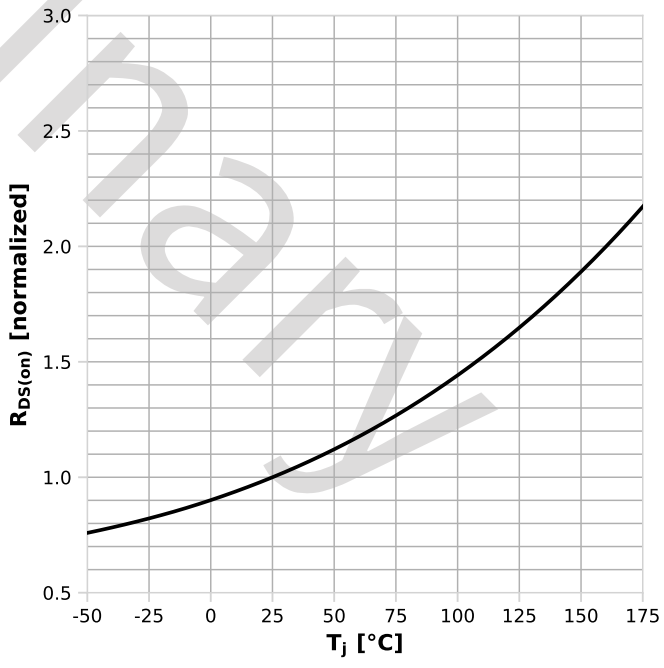
I_D=f(V_{DS}); T_j=175 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



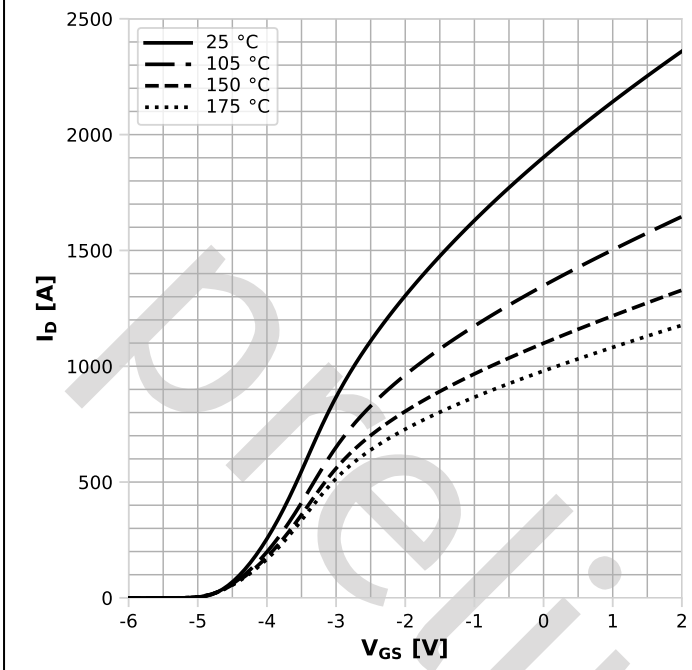
$R_{DS(on)}$=f(I_D); T_j=105 °C; parameter: V_{GS}

Diagram 8: Typ. drain-source on-state resistance



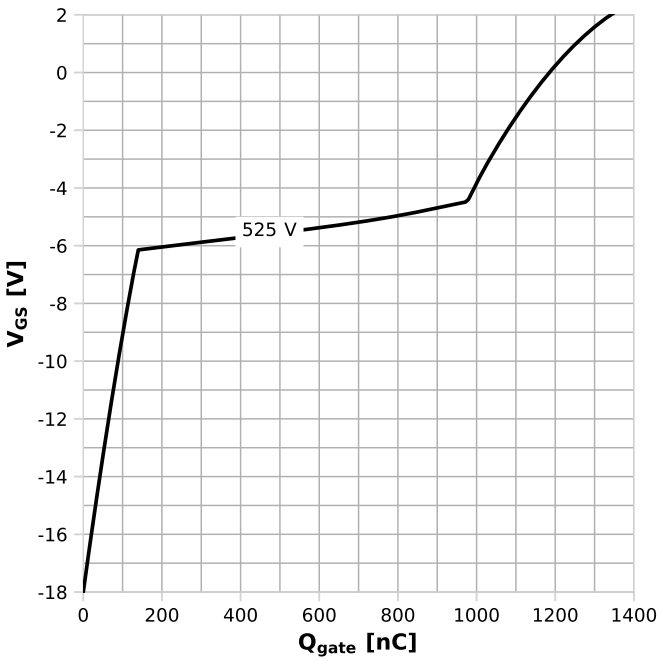
$R_{DS(on)}$=f(T_j); I_D=55.0 A; V_{GS}=2 V

Diagram 9: Typ. transfer characteristics



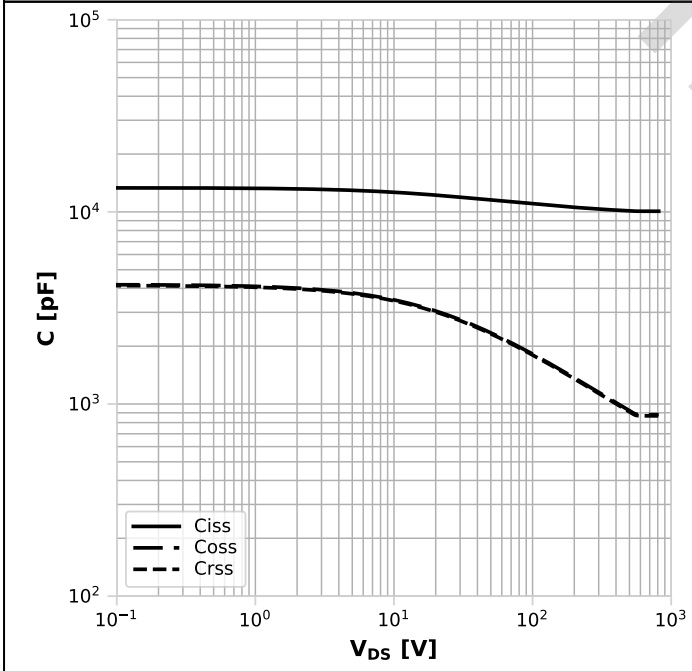
I_D=f(V_{GS}); V_{DS}=5 V; parameter: T_j

Diagram 10: Typ. gate charge



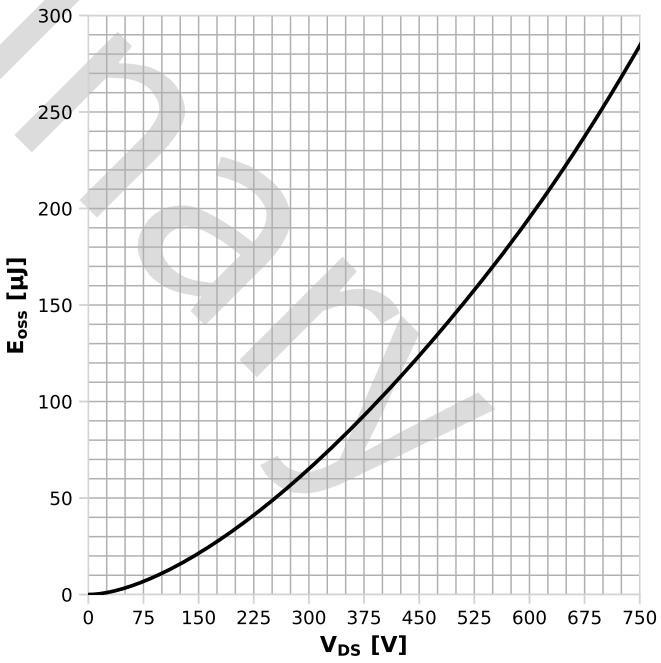
V_{GS}=f(Q_{gate}); I_D=55.0 A pulsed; V_{dr}=-18 V; parameter: V_{DD}

Diagram 11: Typ. capacitances AC

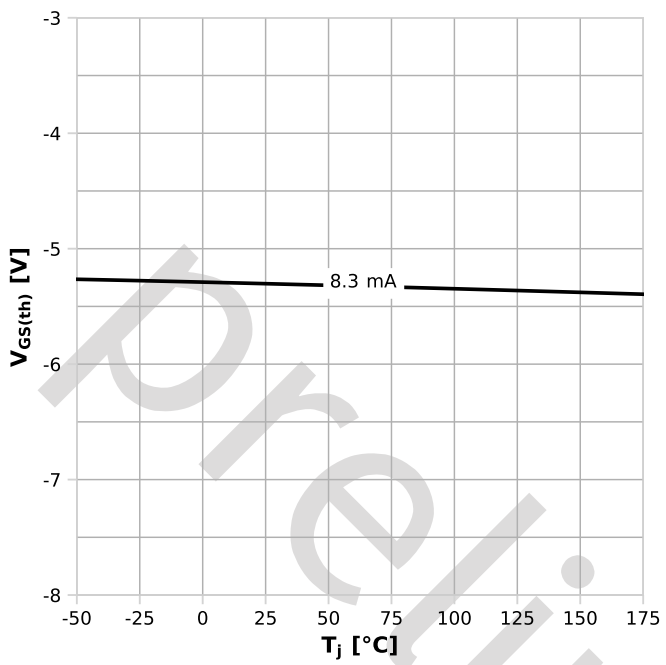
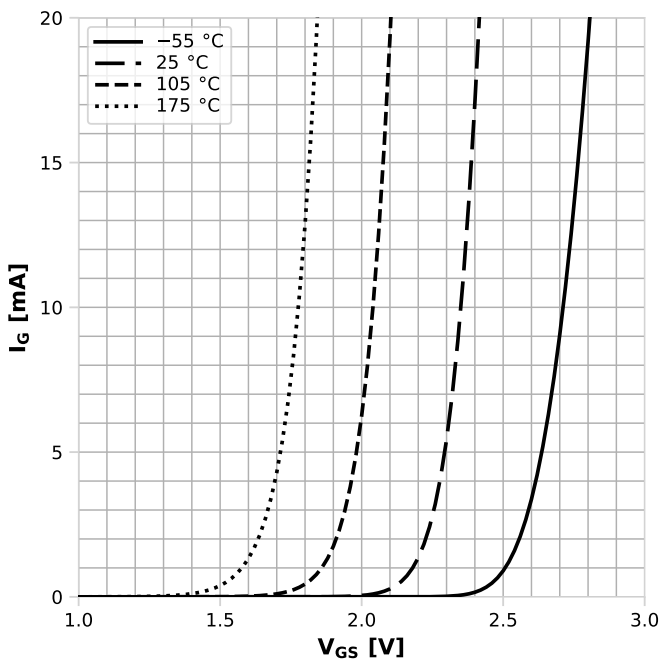


C=f(V_{DS}); V_{GS}=-18 V; f=250 kHz

Diagram 12: Typ. Coss stored energy AC



E_{oss}=f(V_{DS}); V_{GS}=-18 V

Diagram 15: Typ. gate threshold voltage	Diagram 16: Typ. transfer gate forward current
	
$V_{GS(th)}$=f(T_j), V_{DS}=1 V; parameter: I_D	I_G=f(V_{GS}); V_{DS}=0 V; parameter: T_j

5 Test circuits

Table 8 Switching times

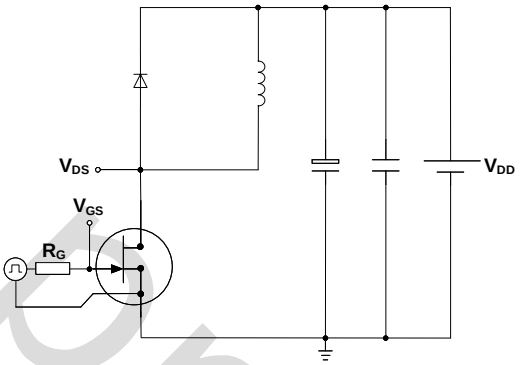
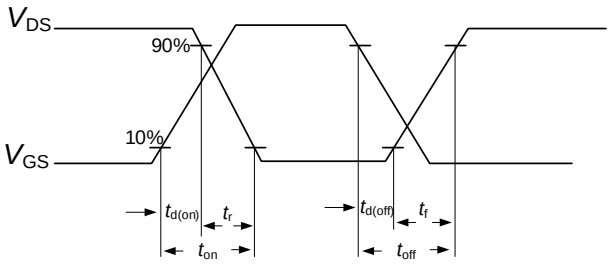
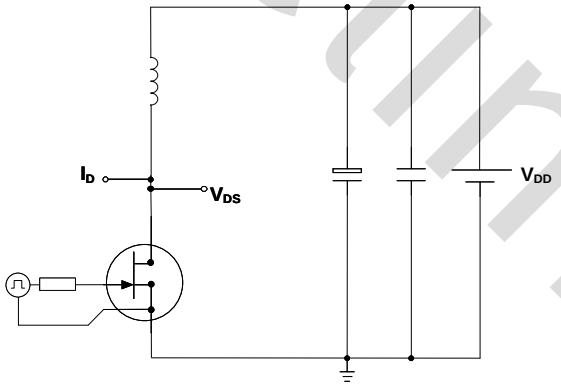
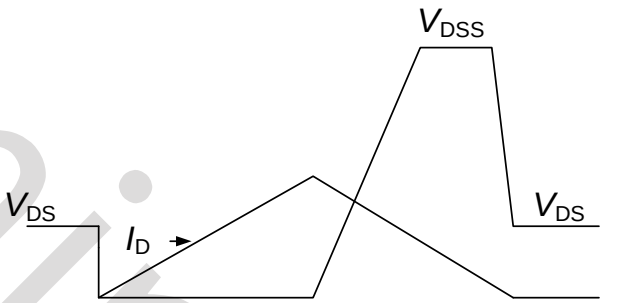
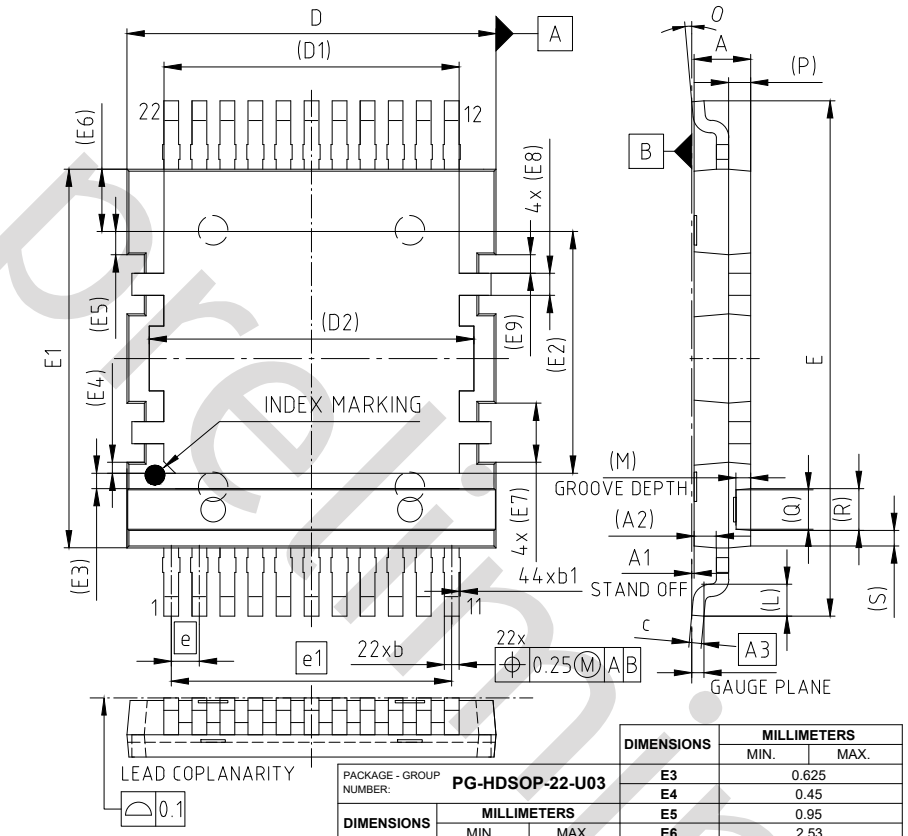
Switching times test circuit for inductive load	Switching times waveform
	

Table 9 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



NOTES:

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER: PG-HDSOP-22-U03

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.90	
A3	0.50	
b	0.50	0.70
b1	---	0.15
c	0.46	0.58
D	14.90	15.10
D1	12.00	
D2	13.20	
E	20.81	21.11
E1	15.30	15.50
E2	9.83	

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
E3	0.625	
E4	0.45	
E5	0.95	
E6	2.53	
E7	2.40	
E8	0.90	
E9	0.75	
e	1.14	
e1	11.4	
L	1.30	
M	0.60	
N	22	
O	0°	8°
P	0.90	
Q	1.60	
R	1.70	
S	0.631	

Figure 1 Outline PG-HDSOP-22, dimensions in mm

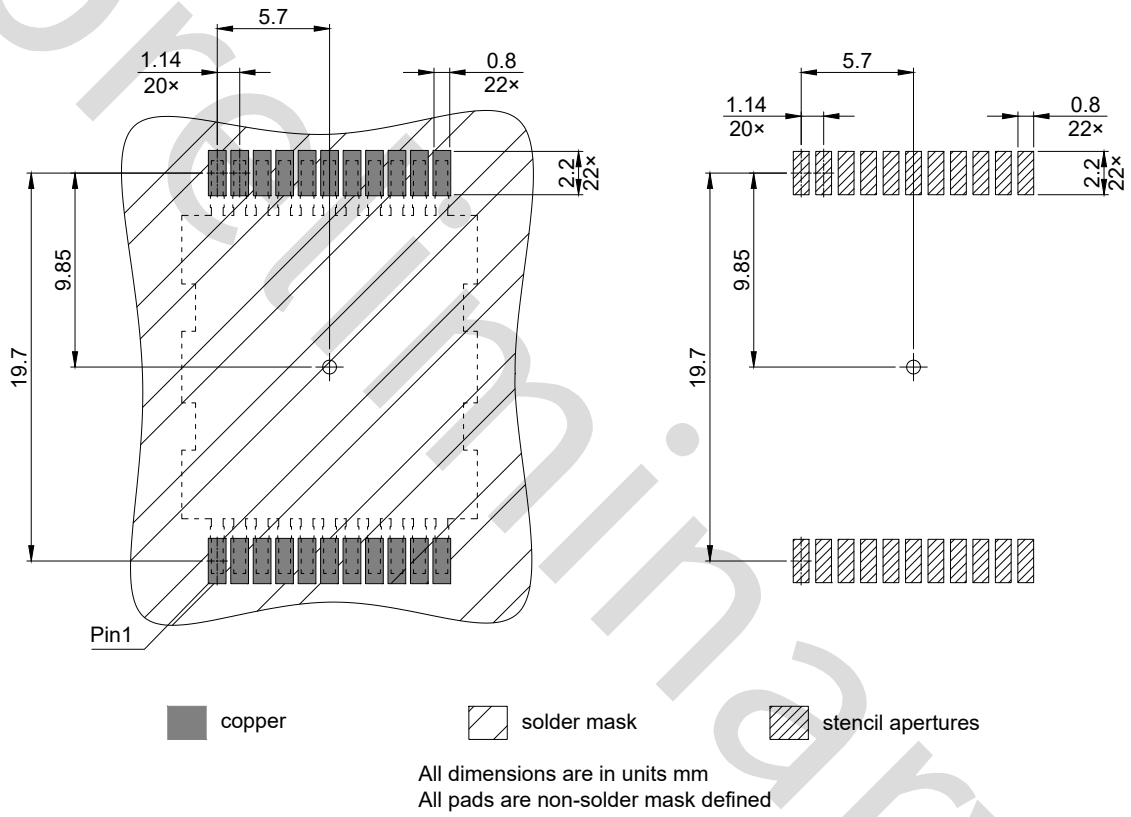


Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm

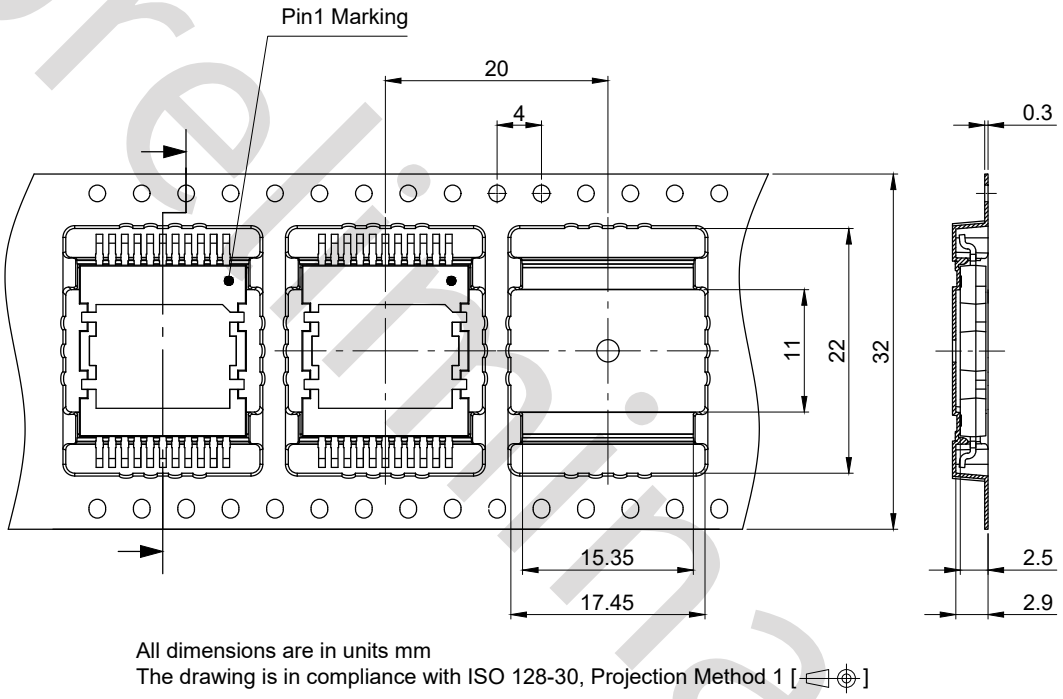


Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

7 Appendix A

Table 10 Related links

- IFX CoolSiC™ JFET 750 V J1 Webpage
- IFX CoolSiC™ JFET 750 V J1 Application Note
- IFX CoolSiC™ JFET 750 V J1 Simulation Model
- IFX Design tools

Revision history

IJCQ75RM16J1

Revision 2026-05-21, Rev. 0.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
0.1	2026-05-21	Release of preliminary version

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