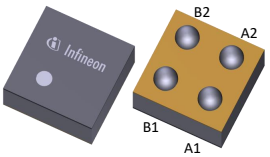
CoolGaN™

SG-UFWLB-4

CoolGaN™ Transistor 100 V G3

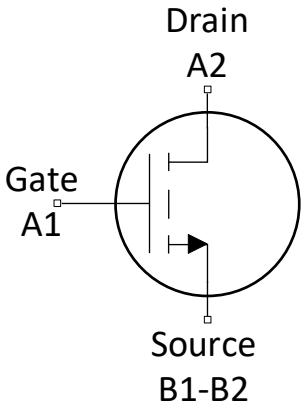


Features

- Ultra fast switching and high efficiency
- Low reverse conduction voltage
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade package

Potential applications

- DC-DC converters
- Wireless charging
- LiDAR
- Class-D audio



Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	185	mΩ
I_D	2.2	A
Q_{oss}	0.7	nC
Q_G	0.20	nC
Q_{rr}	0	nC
V_{SD}	2.3	V

GaN Hal Pb RoHS

Part number	Package	Marking	Related links
IGKA23S101S	SG-UFWLB-4	A23	see Appendix A

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1 Maximum ratings

at T_j = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	V_{GS}=0 V
Pulsed drain-source voltage [1]	$V_{DS,pulse}$	-	-	120	V	V_{GS}=0 V, 1 h total time
Continuous drain current	I_D	-	-	2.2	A	V_{GS}=5 V, T_C=25 °C
				1.5		V_{GS}=5 V, T_A=25 °C, R_{thJA}=115 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	9.0	A	T_j=25 °C
				5.0		T_j=125 °C
Pulsed gate-source voltage	V_{GS}	-6.5	-	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	2.2	W	T_c=25 °C
				1.0		T_A=25 °C, R_{thJA}=115 °C/W [2]
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating temperature	T_j	-40				

[1] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

[2] Device on 4-layer FR4 PCB, vertical in still air.

[3] Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	13	16	°C/W	-
Thermal resistance, junction - case, bottom			38	60		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	140	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	115	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical characteristics

at T_j=25 °C, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	2.1	2.9	V	V_{DS}=V_{GS}, I_D= 1 mA
Drain-source leakage current	I_{DSS}	-	0.02	0.1	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
			0.15	4		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	0.30	4.6	µA	V_{GS}=5 V, T_j=25 °C
			0.01	0.45		V_{GS}=-4 V, T_j=25 °C
			3.0	50		V_{GS}=5 V, T_j=125 °C
			0.01	0.45		V_{GS}=-4 V, T_j=125 °C
Drain-source on-state resistance	$R_{DS(on)}$	-	185	230	mΩ	V_{GS}=5 V, I_D=0.3 A
Gate resistance [4)]	R_G	-	4.0	-	Ω	-

4) Defined by design. Not subject to production test.

Table 6 Capacitance characteristics [5)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	18	-	pF	V_{GS}=0 V, V_{DS}= 50 V, f=1 MHz
Output capacitance	C_{oss}		10			
Reverse transfer capacitance	C_{rss}		0.38			

5) Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.08	-	nC	V_{DS}= 50 V, I_D= 0.3 A, V_{GS}=0 to 5 V
Gate charge at threshold	$Q_{g(th)}$		0.05		nC	
Gate charge [6)]	Q_{gd}		0.03		nC	
Switching charge	Q_{sw}		0.06		nC	
Gate charge total [6)]	Q_g		0.20		nC	
Gate plateau voltage	$V_{plateau}$		2.6		V	
Output charge [6)]	Q_{oss}	-	0.7	-	nC	V_{DS}= 50 V, V_{GS}=0 V

6) Defined by design. Not subject to production test.

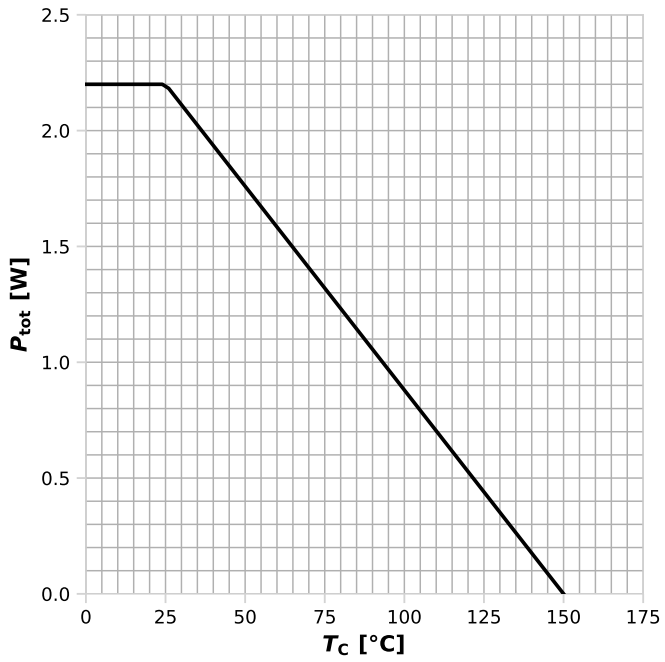
Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	1.0	A	T_C=25 °C
Pulsed current, reverse	$I_{S,pulse}$			9.0		
Source-drain reverse voltage	V_{SD}	-	2.2	-	V	V_{GS}=0 V, I_{spulse}=0.3 A, T_j=25 °C
			2.3			V_{GS}=0 V, I_{spulse}=0.5 A, T_j=25 °C
Reverse recovery charge [7)]	Q_{rr}	-	0	-	nC	V_R=50 V, $I_{S,pulse}$= 0.3 A, $di_{s,pulse}/dt$ =100 A/us

7) Defined by design. Not subject to production test.

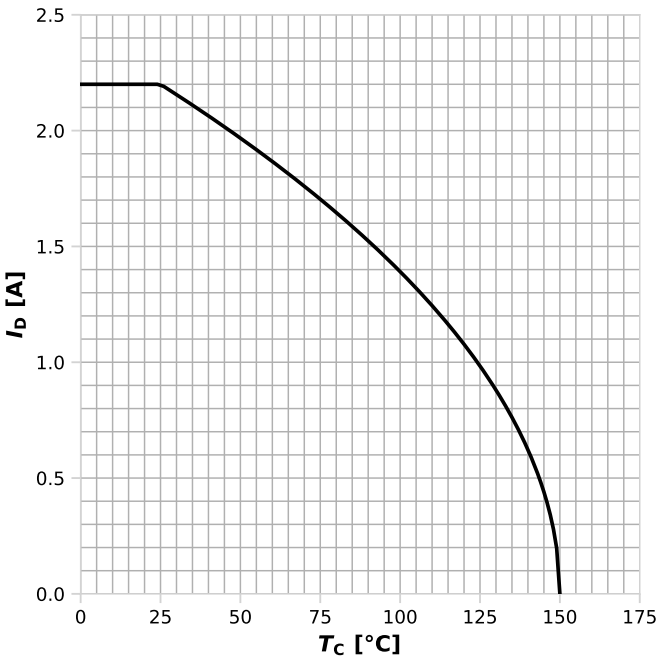
5 Electrical characteristics diagrams

Diagram 1: Power Dissipation



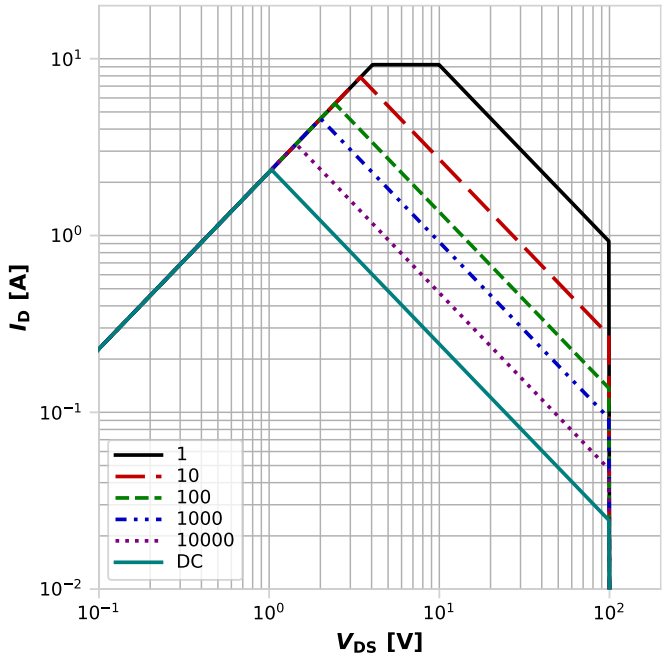
P_{tot}=f(T_C)

Diagram 2: Drain Current



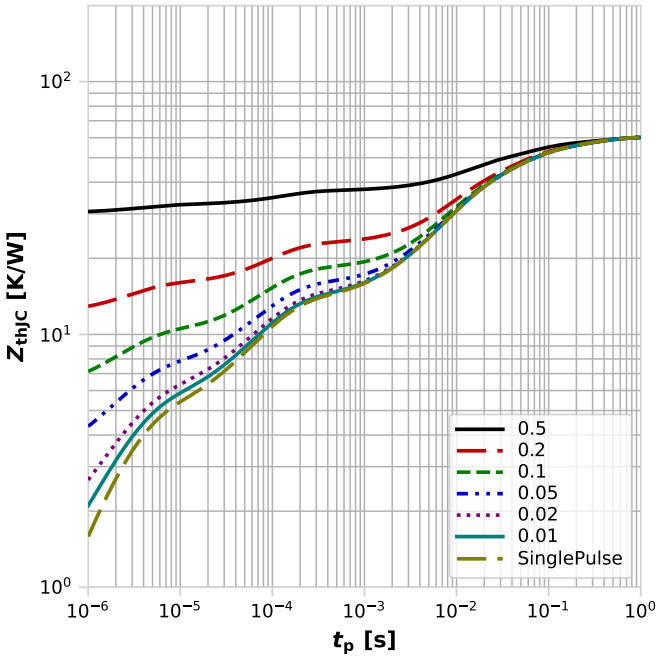
I_D=f(T_C)

Diagram 3: Safe Operating Area



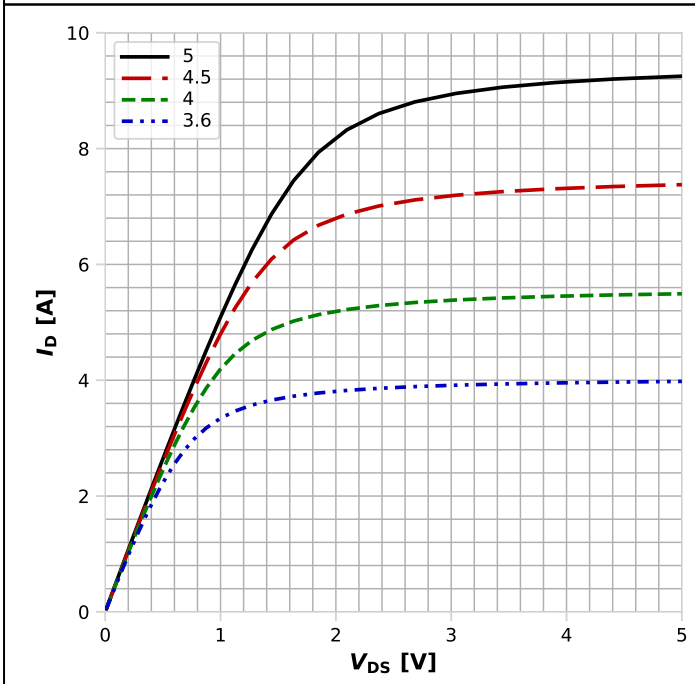
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p *[us]*

Diagram 4: Max. transient thermal impedance



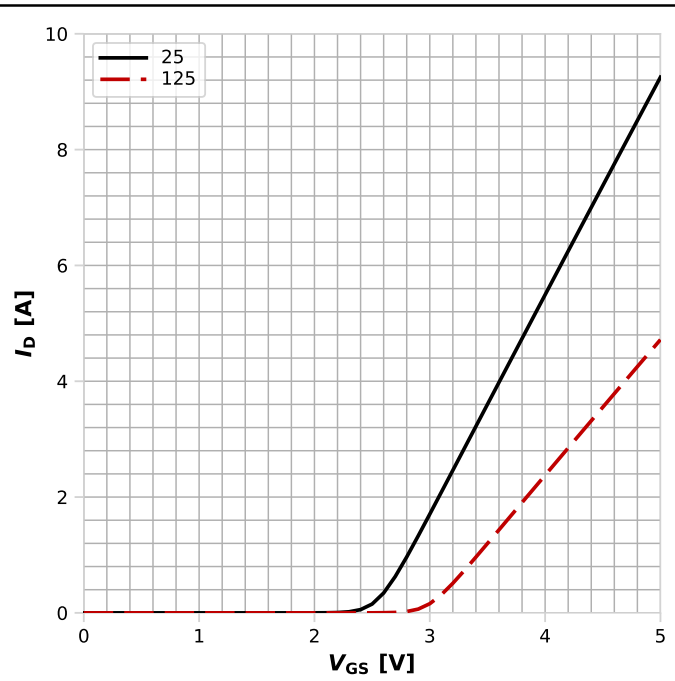
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



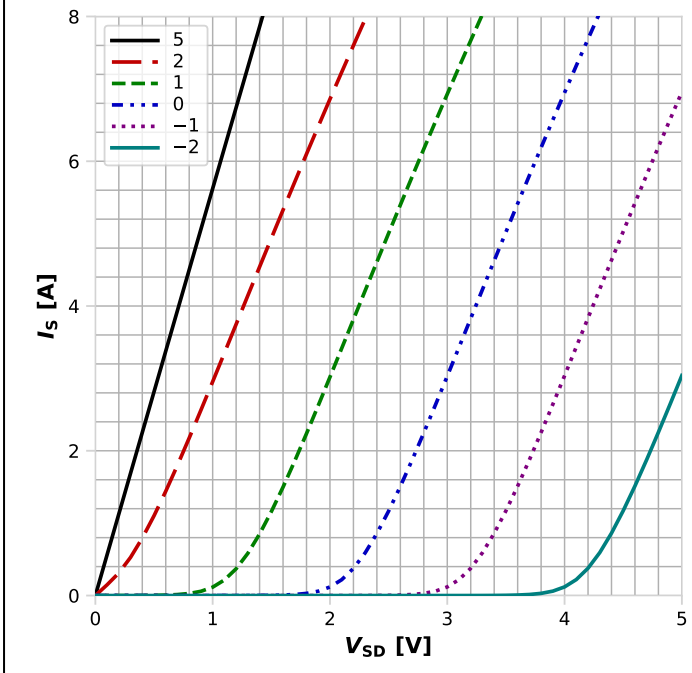
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS} *[V]*

Diagram 6: Typ. transfer characteristics



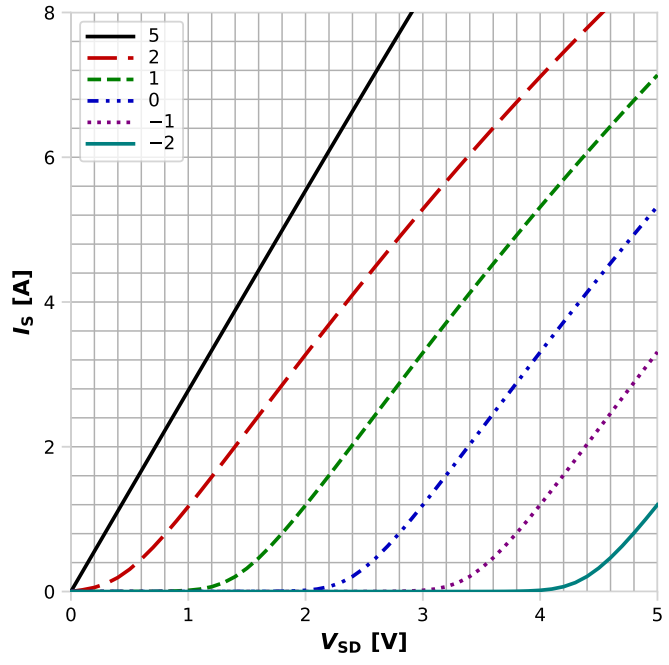
I_D=f(V_{GS}) |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j *[°C]*

Diagram 7: Typ. reverse output characteristics



I_S=f(V_{SD}); T_j=25 °C; parameter: V_{GS} *[V]*

Diagram 8: Typ. reverse output characteristics



I_s=f(V_{SD}); T_j=125 °C; parameter: V_{GS} *[V]*

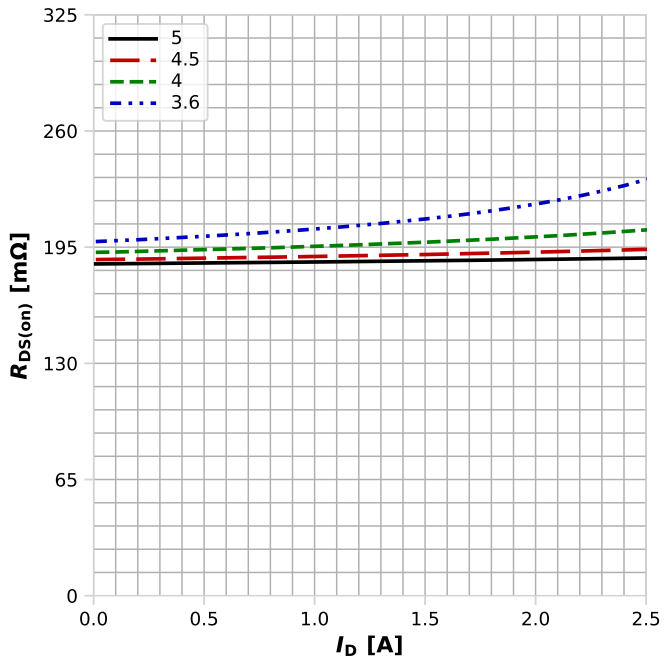
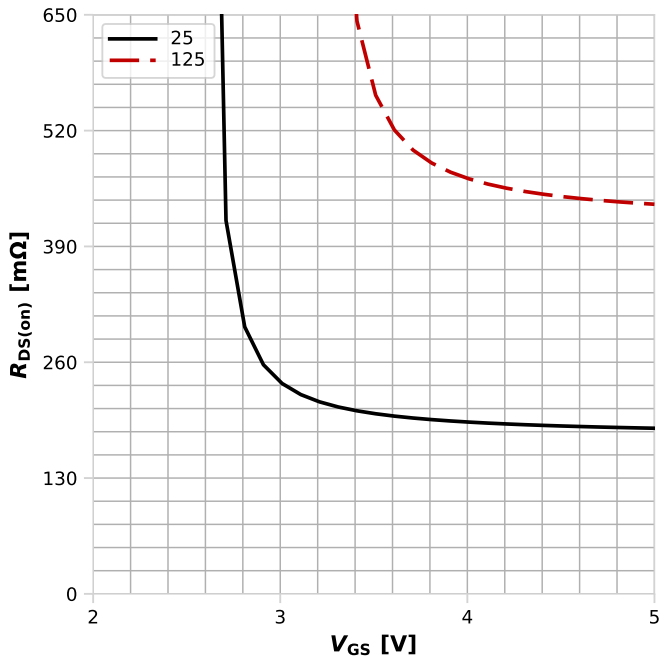
Diagram 9: Typ. drain-source on resistance	Diagram 10: Typ. drain-source on resistance
	
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS} *[V]*	$R_{DS(on)}$=f(V_{GS}); I_D=0.3 A; parameter: T_j *[°C]*

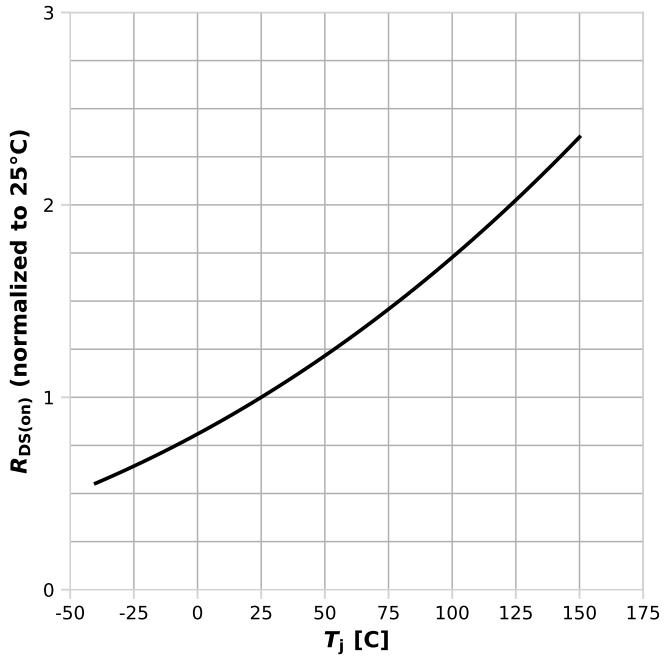
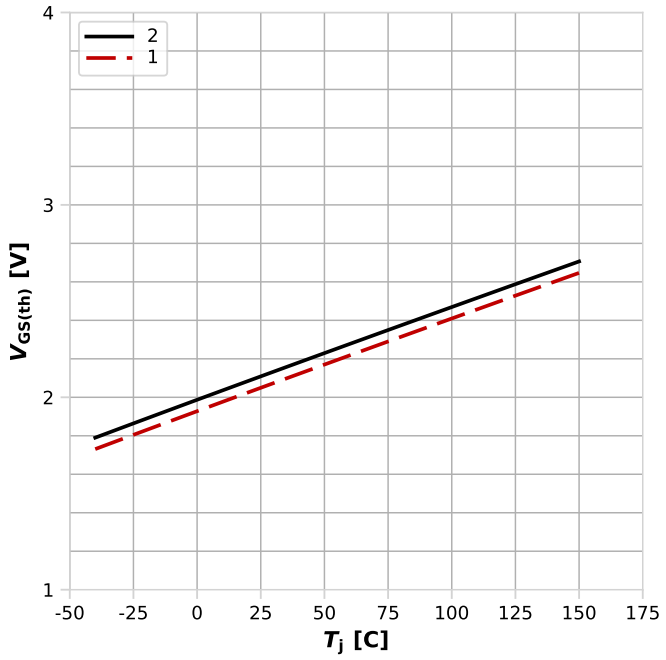
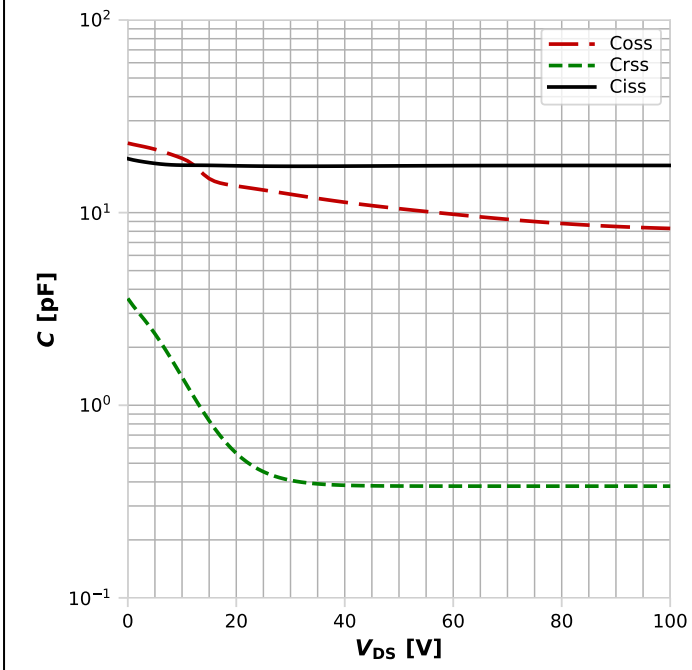
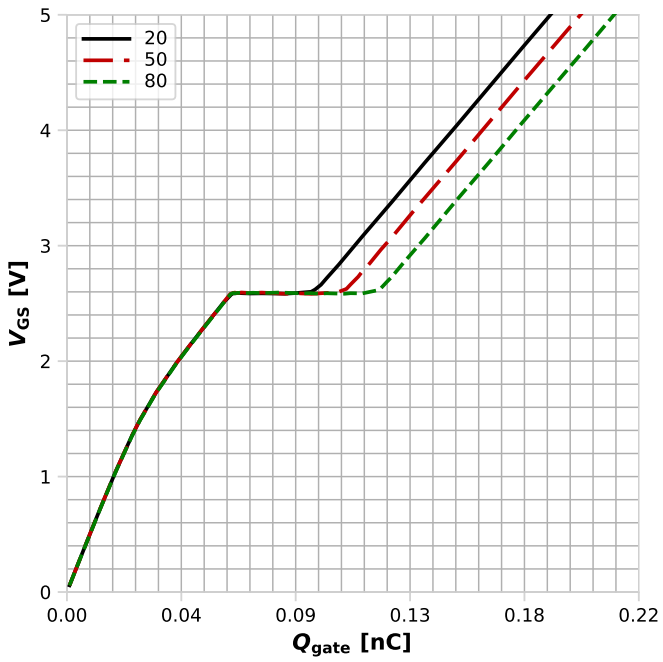
Diagram 11: Drain-source on-state resistance	Diagram 12: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=0.3 A; V_{GS}=5 V	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D *[mA]*

Diagram 13: Typ. capacitances



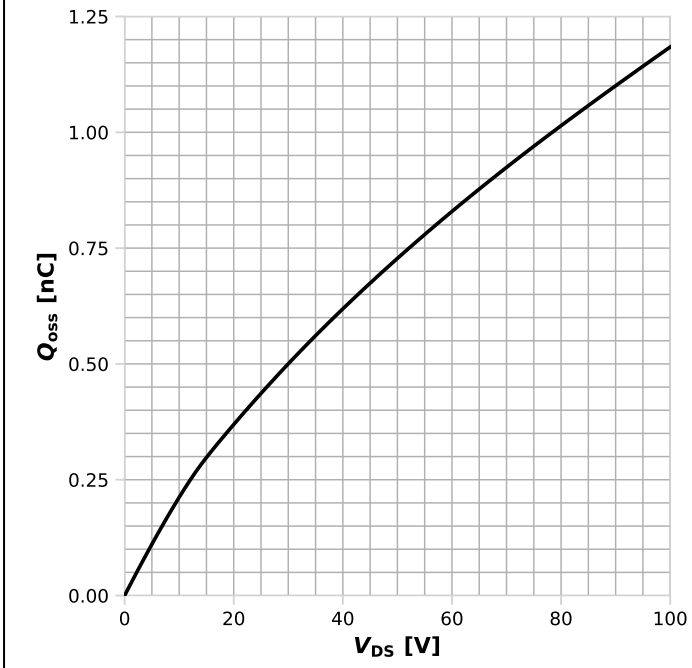
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 14: Typ. gate charge



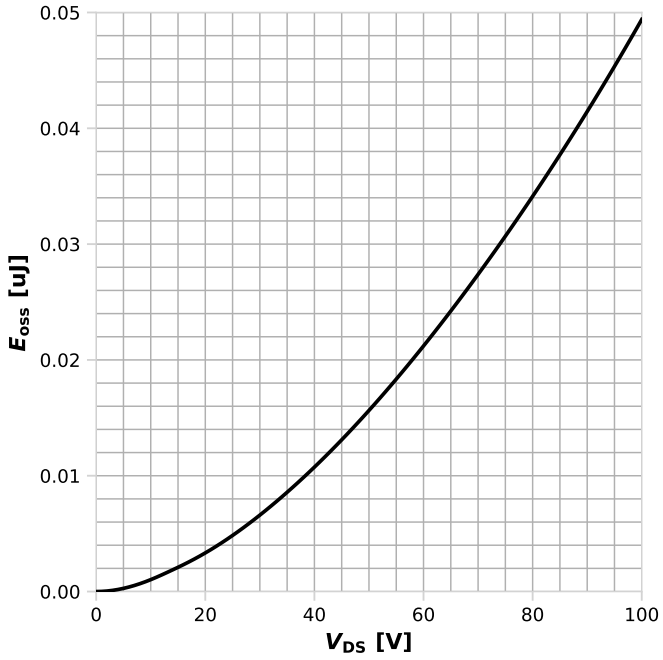
V_{GS}=f(Q_{gate}); I_D=0.3 A pulsed; parameter: V_{DS} *[V]*

Diagram 15: Typ. output charge



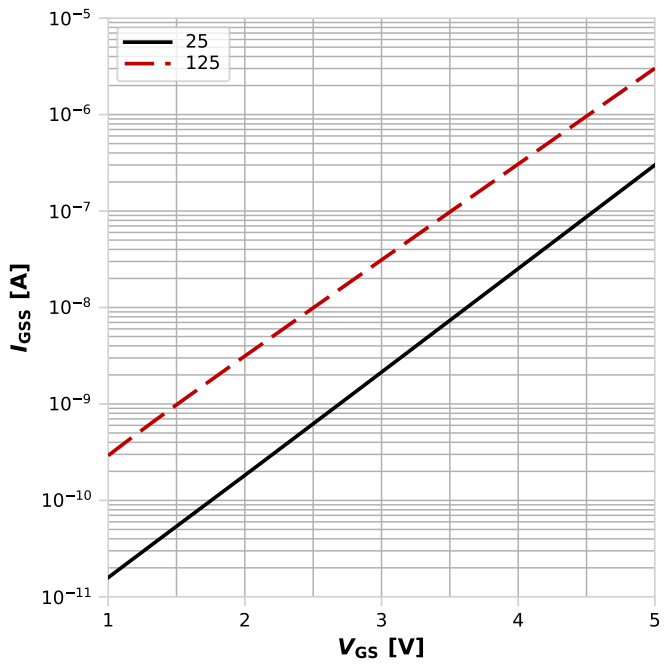
Q_{oss}=f(V_{DS}); V_{GS}=0 V

Diagram 16: Typ. output energy



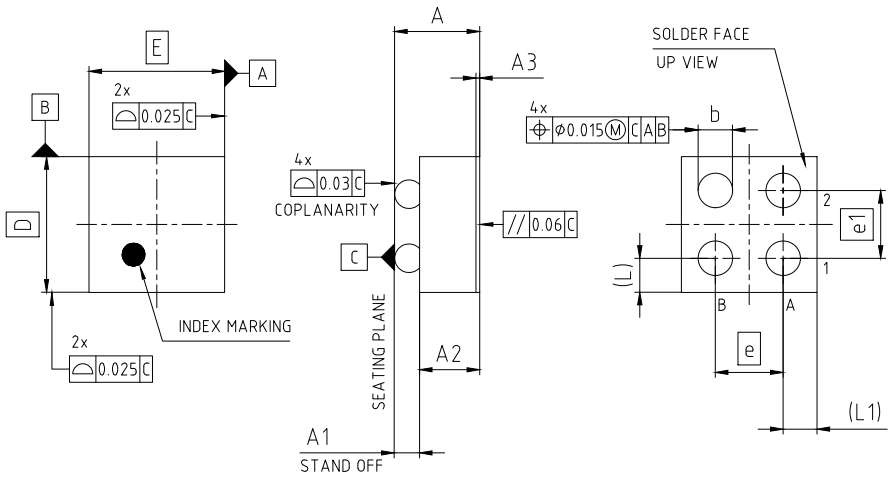
E_{oss}=f(V_{DS}); V_{GS}=0 V

Diagram 17: Typ. Gate-source leakage current



I_{GSS}=f(V_{GS}); V_{DS}=0 V; parameter: T_j *[°C]*

6 Package outlines



PACKAGE - GROUP NUMBER:	SG-UFWLB-4-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.531	0.597
A1	0.148	0.182
A2	0.385	0.413
A3	0.022	0.028
b	0.203	0.253
D	0.90	
E	0.90	
e	0.45	
e1	0.45	
L	0.225	
L1	0.225	

Figure 1 Outline SG-UFWLB-4, dimensions in mm

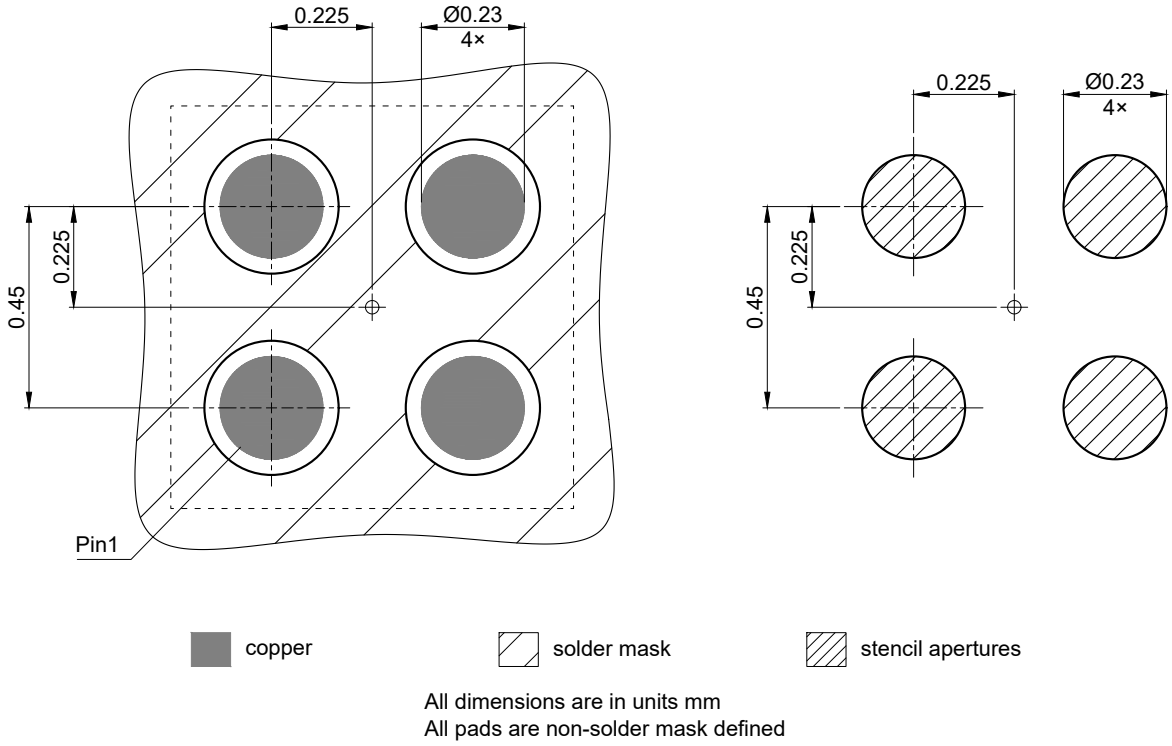


Figure 2 Footprint drawing SG-UFWLB-4, dimensions in mm

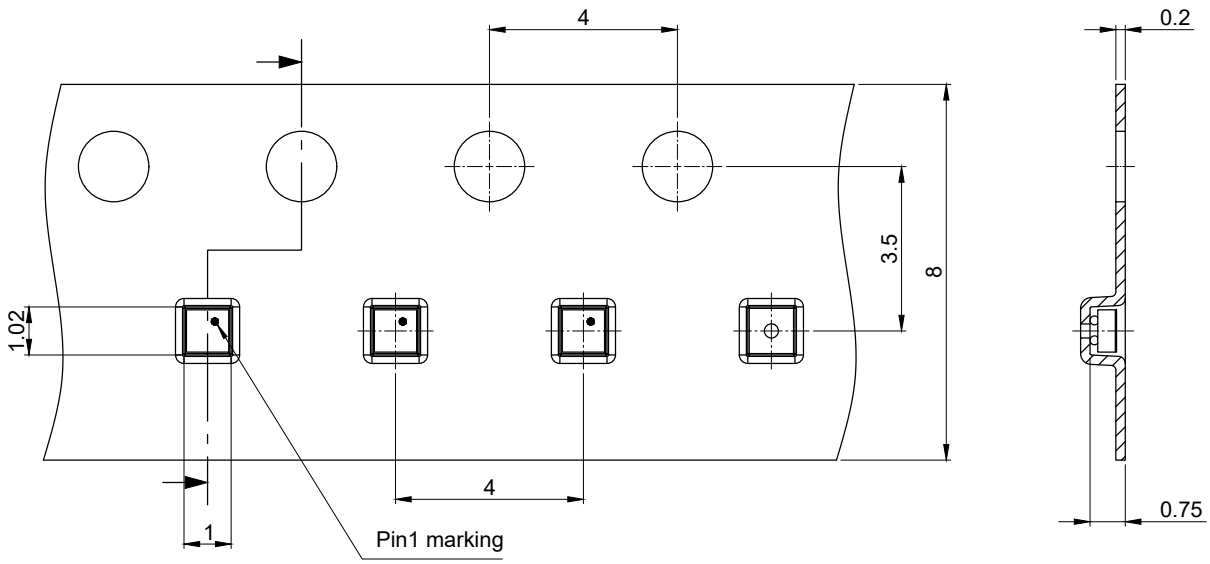


Figure 3 Packaging variant SG-UFWLB-4, dimensions in mm

7 Appendix A

Table 9 Related links

- IFX CoolGaN™ GaN webpage
- IFX CoolGaN™ reliability white paper
- IFX CoolGaN™ gate driver application note
- IFX CoolGaN™ Evaluation Boards
- IFX Packages

Revision history

IGKA23S101S

Revision 2026-08-07, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-08-07	Release of final version

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