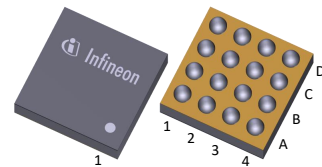


CoolGaN™
CoolGaN™ BDS 40 V

SG-UFWLB-16

Features

- E-mode bidirectional transistor - normally OFF switch
- Drain-to-Drain configuration
- Bidirectional blocking capability
- Low on-resistance, low gate charge, low output charge
- Qualified according to JEDEC for target applications
- Space saving chip scale packaging with topside protective coating
- OPN: IGK080B041SXUSA1



Potential applications

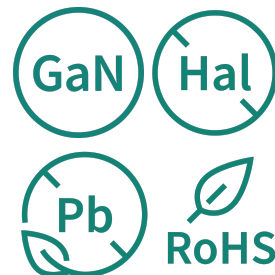
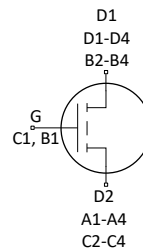
- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power supply system

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DD}	40	V
$R_{DD(on)}$	6.0	mΩ
I_D	35	A
Q_{oss}	5.0	nC
Q_G	5.3	nC



Part number	Package	Marking	Related links
IGK080B041S	SG-UFWLB-16	BF1	see Appendix A

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1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-drain voltage	V_{DD}	-	-	40	V	$V_{GD}=0\text{ V}$
Pulsed drain-drain voltage ¹⁾	$V_{DD,pulse}$	-	-	48	V	$V_{GD}=0\text{ V}$, 1 h total time
Continuous drain current	I_D	-	-	35	A	$V_{GD}=5\text{ V}$, $T_C=25\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	70	A	$T_j=25\text{ °C}$
Gate-drain voltage ¹⁾	V_{GD}	-40	-	6.0	V	-
Power dissipation	P_{tot}	-	-	21	W	$T_C=25\text{ °C}$
				1.6		$T_A=25\text{ °C}$, $R_{thJA}=62\text{ °C/W}$ ³⁾
Storage temperature	T_{stg}	-40	-	150	°C	-
Junction temperature	T_j			125		

¹⁾ Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

²⁾ Pulse current limited by transfer characteristic.

³⁾ Device on 1-layer FR4 PCB, vertical in still air.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-drain voltage	V_{GD}	-32	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	26	31	°C/W	-
Thermal resistance, junction - case, bottom		-	4.0	4.8		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	62	-	°C/W	On 1 layer PCB, vertical in still air.

4 Electrical Characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GD(th)}$	1.2	2.0	2.9	V	$V_{DD}=V_{GD}$, $I_D=3.0\text{ mA}$
Drain-drain leakage current	I_{DDs}	-	0.05	2.0	μA	$V_{DD}=40\text{ V}$, $V_{GD}=0\text{ V}$, $T_j=25\text{ °C}$
Gate-drain leakage current	I_{GDS}	-	3.3	6.7	μA	$V_{GD}=5\text{ V}$, $T_j=25\text{ °C}$
			0.01	0.1		$V_{GD}=-4\text{ V}$, $T_j=25\text{ °C}$
			10	20		$V_{GD}=5\text{ V}$, $T_j=85\text{ °C}$
			0.01	0.1		$V_{GD}=-4\text{ V}$, $T_j=85\text{ °C}$
Drain-drain on-state resistance	$R_{DD(on)}$	-	6.0	8.0	$\text{m}\Omega$	$V_{GD}=5\text{ V}$, $I_D=5\text{ A}$
Gate resistance ⁴⁾	R_G	-	0.5	-	Ω	-

⁴⁾ Defined by design. Not subject to production test.

Table 6 Capacitance characteristics ⁵⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{ISS}	-	370	-	pF	$V_{GD}=0\text{ V}$, $V_{DD}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{OSS}		140			
Reverse transfer capacitance	C_{RSS}		87			

⁵⁾ Defined by design. Not subject to production test.

Table 7 Gate charge characteristics ⁶⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate charge at threshold	$Q_{g(th)}$	-	1.0	-	nC	$V_{DD}=20\text{ V}$, $I_D=14\text{ A}$, $V_{GD}=0\text{ to }5\text{ V}$
Gate to drain charge	Q_{gd}		2.1		nC	
Gate charge total	Q_g		5.3		nC	
Gate plateau voltage	$V_{plateau}$		2.7		V	
Output charge	Q_{OSS}		5.0		nC	

⁶⁾ Defined by design. Not subject to production test.

5 Electrical characteristics diagrams

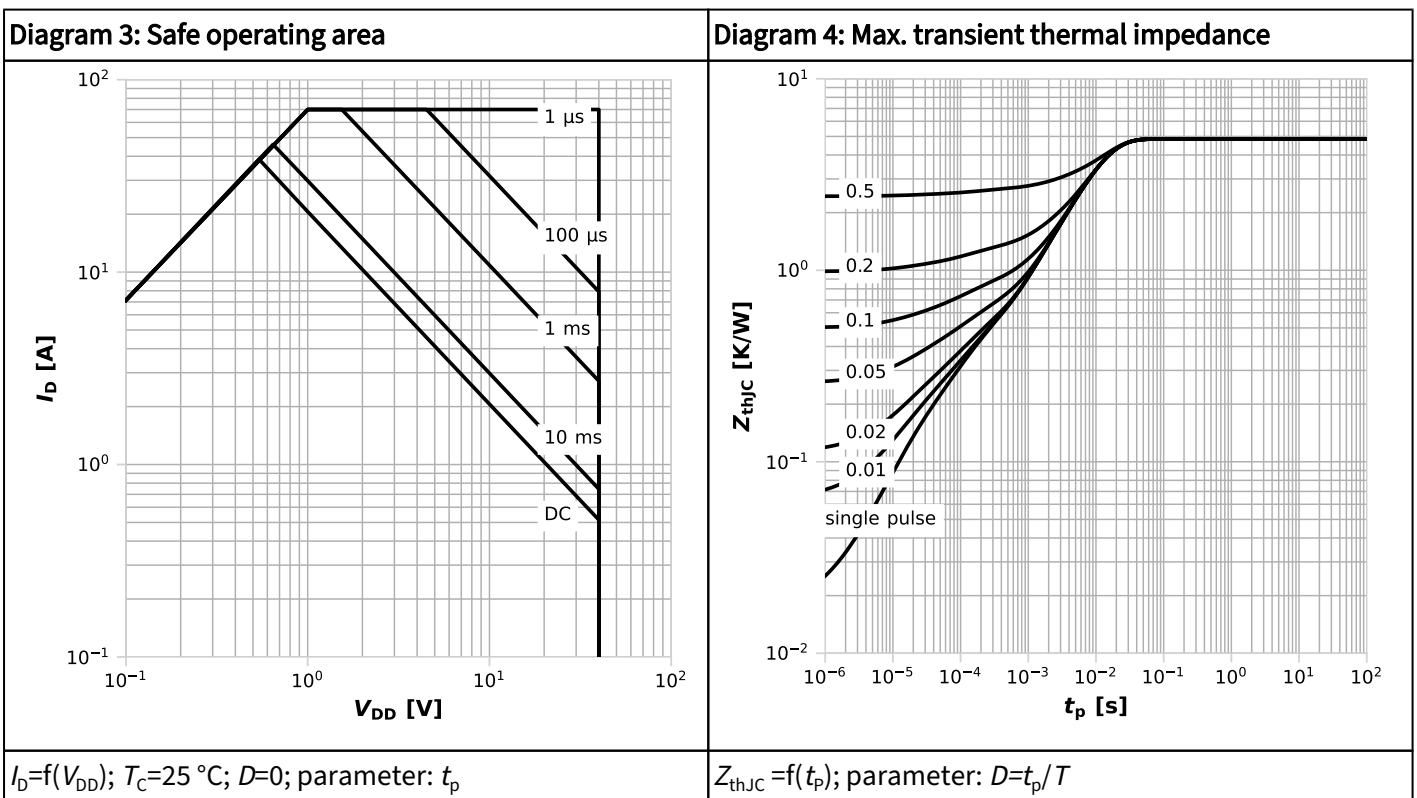
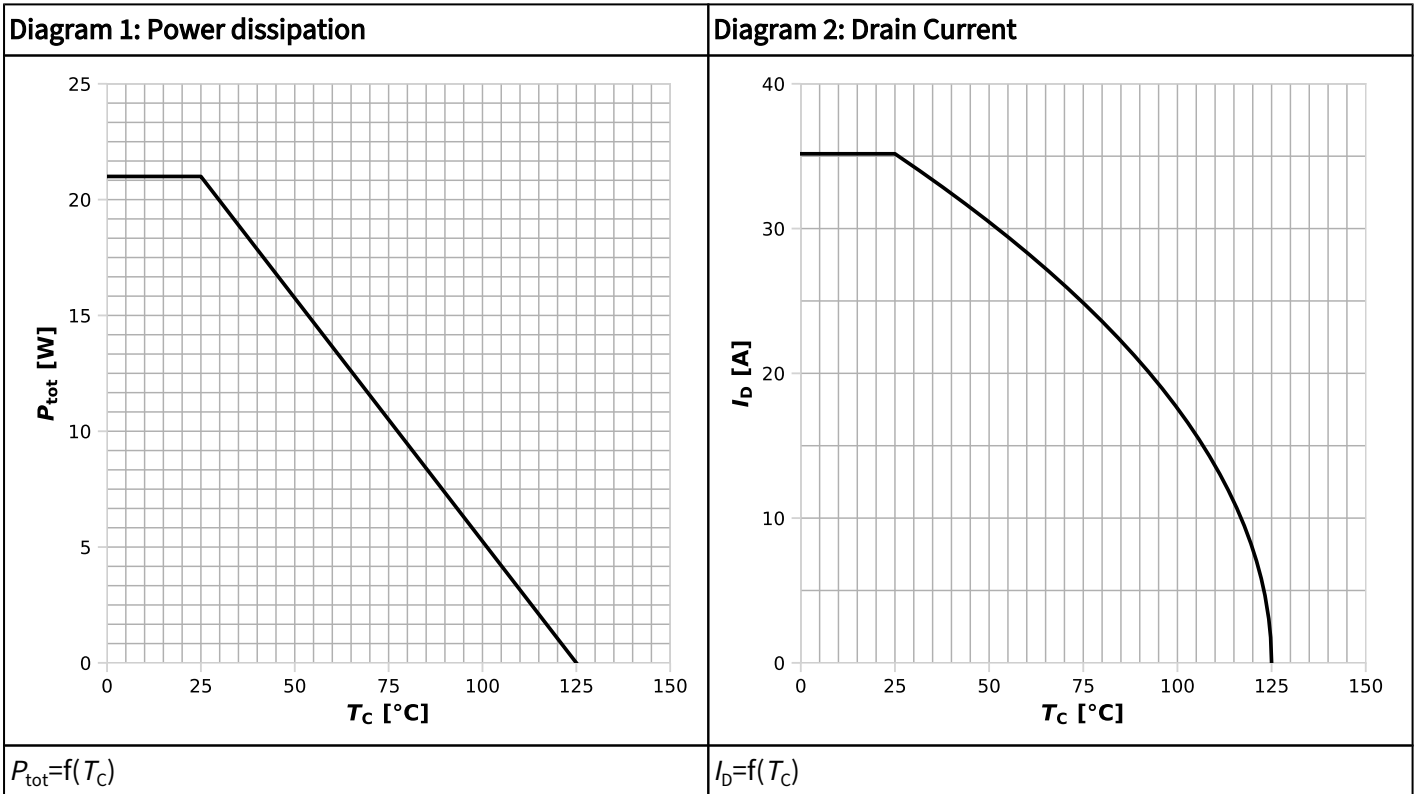
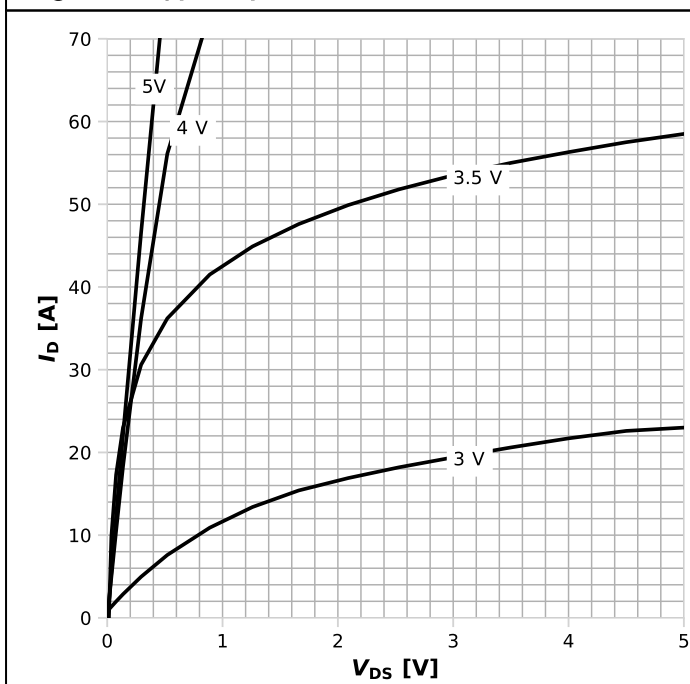
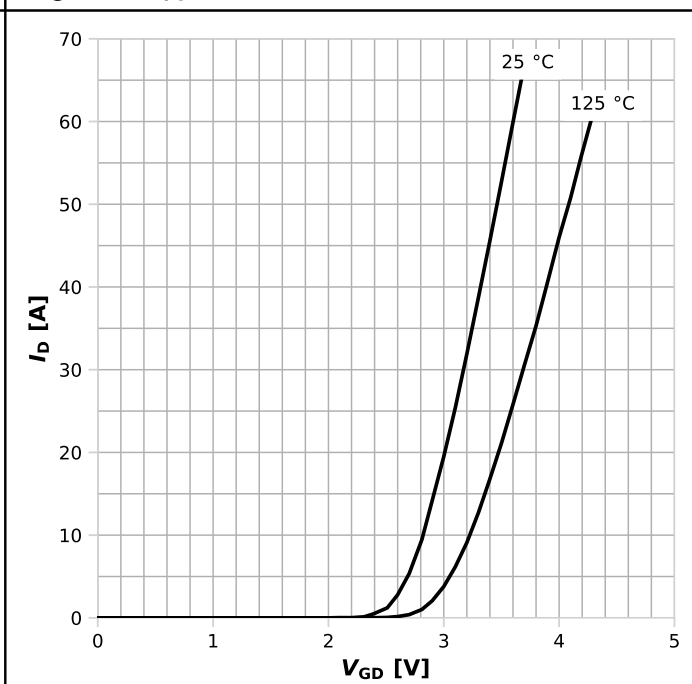


Diagram 5: Typ. output characteristics



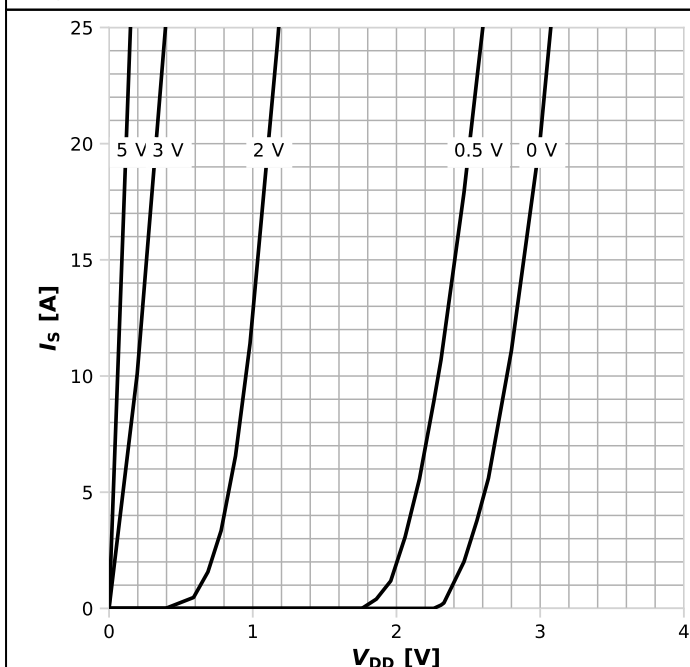
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. transfer characteristics



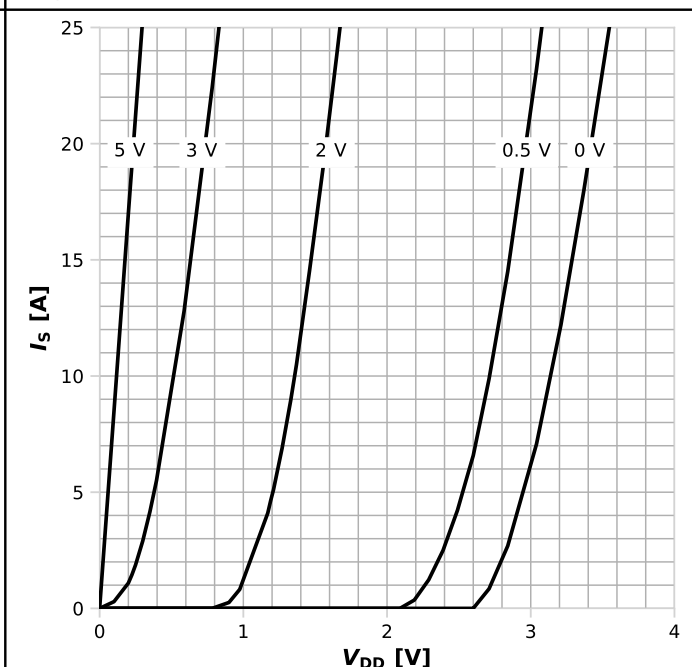
$I_D = f(V_{GD}); |V_{DD}| > 2|I_D|R_{DD(on)max}; \text{parameter: } T_j$

Diagram 7: Typ. channel reverse characteristics



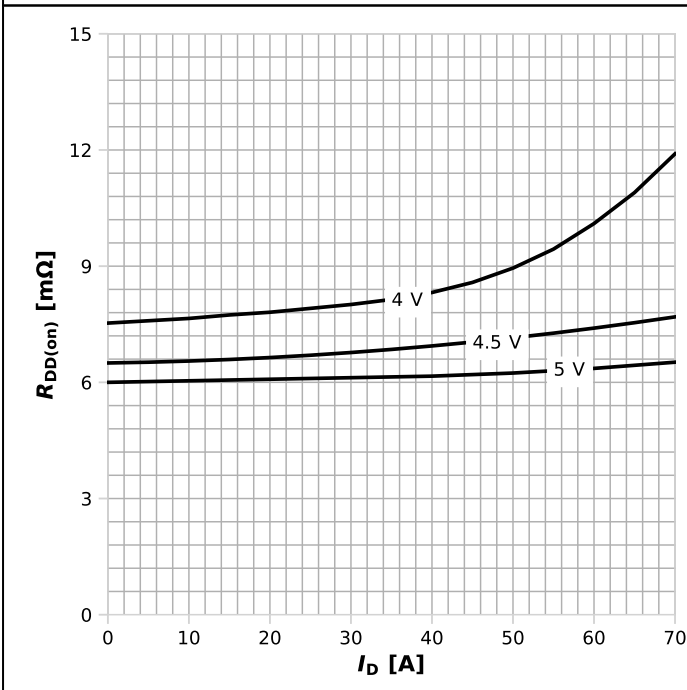
$I_S = f(V_{DD}); T_j = 25\text{ °C}; \text{parameter: } V_{GD}$

Diagram 8: Typ. channel reverse characteristics



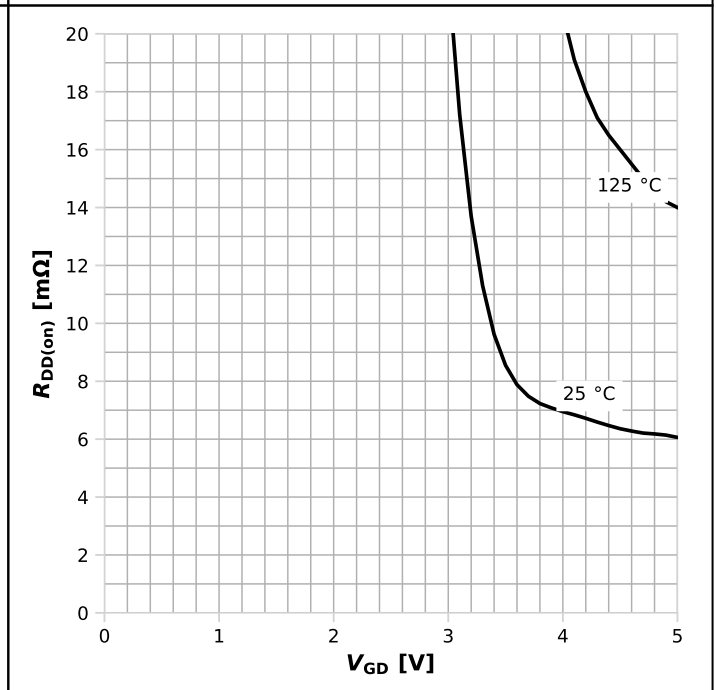
$I_S = f(V_{DD}); T_j = 125\text{ °C}; \text{parameter: } V_{GD}$

Diagram 9: Typ. drain-drain on-state resistance



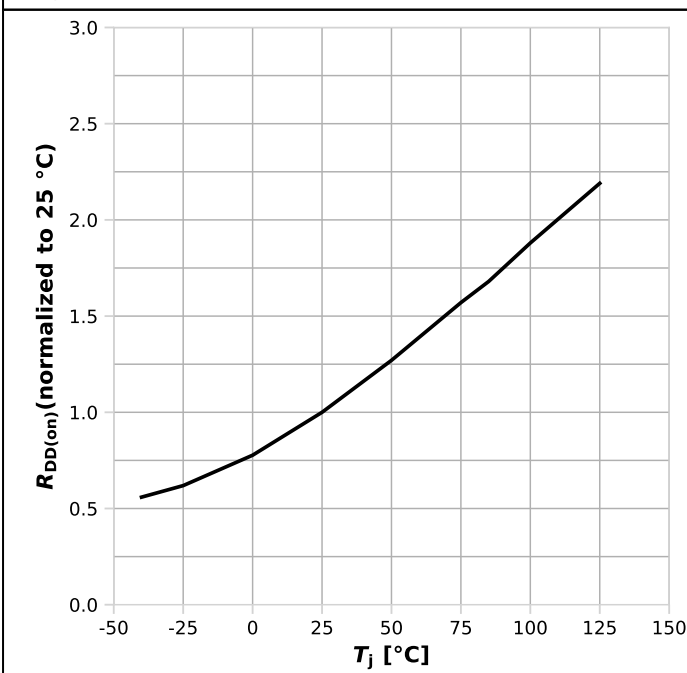
$R_{DD(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}; \text{parameter: } V_{GD}$

Diagram 10: Typ. Drain-drain on-state resistance



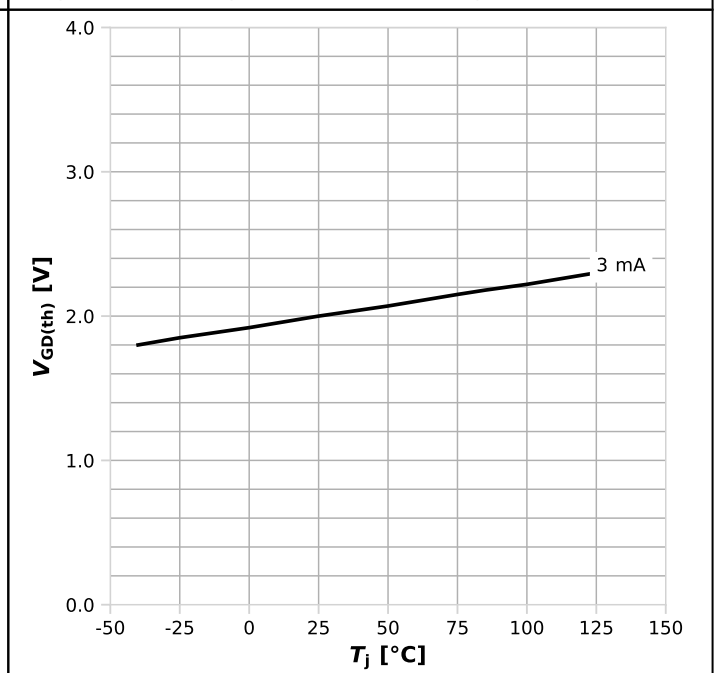
$R_{DD(on)}=f(V_{GD}); I_D=5\text{ A}; \text{parameter: } T_j$

Diagram 11: Drain-drain on-state resistance



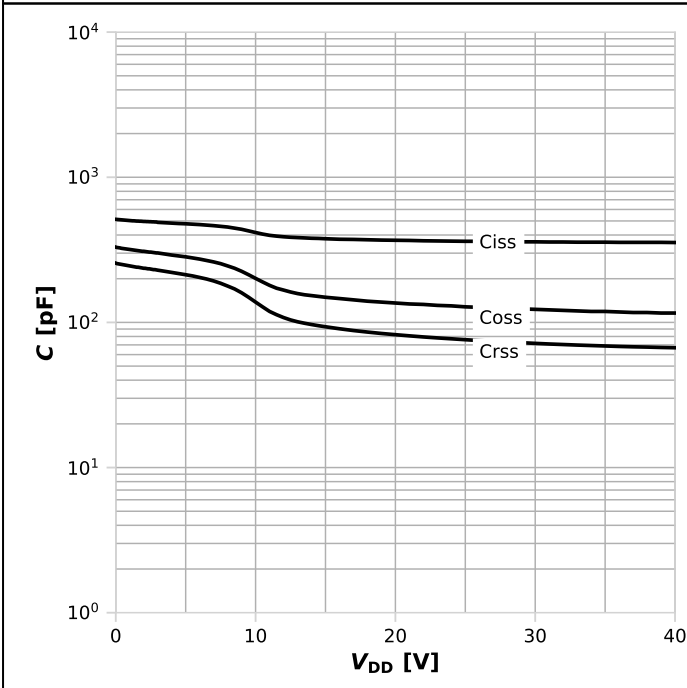
$R_{DD(on)}=f(T_j); I_D=5\text{ A}, V_{GD}=5\text{ V}$

Diagram 12: Typ. gate threshold voltage



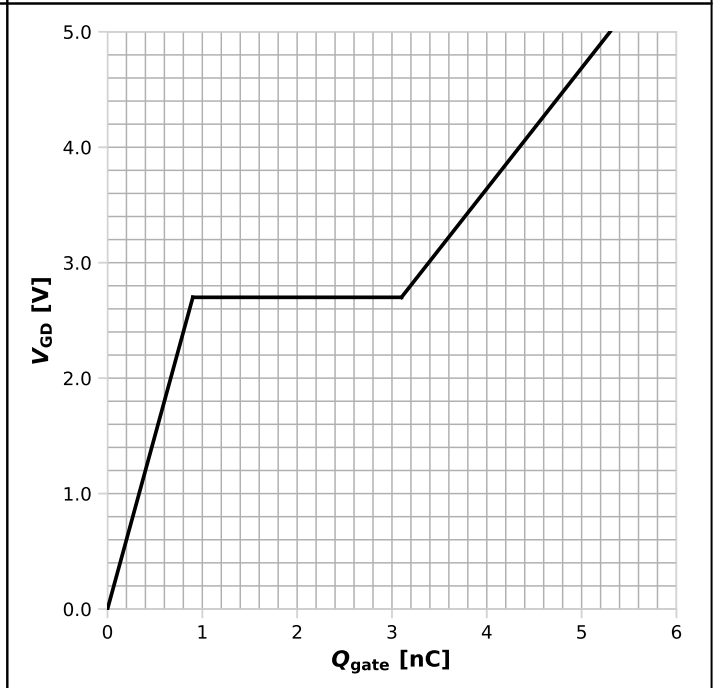
$V_{GD(th)}=f(T_j), V_{GD}=V_{DD}; \text{parameter: } I_D$

Diagram 13: Typ. capacitances



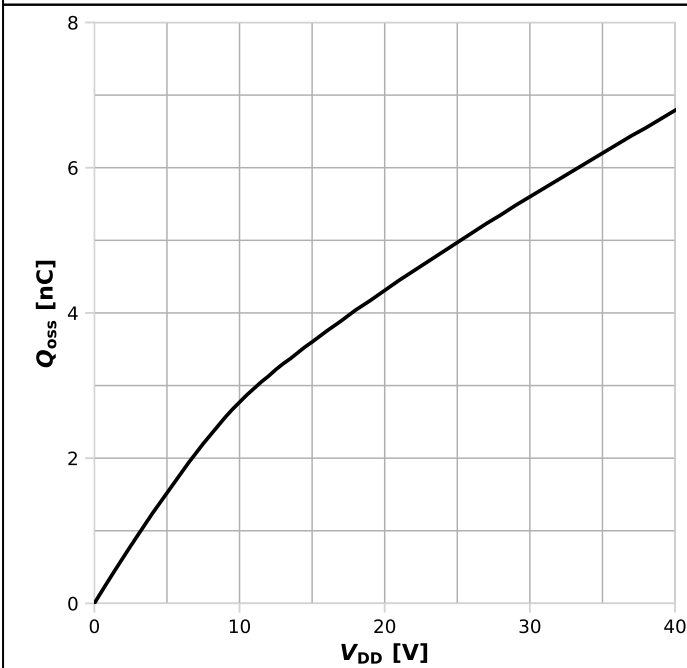
$C=f(V_{DD}); V_{GD}=0\text{ V}$

Diagram 14 Typ. gate charge



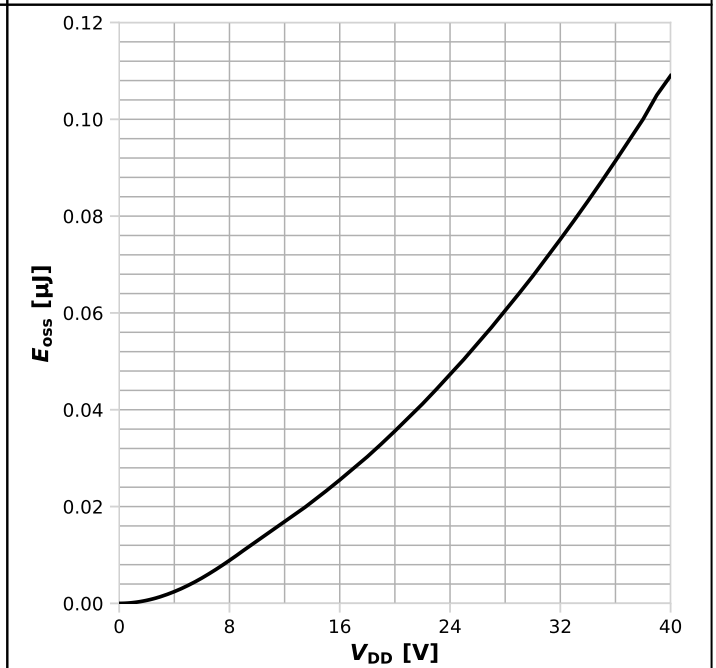
$V_{GD}=f(Q_{gate}); I_D=14\text{ A pulsed}; V_{DD}=20\text{ V}$

Diagram 15: Typ. output charge



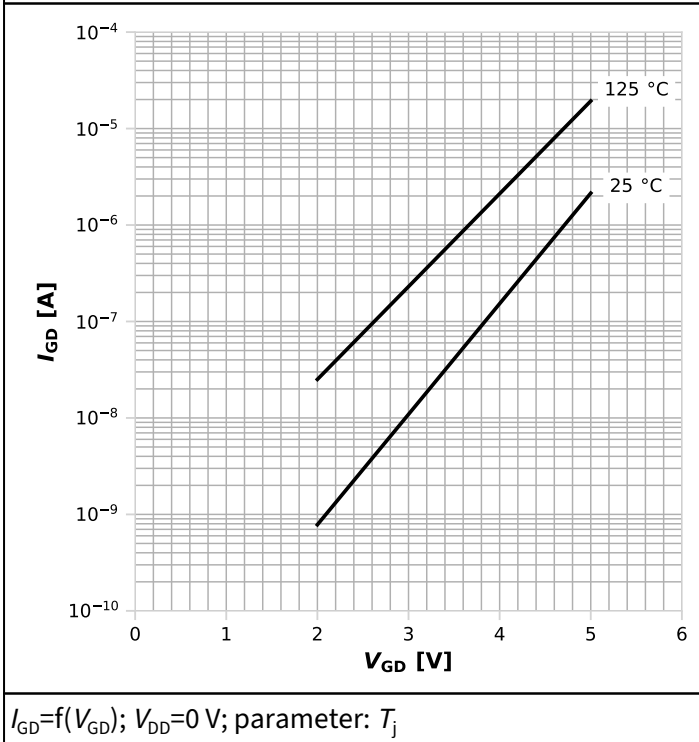
$Q_{oss}=f(V_{DD}), V_{GD}=0\text{ V}$

Diagram 16: Typ. Coss stored Energy

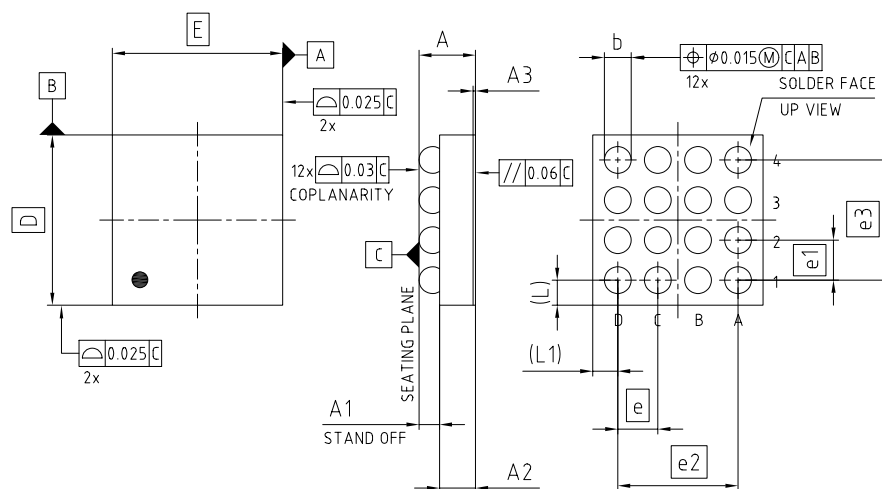


$E_{oss}=f(V_{DD}), V_{GD}=0\text{ V}$

Diagram 17: Typ. gate characteristics forward



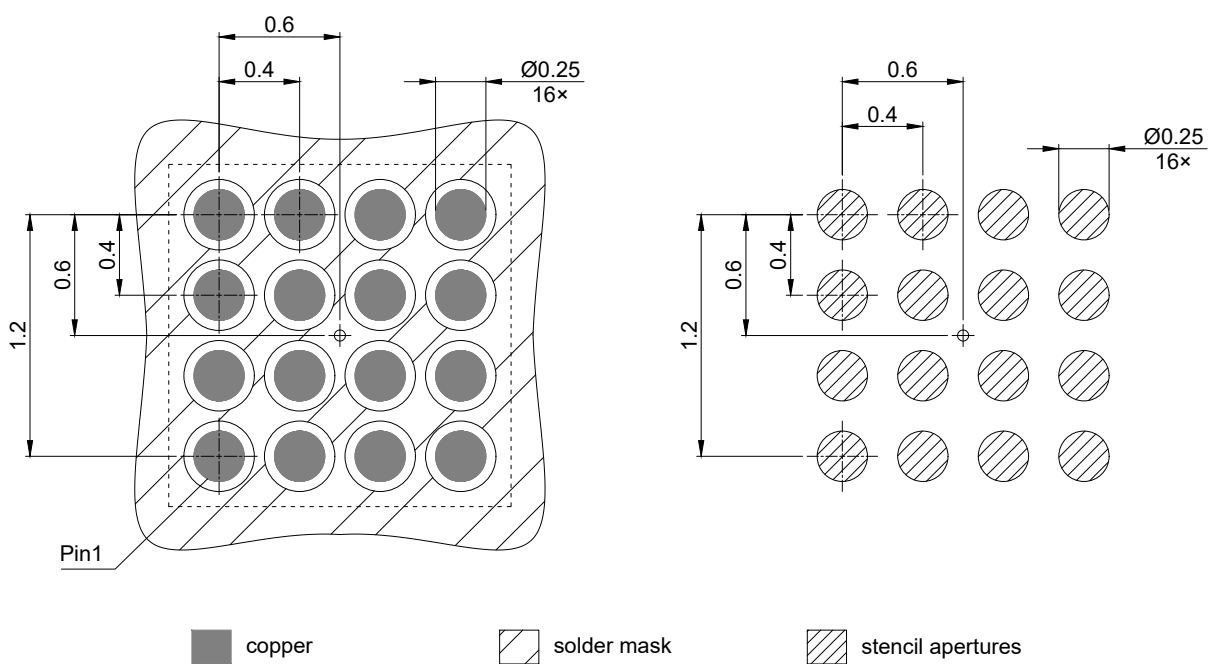
6 Package outlines



PACKAGE - GROUP NUMBER: SG-UFWLB-16-U01		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.531	0.597
A1	0.175	0.235
A2	0.346	0.374
A3	0.022	0.028
b	0.241	0.295
D	1.70	
E	1.70	
e	0.40	
e1	0.40	
e2	1.20	
e3	1.20	
L	0.25	
L1	0.25	

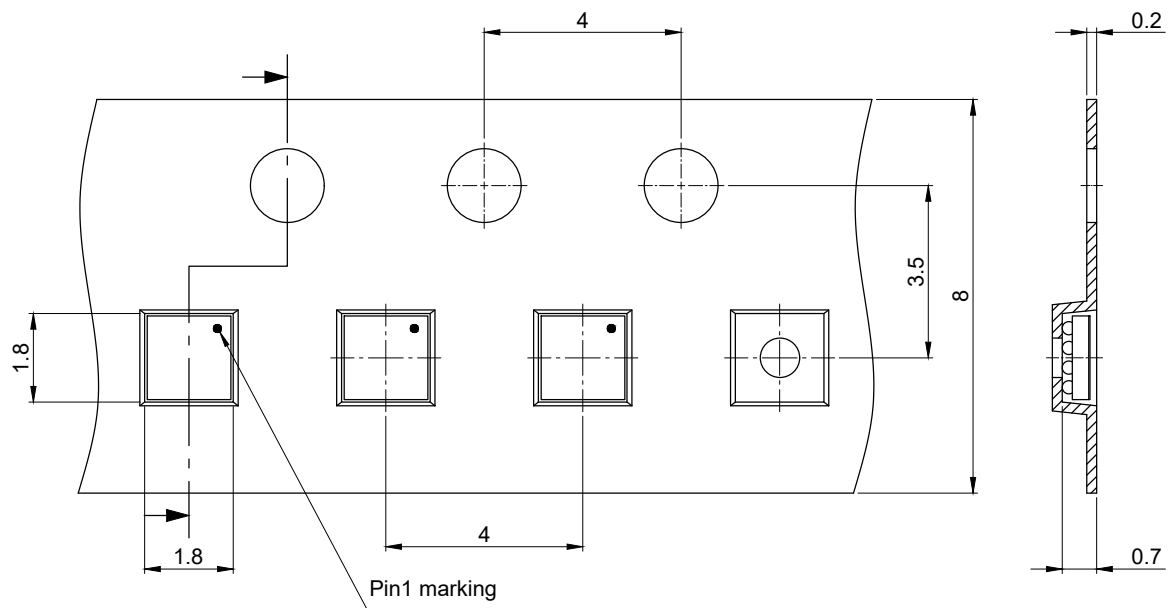
NOTE: Space saving chip scale packaging with topside protective coating

Figure 1 Outline SG-UFWLB-16, dimensions in mm



All dimensions are in units mm
All pads are non-solder mask defined

Figure 2 Footprint drawing SG-UFWLB-16, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant SG-UFWLB-16, dimensions in mm

7 Appendix A

Table 8 Related links

- [IFX CoolGaN™ GaN webpage](#)
- [IFX CoolGaN™ reliability white paper](#)
- [IFX Packages Description-SG-UFWLB-16-2](#)

Revision history

IGK080B041S

Revision 2026-01-23, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-04-07	First release
1.1	2026-01-23	Drawing update

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