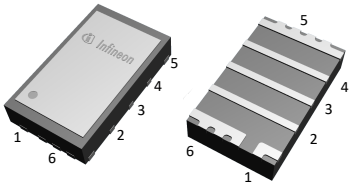
CoolGaN™

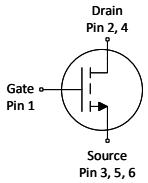
PG-TSON-6

CoolGaN™ Transistor 120 V G3



Features

- Ultra fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade 3x5 package



Top side is exposed silicon substrate, internally connected to source terminal. Not recommended to use as an electrical connection.

Potential applications

- Battery powered tools
- Sync Rectification for AC-DC and DC-DC converters
- Robotics and drones
- e-Mobility, UAVs
- Solar & Energy storage systems

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	120	V
$R_{DS(on)}$	2.7	mΩ
I_D	71	A
Q_{oss}	49	nC
Q_G	10	nC
Q_{rr}	0	nC

Part number	Package	Marking	Related links
IGC037S12S1	PG-TSON-6	37SE1	see Appendix A

Table of contents

Description 1
Maximum ratings 3
Recommended operating conditions 4
Thermal characteristics 5
Electrical Characteristics 6
Electrical characteristics diagrams 8
Package outlines 13
Appendix A 16
Revision history 17
Trademarks 18
Disclaimer 18

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	120	V	V_{GS}=0 V
Pulsed drain-source voltage [1]	$V_{DS,\ pulse}$	-	-	144	V	V_{GS}=0 V, 1 h total time
Continuous drain current	I_D	-	-	71	A	V_{GS}=5 V, T_C=25 °C
				19		V_{GS}=5 V, T_A=25 °C, R_{thJA}=38 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	520	A	T_j=25 °C
				270		T_j=150 °C
Pulsed gate-source voltage [1]	V_{GS}	-6.5	-	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	45	W	T_C=25 °C
				3.3		T_A=25 °C, R_{thJA}=38 °C/W [2]
Storage temperature	T_{stg}	-55	-	150	°C	-
Junction temperature	T_j	-40				

[1] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

[2] Device on 4-layer FR4 PCB, vertical in still air.

[3] Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	0.5	0.6	°C/W	-
Thermal resistance, junction - case, bottom			1.9	2.8		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	60	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	38	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical Characteristics

at T_j=25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	2.0	2.9	V	V_{DS}=V_{GS}, I_D=7.0 mA
Drain-source leakage current	I_{DSS}	-	0.15	2.1	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C
			6.0	50		V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	15	250	µA	V_{GS}=5 V, T_j=25 °C
			0.01	0.1		V_{GS}=-4 V, T_j=25 °C
			110	1010		V_{GS}=5 V, T_j=125 °C
			0.01	0.1		V_{GS}=-4 V, T_j=125 °C
Drain-source on-state resistance	$R_{DS(on)}$	-	2.7	3.7	mΩ	V_{GS}=5 V, I_D=18 A
Gate resistance [4)]	R_G	-	0.5	-	Ω	-

4) Defined by design. Not subject to production test.

Table 6 Capacitance characteristics [5)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1000	1100	pF	V_{GS}=0 V, V_{DS}=60 V, f=1 MHz
Output capacitance	C_{oss}		500	550		
Reverse transfer capacitance	C_{rss}		4.9	6.4		

5) Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.7	-	nC	V_{DS}=60 V, I_D=18 A, V_{GS}=0 to 5 V
Gate charge at threshold	$Q_{g(th)}$		2.0	-	nC	
Gate to drain charge [6)]	Q_{gd}		2.3	-	nC	
Switching charge	Q_{sw}		3.0	-	nC	
Gate charge total [6)]	Q_g		10	13	nC	
Gate plateau voltage	$V_{plateau}$		2.7	-	V	
Output charge [6)]	Q_{oss}	-	49	54	nC	V_{DS}=60 V, V_{GS}=0 V

6) Defined by design. Not subject to production test.

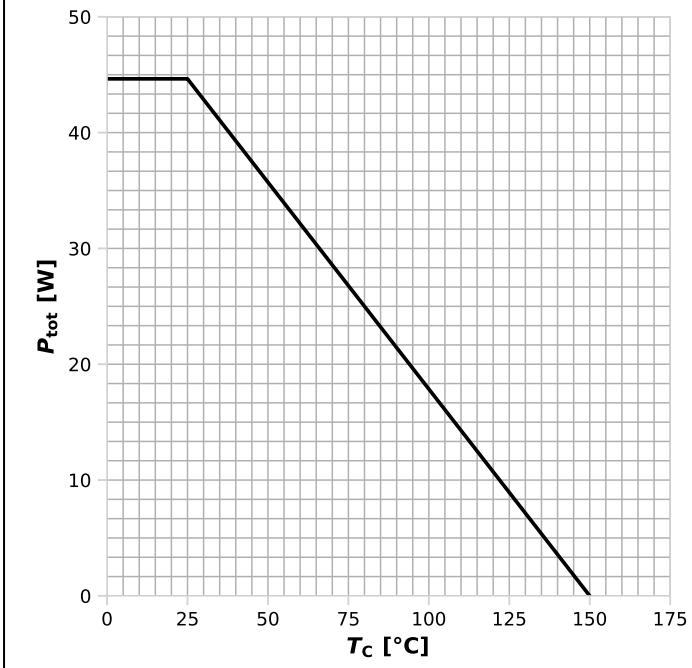
Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	15	A	T_C=25 °C
Pulsed current, reverse	$I_{S,pulse}$			284		
Source-Drain reverse voltage	V_{SD}	-	2.6	3.4	V	V_{GS}=0 V, $I_{S,pulse}$=18 A, T_j=25 °C
			2.1	-		V_{GS}=0 V, $I_{S,pulse}$=0.5 A, T_j=25 °C
Reverse recovery charge [7)]	Q_{rr}	-	0	-	nC	V_R=60 V, $I_{S,pulse}$=18 A, d$i_{S,pulse}$/dt =100 A/µs

7) Defined by design. Not subject to production test.

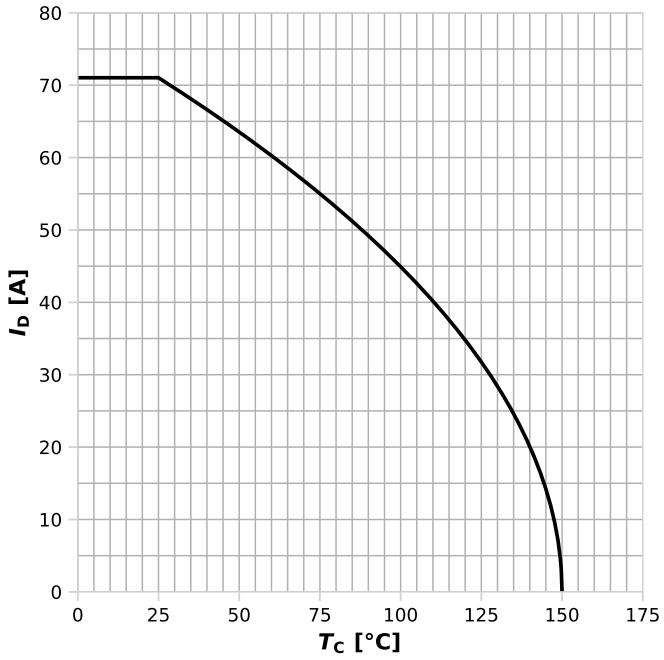
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



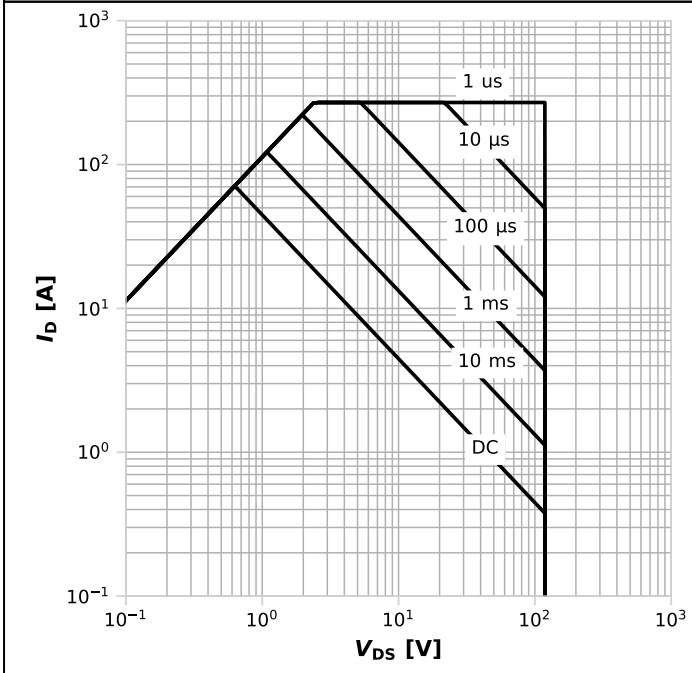
P_{tot}=f(T_C)

Diagram 2: Drain Current



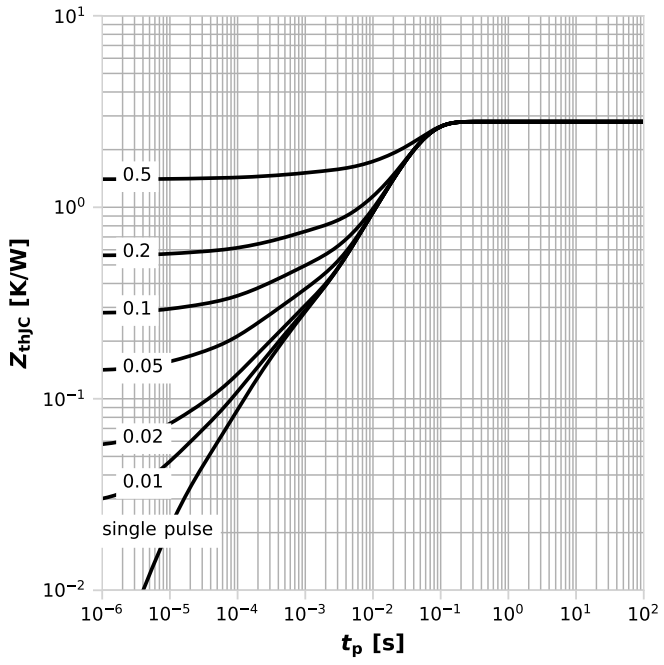
I_D=f(T_C)

Diagram 3: Safe operating area



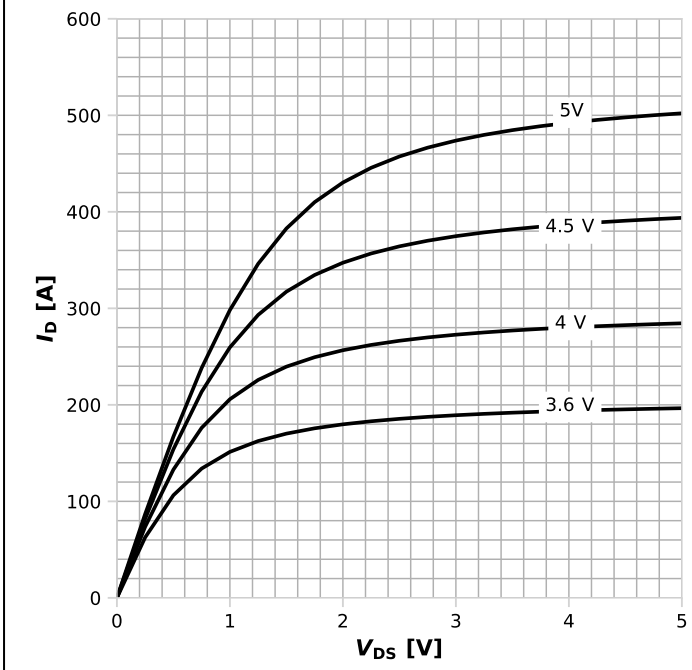
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



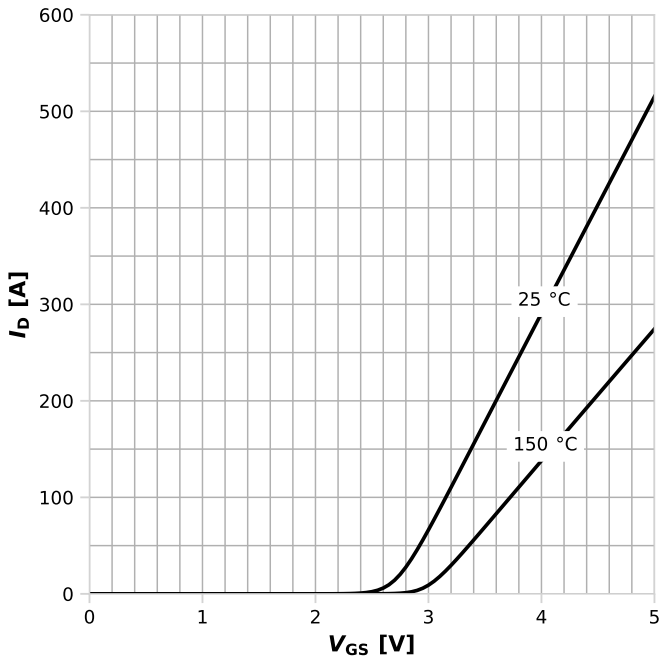
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



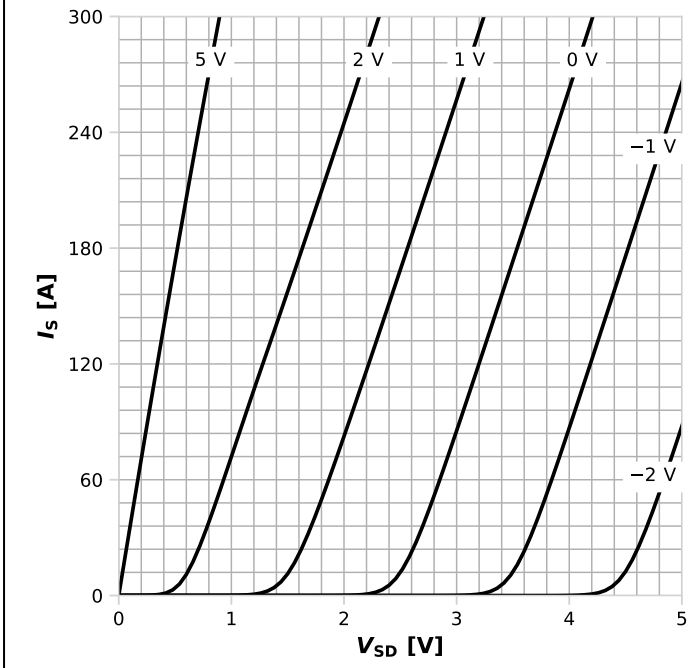
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. transfer characteristics



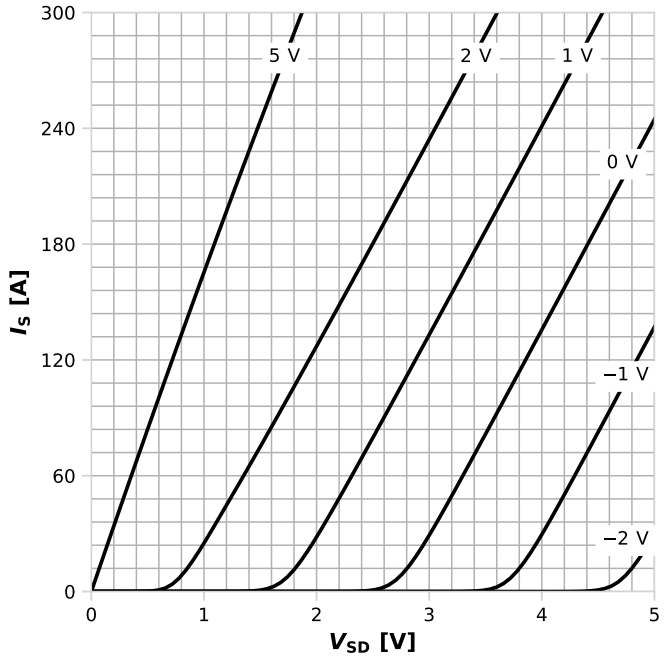
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 7: Typ. channel reverse characteristics



I_S=f(V_{SD}); T_j=25 °C; parameter: V_{GS}

Diagram 8: Typ. channel reverse characteristics



I_S=f(V_{SD}); T_j=125 °C; parameter: V_{GS}

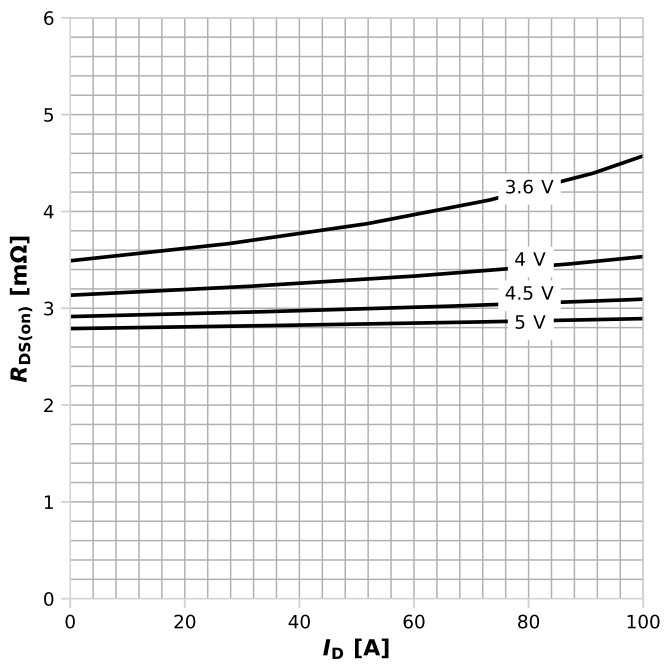
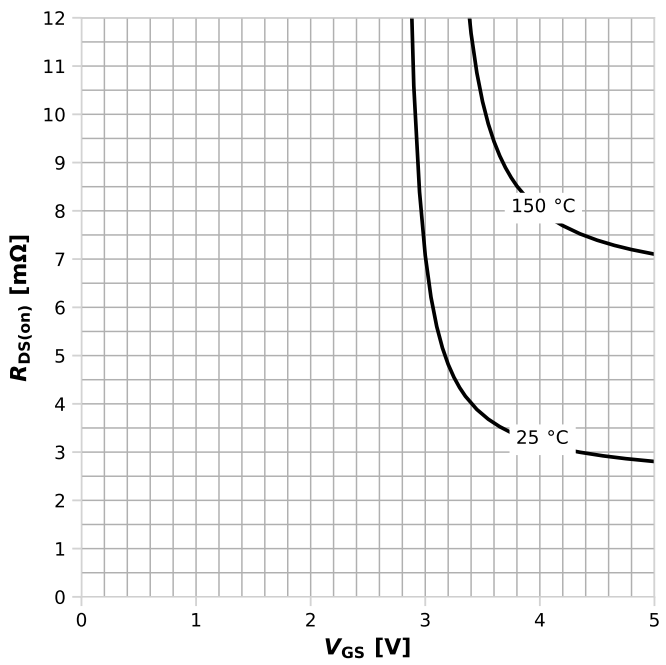
Diagram 9: Typ. drain-source on-state resistance	Diagram 10: Typ. Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(V_{GS}); I_D=18 A; parameter: T_j

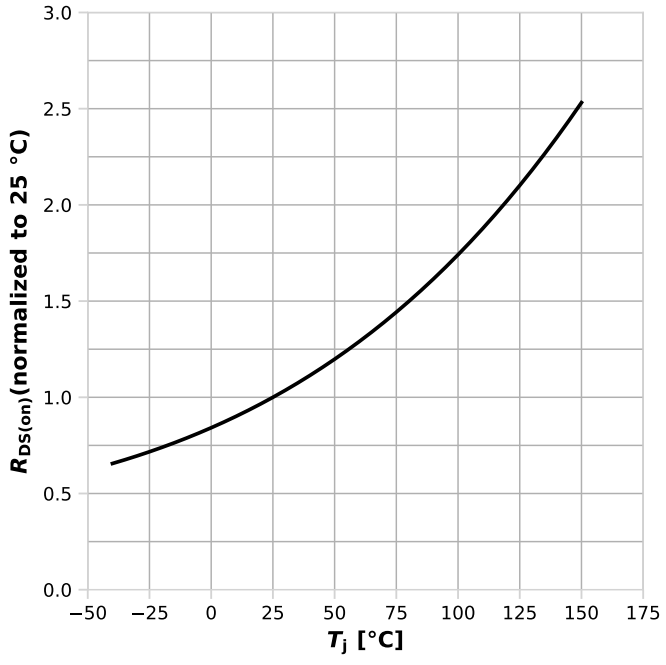
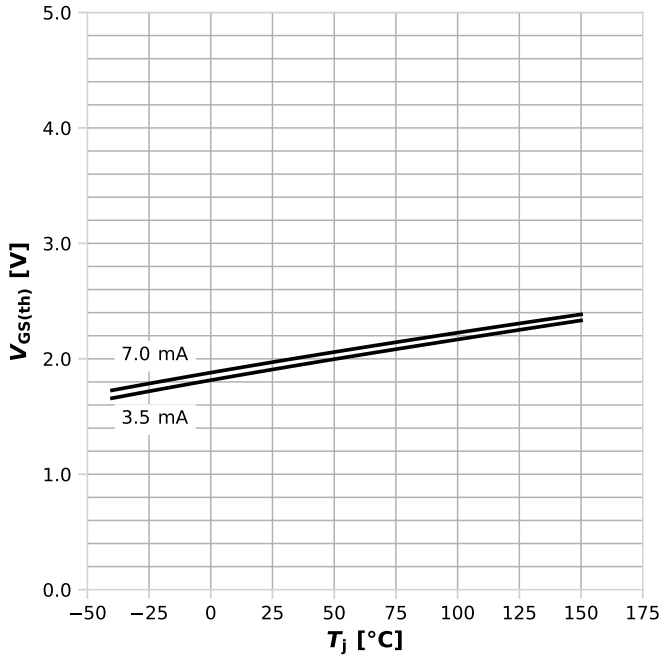
Diagram 11: Drain-source on-state resistance	Diagram 12: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=18 A, V_{GS}=5V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

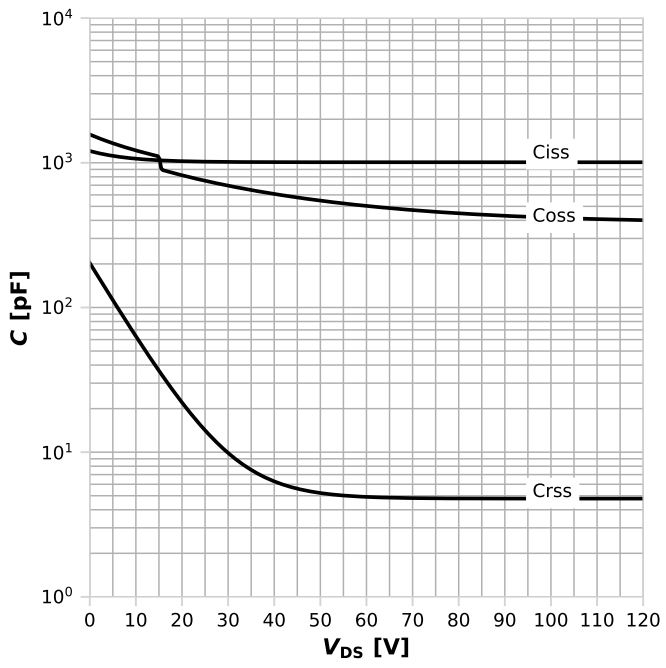
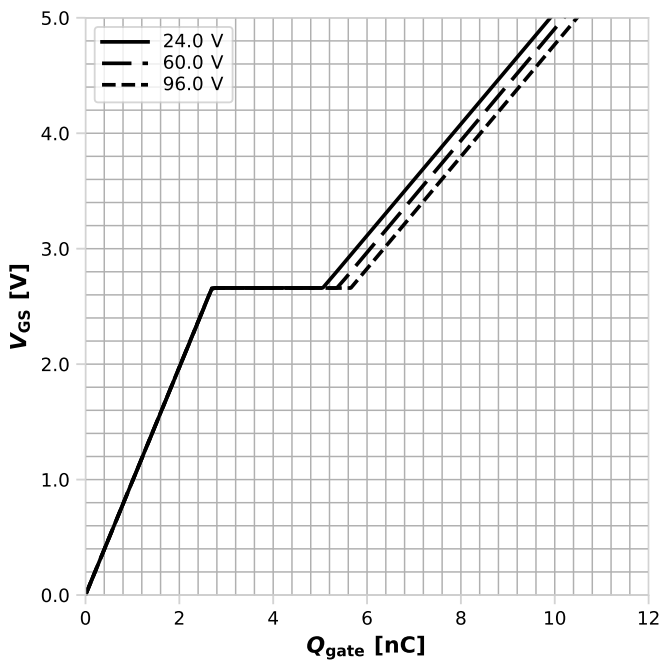
Diagram 13: Typ. capacitances	Diagram 14 Typ. gate charge
	
C=f(V_{DS}); V_{GS}=0 V	V_{GS}=f(Q_{gate}); I_D=18 A pulsed; parameter: V_{DS}

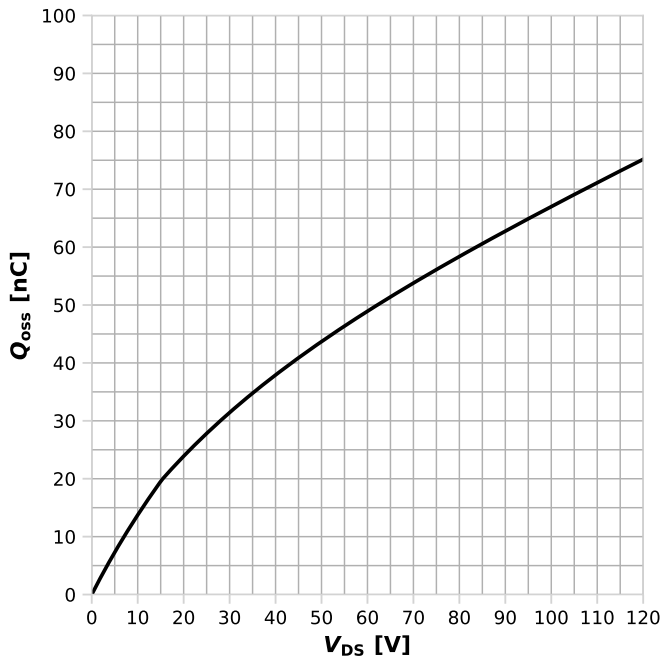
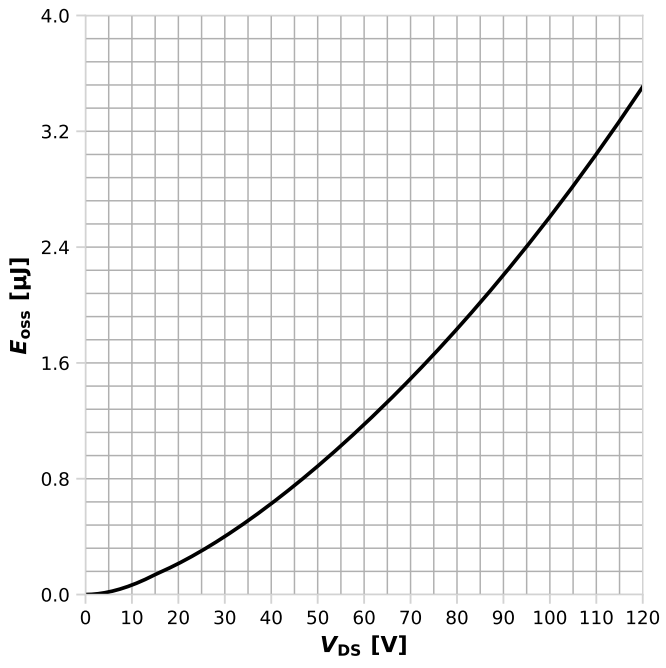
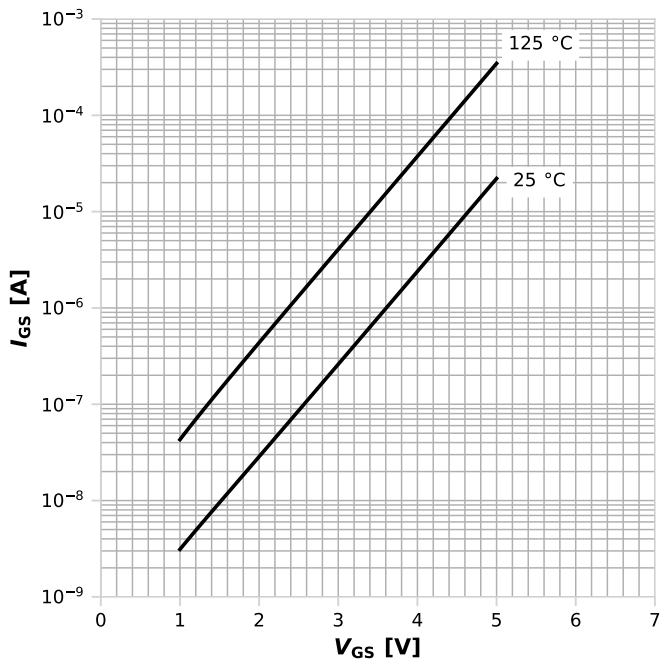
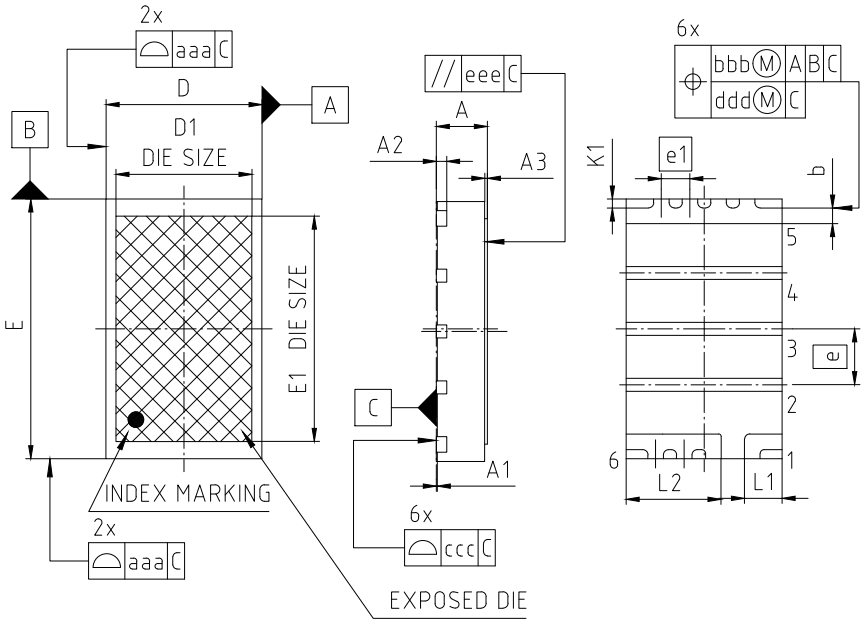
Diagram 15: Typ. output charge	Diagram 16: Typ. Coss stored Energy
	
Q_{oss}=f(V_{DS}), V_{GS}=0 V	E_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 17: Typ. gate characteristics forward



I_{GS}=f(V_{GS}); V_{DS}=0 V; parameter: T_j

6 Package outlines



PACKAGE - GROUP NUMBER:	PG-TSON-6-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	-	1.032
A1	-	0.05
A2	0.20	
A3	-	0.05
b	0.18	0.30
D	2.90	3.10
D1	2.616	
E	4.90	5.10
E1	4.336	
e	1.075	
e1	0.55	
K1	0.125	0.225
L1	0.625	0.825
L2	1.725	1.925
aaa	0.05	
bbb	0.10	
ccc	0.08	
ddd	0.05	
eee	0.10	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH,
PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSON-6, dimensions in mm

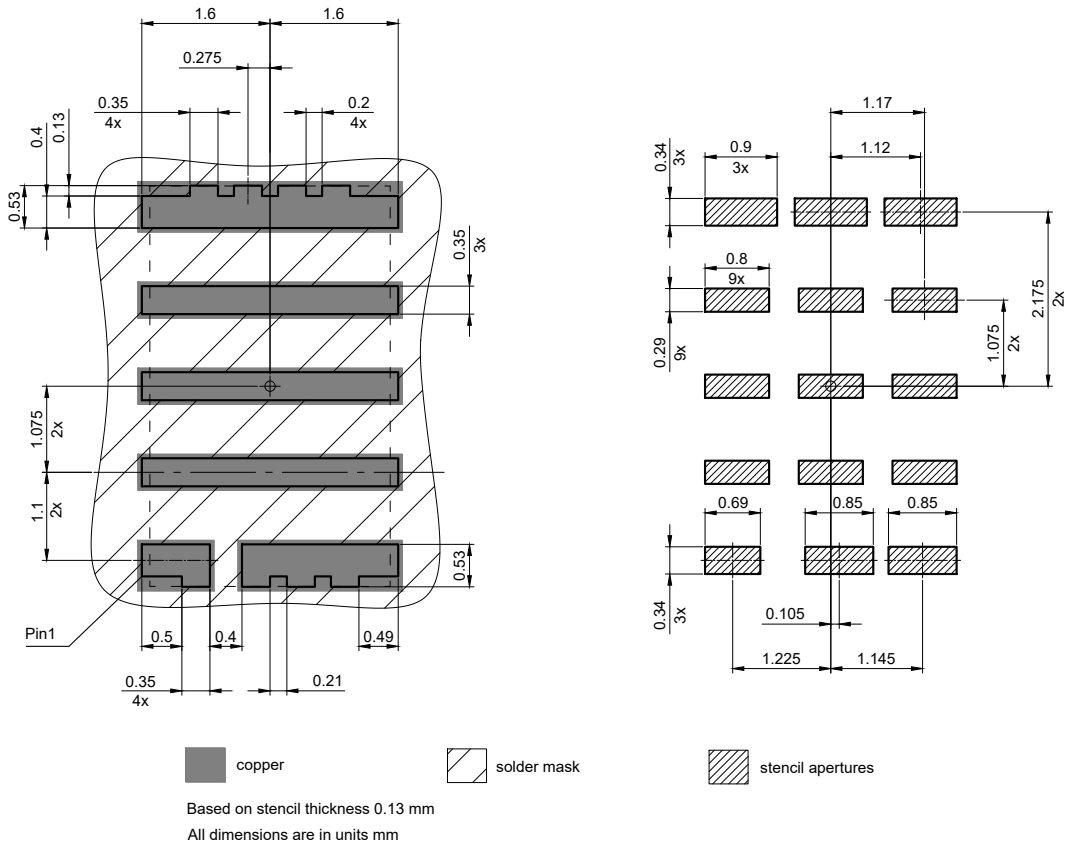


Figure 2 Footprint drawing PG-TSON-6, dimensions in mm

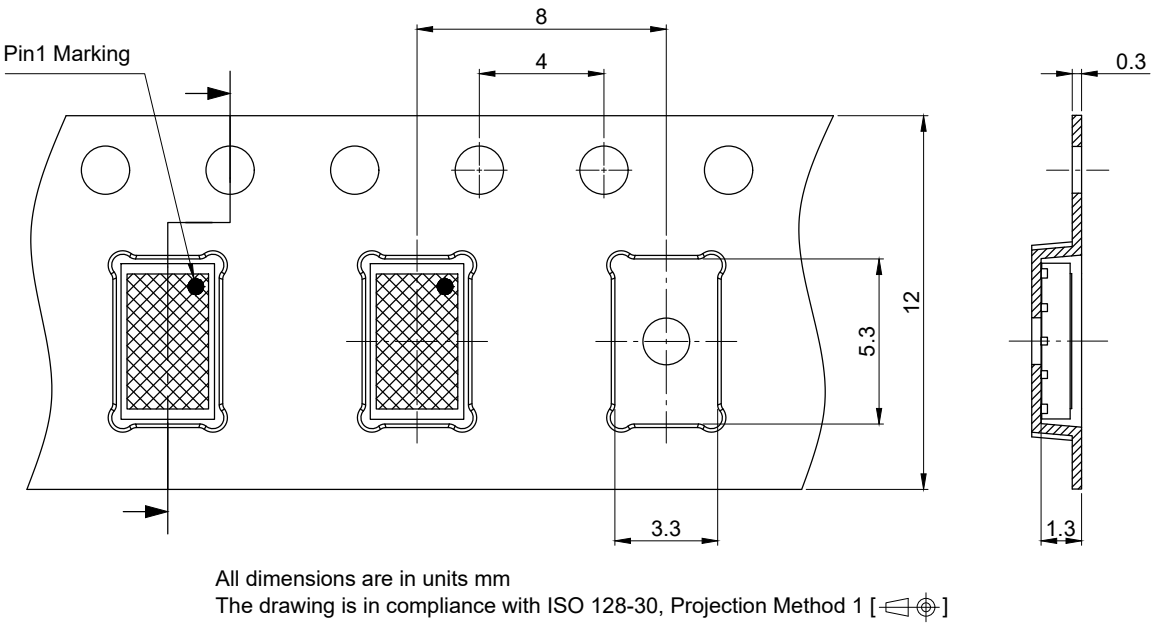


Figure 3 Packaging variant PG-TSON-6, dimensions in mm

7 Appendix A

Table 9 Related links

- IFX CoolGaN™ GaN webpage
- IFX CoolGaN™ reliability white paper
- IFX CoolGaN™ gate driver application note
- IFX CoolGaN™ Evaluation Boards
- IFX Packages Description-PG-TSON-6-2

Revision history

IGC037S12S1

Revision 2025-02-21, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-01-28	Release of final version
1.1	2025-02-21	Diagram harmonization

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Published by
Infineon Technologies AG
81726 München, Germany
© 2025 Infineon Technologies AG
All Rights Reserved.

Important notice
The products which may also include samples and may be comprised of hardware or software or both ("Product") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Product or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).