

CoolGaN™

CoolGaN™ Transistor 100 V G5 with integrated Schottky Diode

Features

- Ultra fast switching and high efficiency
- Low reverse conduction voltage
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade package

Potential applications

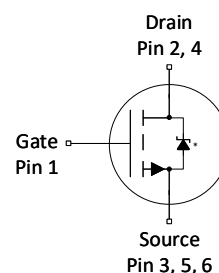
- Telecom & Datacenter
- Sync Rectification for AC-DC and DC-DC converters
- Robotics and drones
- Battery powered tools
- Servo drive
- Point of Load Converters

Product validation

Qualified according to relevant JEDEC tests.

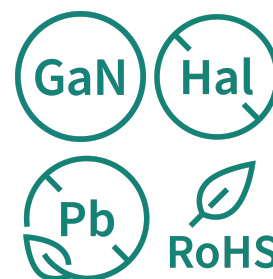
Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	1.3	mΩ
I_D	105	A
Q_{oss}	65	nC
Q_G	15	nC
Q_{rr}	0	nC
V_{SD}	0.9	V



*Top side is exposed silicon substrate,
internally connected to source terminal.
Not recommended to use as an electrical
connection.*

* Integrated Schottky diode



Part number	Package	Marking	Related links
IGC016K10S2	PG-TSON-6	16KA2	see Appendix A



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1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	$V_{GS}=0\text{ V}$
Pulsed drain-source voltage ¹⁾	$V_{DS,pulse}$	-	-	120	V	$V_{GS}=0\text{ V}$, 1 h total time
Continuous drain current	I_D	-	-	105	A	$V_{GS}=5\text{ V}$, $T_C=25\text{ °C}$
				29		$V_{GS}=5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=38\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	970	A	$T_j=25\text{ °C}$
				380		$T_j=125\text{ °C}$
Pulsed gate-source voltage	V_{GS}	-7.0	-	7.0	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	45	W	$T_C=25\text{ °C}$
				3.3		$T_A=25\text{ °C}$, $R_{thJA}=38\text{ °C/W}$ ²⁾
Storage temperature	T_{stg}	-55	-	150	°C	-
Junction temperature	T_j	-40				

¹⁾ Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

²⁾ Device on 4-layer FR4 PCB, vertical in still air.

³⁾ Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	6.0	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	0.5	0.6	°C/W	-
Thermal resistance, junction - case, bottom			1.9	2.8		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	60	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	38	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical characteristics

at $T_j=25\text{ °C}$, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	2.0	2.9	V	$V_{DS}=V_{GS}$, $I_D=12\text{ mA}$
Drain-source leakage current	I_{DSS}	-	8.0	105	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			79	1890		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	24	525	μA	$V_{GS}=5\text{ V}$, $T_j=25\text{ °C}$
			0.02	0.16		$V_{GS}=-4\text{ V}$, $T_j=25\text{ °C}$
			360	5800		$V_{GS}=5\text{ V}$, $T_j=125\text{ °C}$
			0.01	2.8		$V_{GS}=-4\text{ V}$, $T_j=125\text{ °C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3	1.6	$\text{m}\Omega$	$V_{GS}=5\text{ V}$, $I_D=30\text{ A}$
Gate resistance ⁴⁾	R_G	-	0.65	-	Ω	-

⁴⁾ Defined by design. Not subject to production test.

Table 6 Capacitance characteristics ⁵⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1700	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		750			
Reverse transfer capacitance	C_{rss}		17			

⁵⁾ Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.4	-	nC	$V_{DS}=50\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		3.5		nC	
Gate charge ⁶⁾	Q_{gd}		4.6		nC	
Switching charge	Q_{sw}		6.5		nC	
Gate charge total ⁶⁾	Q_g		15		nC	
Gate plateau voltage	$V_{plateau}$		2.6		V	
Output charge ⁶⁾	Q_{oss}	-	65	-	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁶⁾ Defined by design. Not subject to production test.

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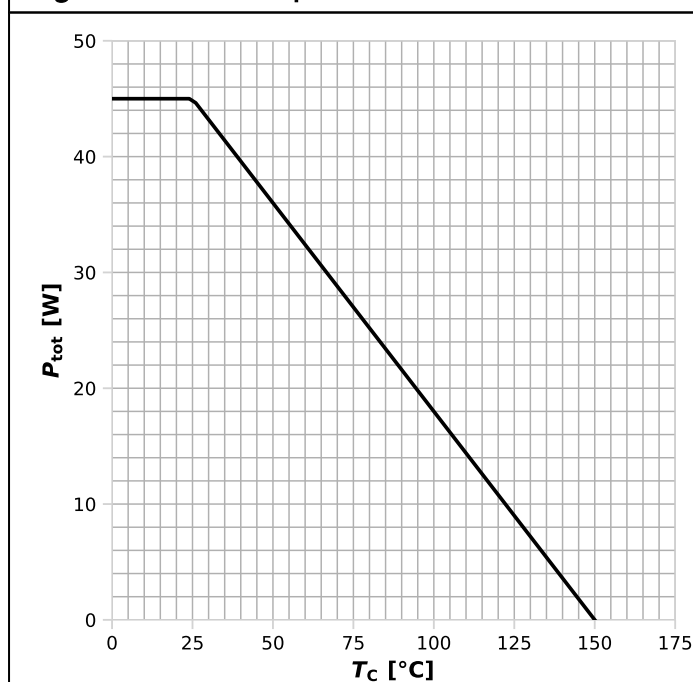

Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	32	A	$T_C = 25\text{ °C}$
Pulsed current, reverse	$I_{S,pulse}$			420		
Source-drain reverse voltage	V_{SD}	-	1.7	-	V	$V_{GS} = 0\text{ V}, I_{spulse} = 30\text{ A}, T_j = 25\text{ °C}$
			0.9			$V_{GS} = 0\text{ V}, I_{spulse} = 0.5\text{ A}, T_j = 25\text{ °C}$
Reverse recovery charge ⁷⁾	Q_{rr}	-	0	-	nC	$V_R = 50\text{ V}, I_{S,pulse} = 30\text{ A}, di_{s,pulse}/dt = 100\text{ A/us}$

⁷⁾ Defined by design. Not subject to production test.

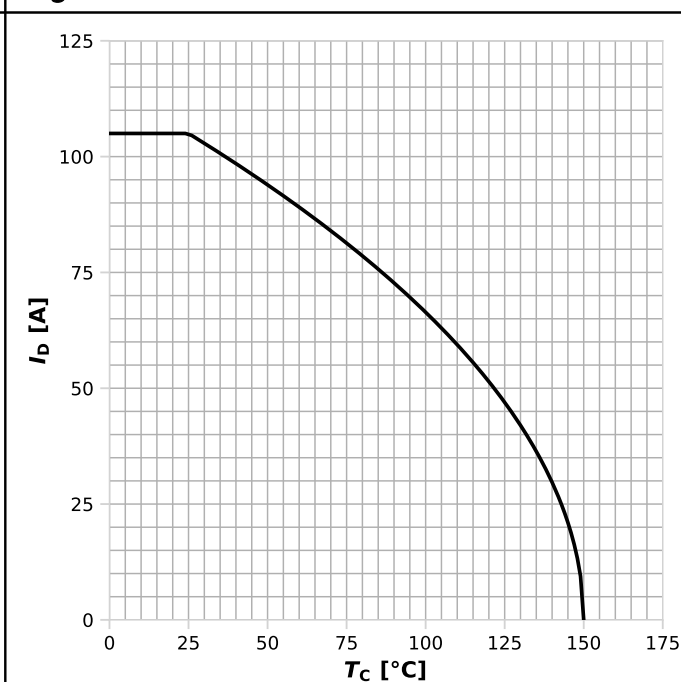
5 Electrical characteristics diagrams

Diagram 1: Power Dissipation



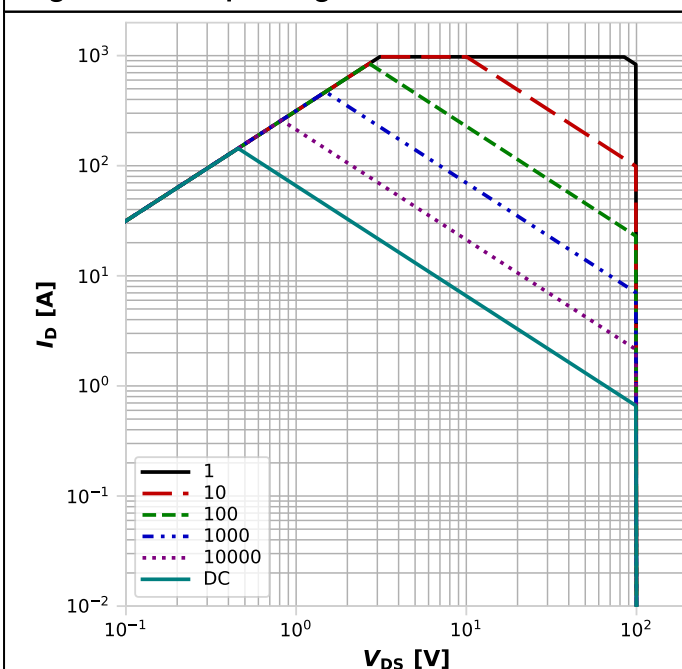
$$P_{tot}=f(T_c)$$

Diagram 2: Drain Current



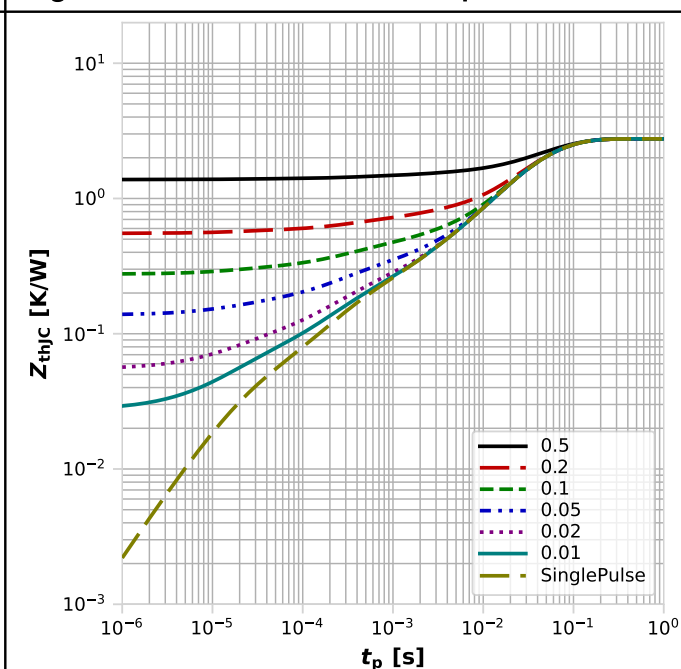
$$I_D=f(T_c)$$

Diagram 3: Safe Operating Area



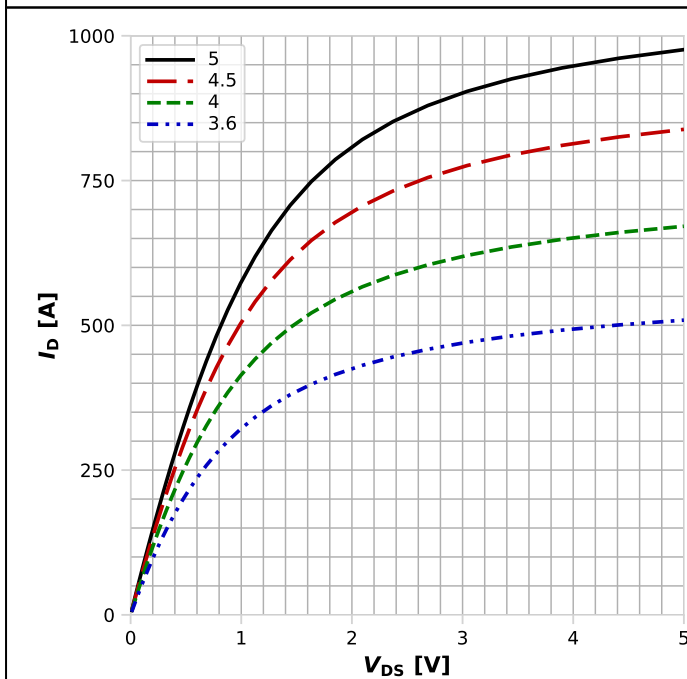
$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p [\mu s]$$

Diagram 4: Max. transient thermal impedance



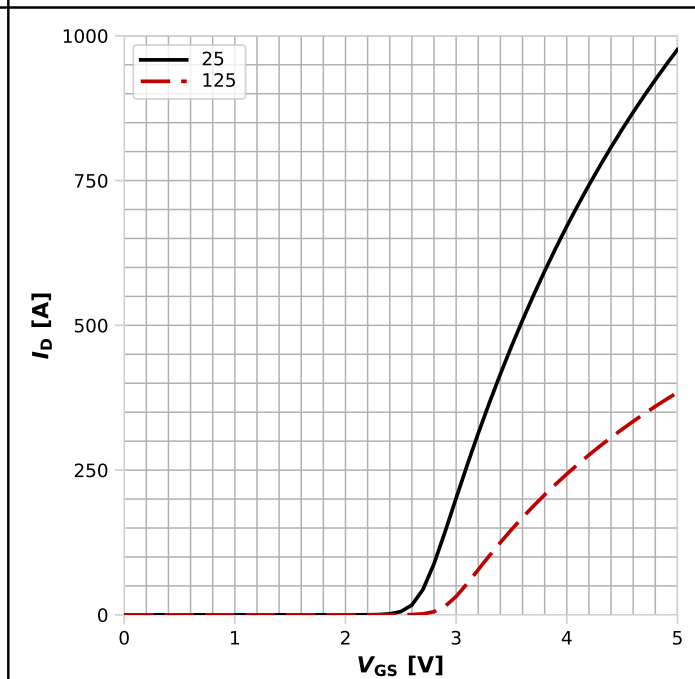
$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics



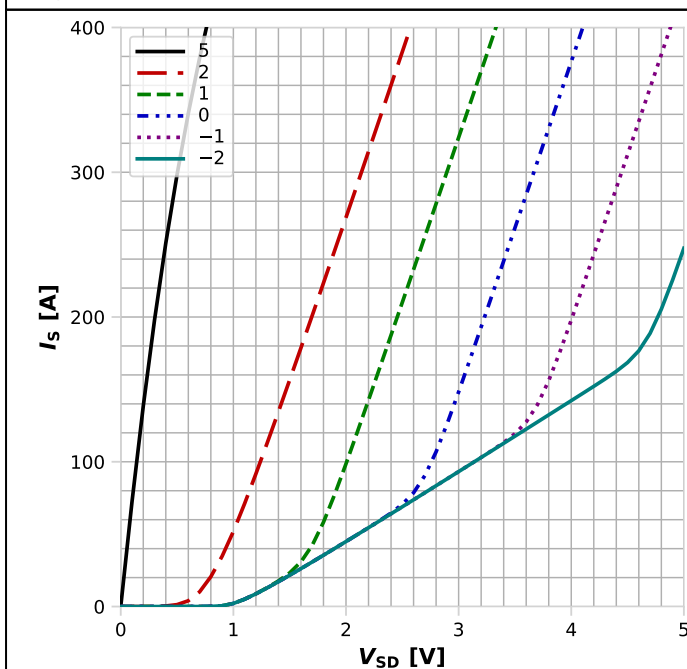
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS} [V]

Diagram 6: Typ. transfer characteristics



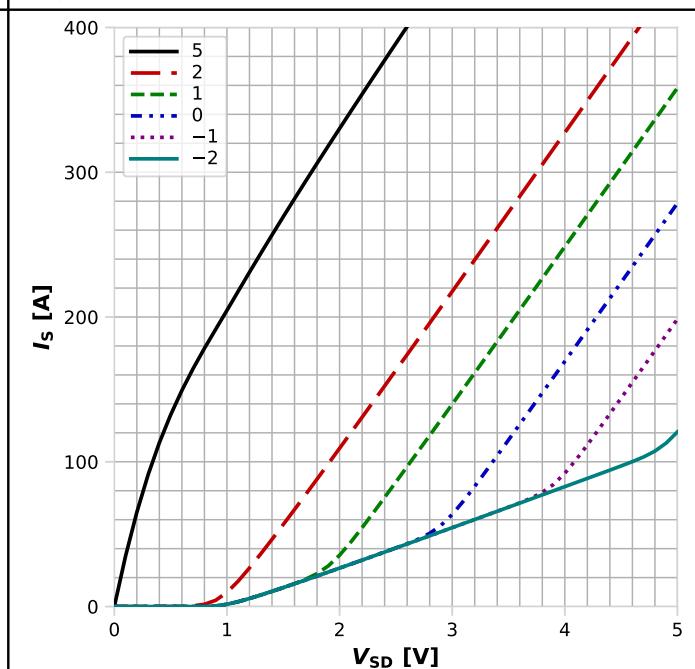
$I_D = f(V_{GS})$ | $V_{DS} > 2|I_D|R_{DS(on)max}$; parameter: T_j [$^\circ\text{C}$]

Diagram 7: Typ. reverse output characteristics



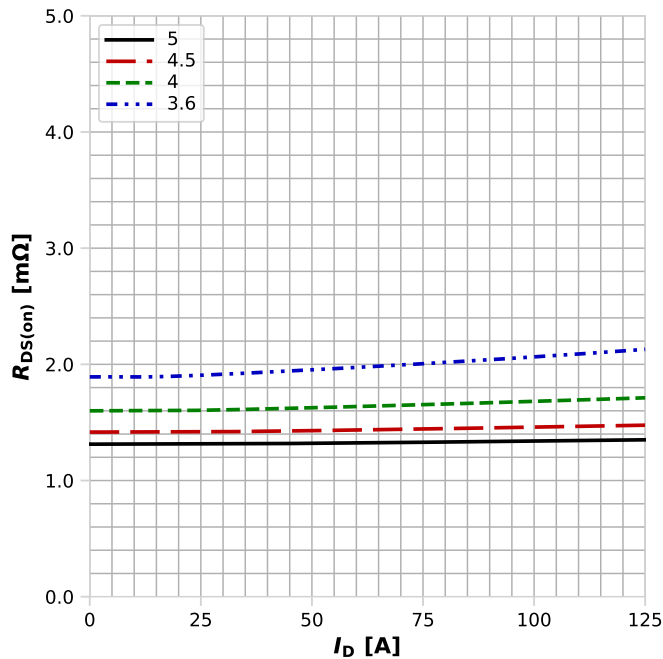
$I_S = f(V_{SD})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS} [V]

Diagram 8: Typ. reverse output characteristics



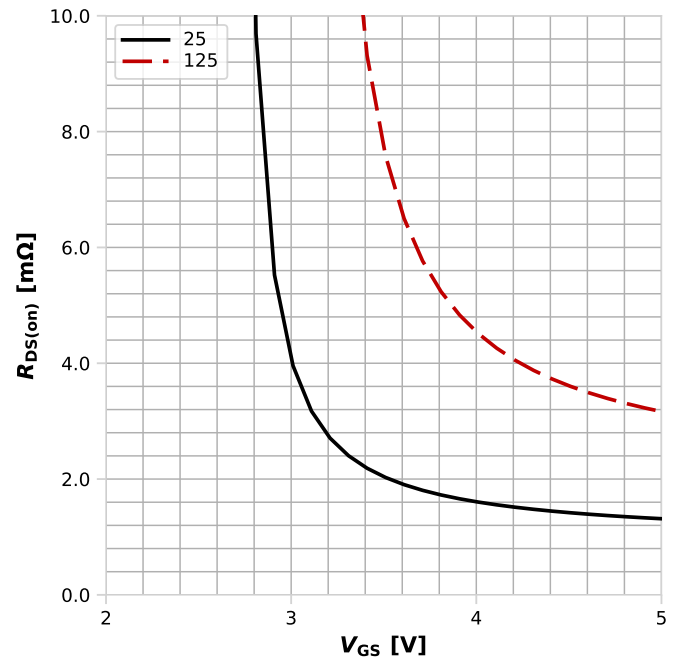
$I_S = f(V_{SD})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS} [V]

Diagram 9: Typ. drain-source on resistance



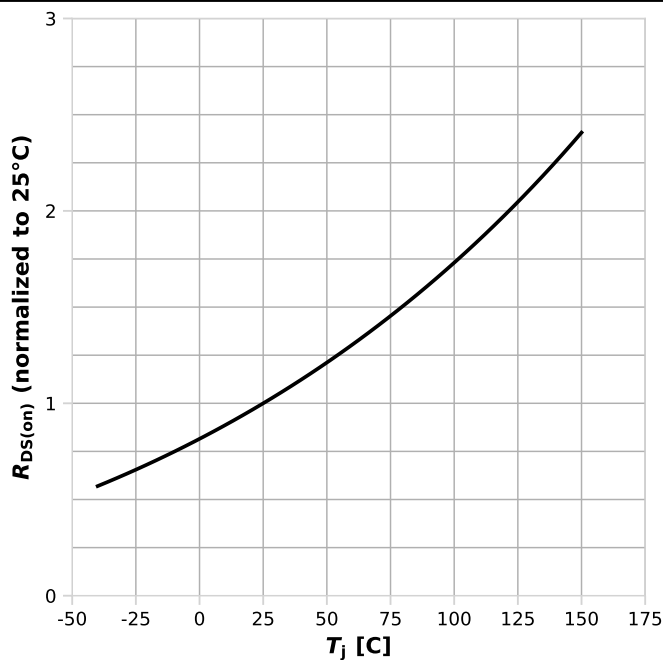
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS} [V]$$

Diagram 10: Typ. drain-source on resistance



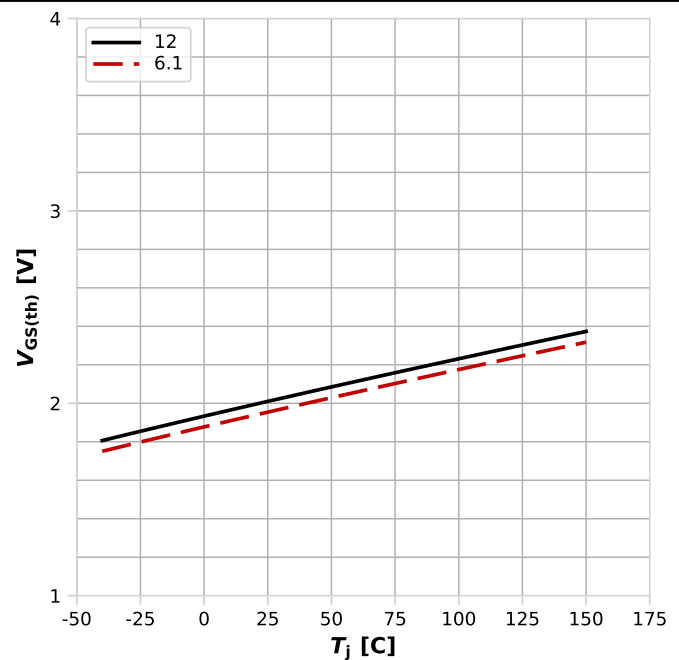
$$R_{DS(on)} = f(V_{GS}); I_D = 30 \text{ A}; \text{parameter: } T_j [^\circ\text{C}]$$

Diagram 11: Drain-source on-state resistance



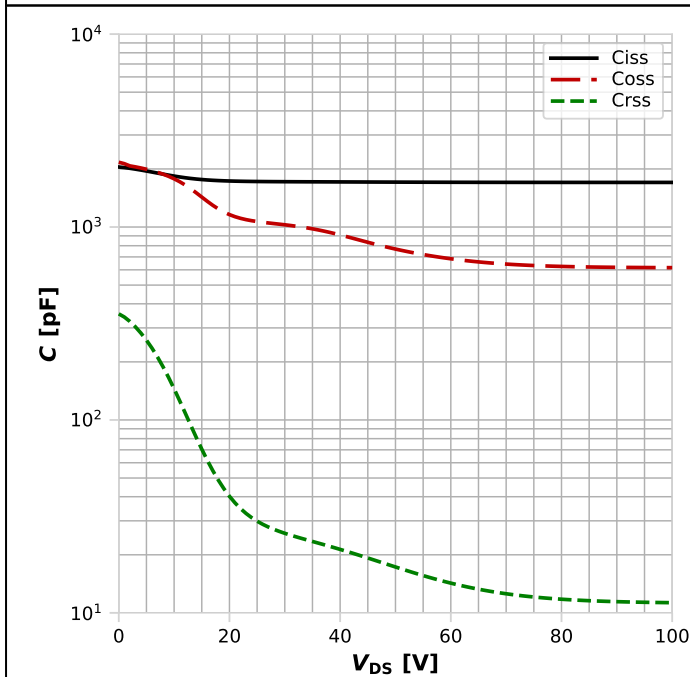
$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 5 \text{ V}$$

Diagram 12: Typ. gate threshold voltage



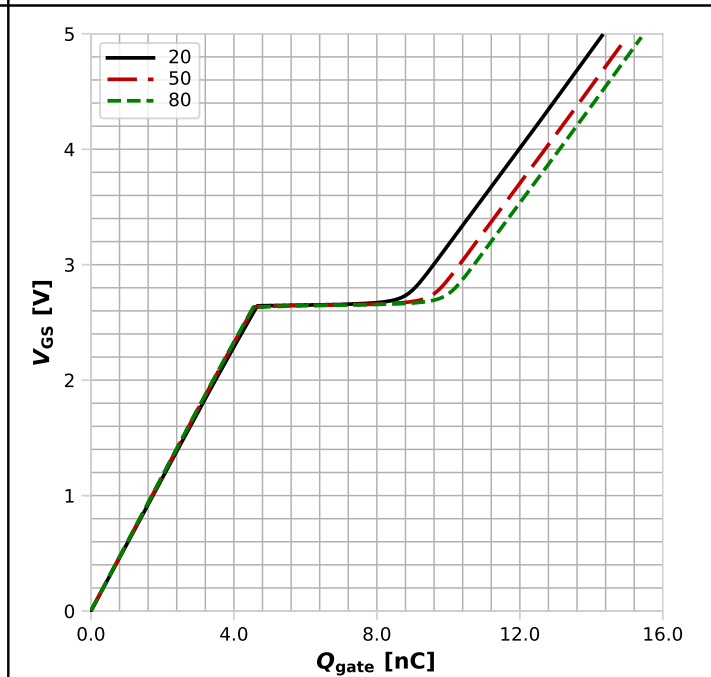
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; \text{parameter: } I_D [mA]$$

Diagram 13: Typ. capacitances



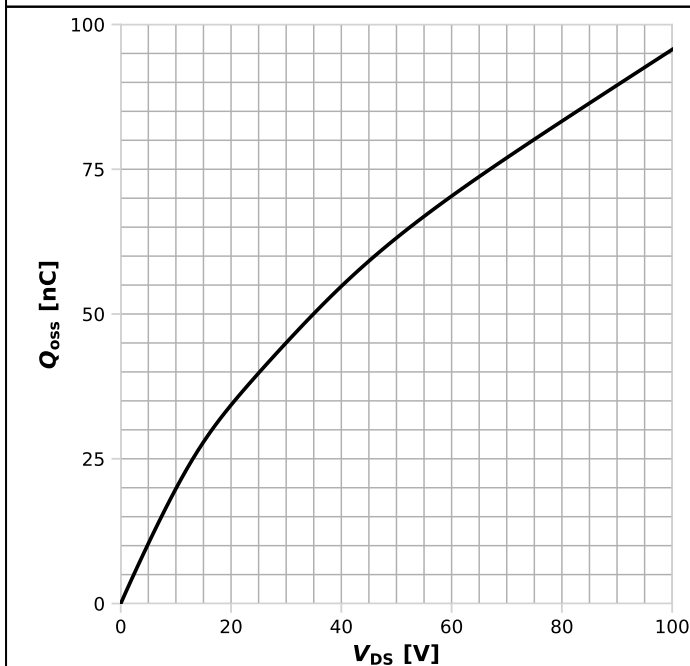
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 14: Typ. gate charge



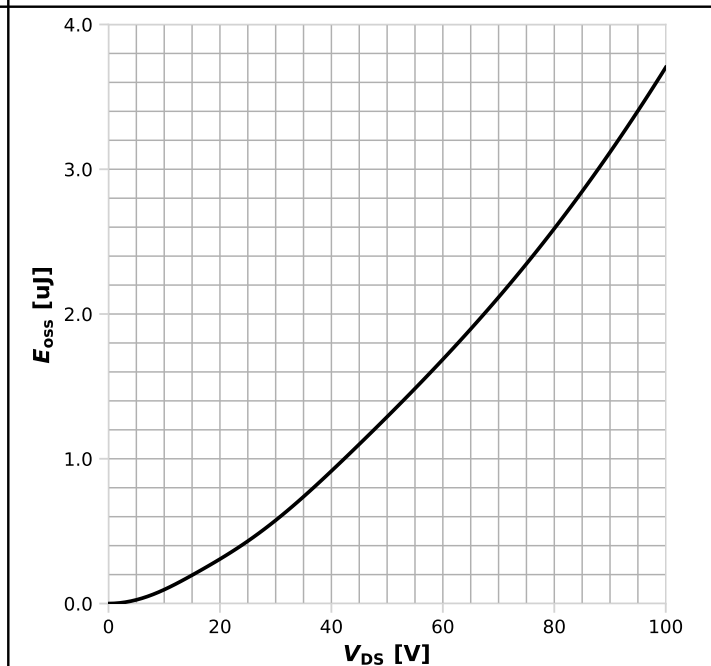
$V_{GS}=f(Q_{gate}); I_D=30\text{ A pulsed}; \text{parameter: } V_{DS}\text{ [V]}$

Diagram 15: Typ. output charge



$Q_{oss}=f(V_{DS}); V_{GS}=0\text{ V}$

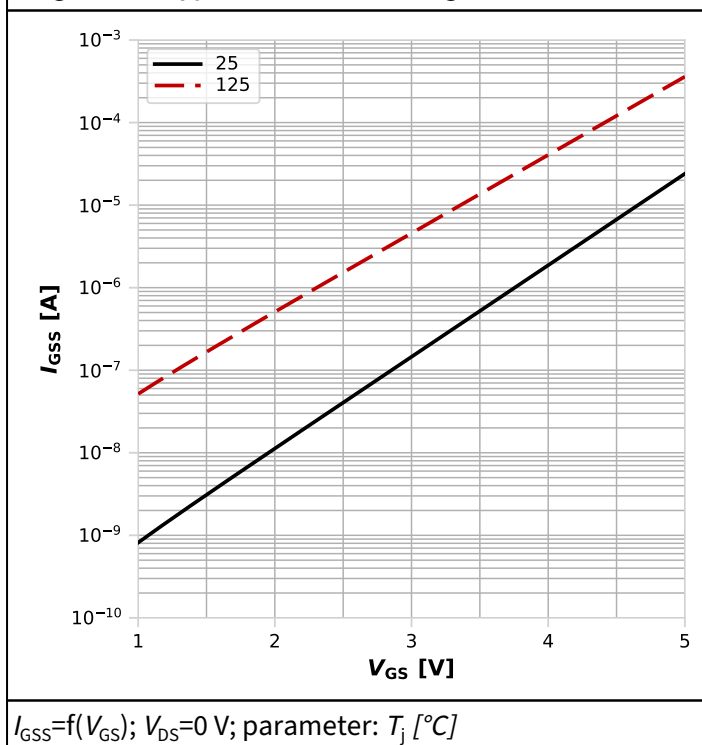
Diagram 16: Typ. output energy



$E_{oss}=f(V_{DS}); V_{GS}=0\text{ V}$

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Diagram 17: Typ. Gate-source leakage current



6 Package outlines

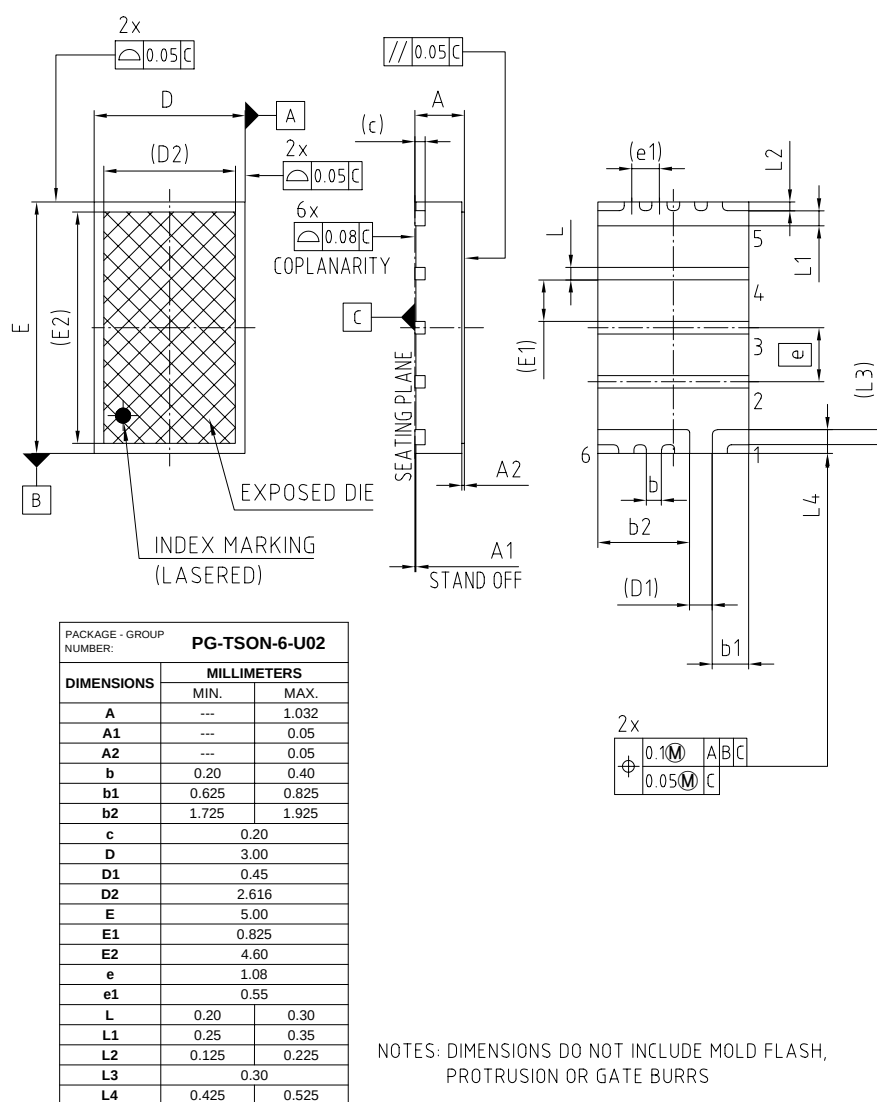
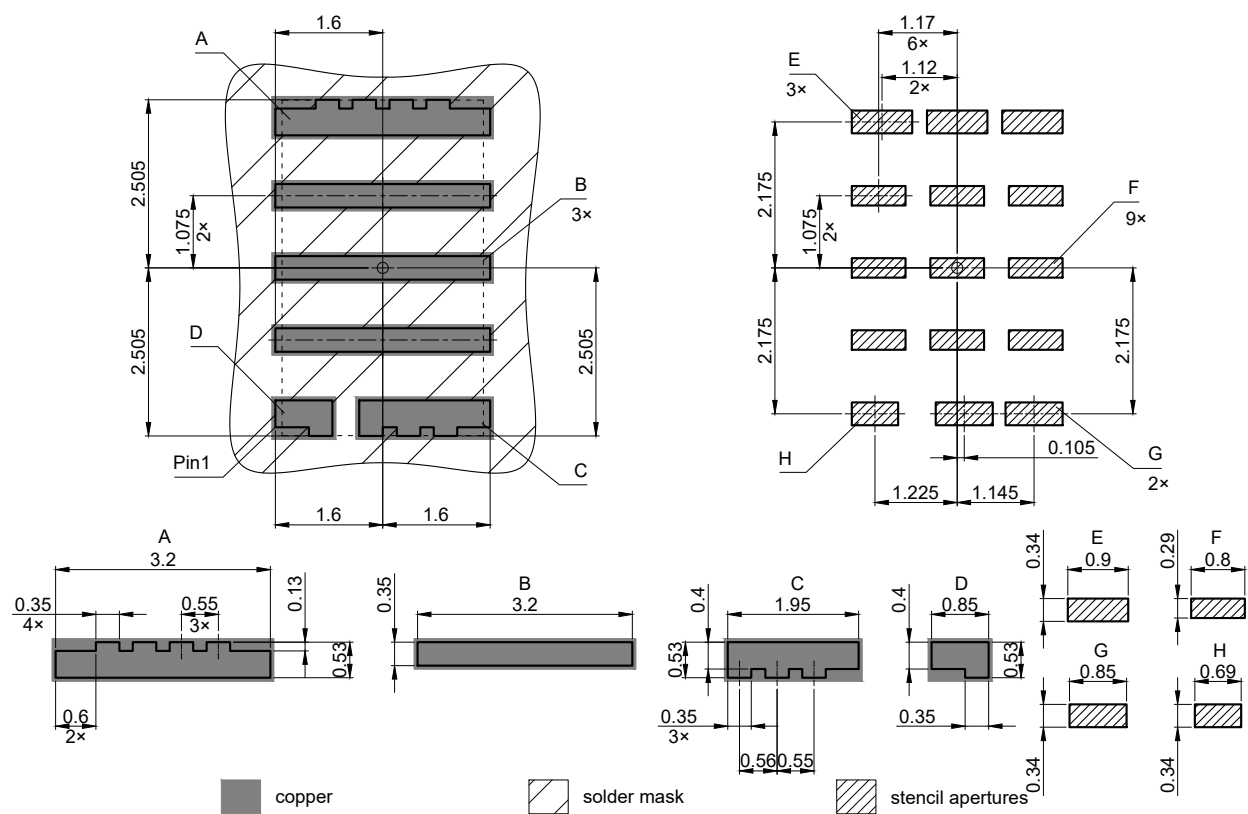


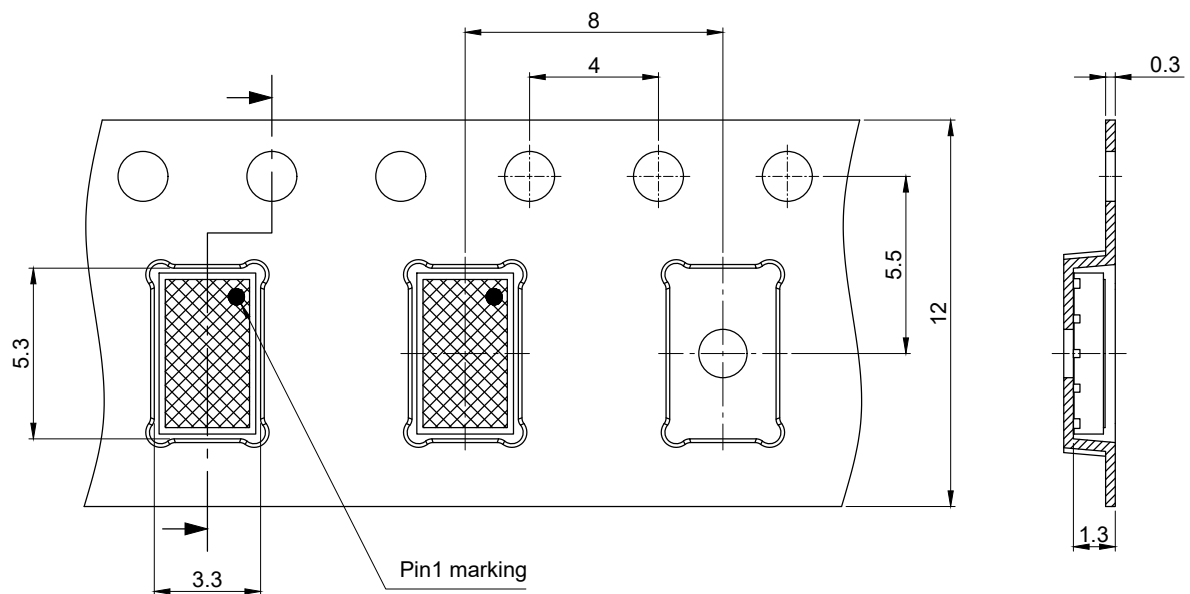
Figure 1 Outline PG-TSON-6, dimensions in mm

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All dimensions are in units mm
Based on stencil thickness 0.13 mm
All pads are solder mask defined

Figure 2 Footprint drawing PG-TSON-6, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-TSON-6, dimensions in mm

7 Appendix A

Table 9 **Related links**

- [IFX CoolGaN™ GaN webpage](#)
- [IFX CoolGaN™ reliability white paper](#)
- [IFX CoolGaN™ gate driver application note](#)
- [IFX CoolGaN™ Evaluation Boards](#)
- [IFX Packages](#)

CoolGaN™ Transistor 100 V G5 with integrated Schottky Diode IGC016K10S2



Revision history

IGC016K10S2

Revision 2026-09-18, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-09-16	Release of final version
1.1	2026-09-18	Public final version

CoolGaN™ Transistor 100 V G5

with integrated Schottky Diode

IGC016K10S2



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