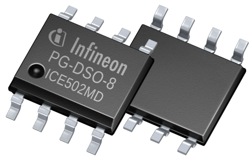
Features

- Selectable gate voltage 10 V, 15 V and 18 V for driving external power MOSFET
- Comprehensive protections, including input line overvoltage protection
- Fast startup by VCC charging via external CoolSiC™ / CoolMOS™
- Integrated soft-start to minimize component stress during startup
- Integrated error amplifier to support direct sense for non-isolated design
- Enhanced active burst mode for low standby power
- Frequency reduction for improved average efficiency
- Frequency jitter for low EMI
- CCM slope compensation
- Pb-free lead plating, halogen-free mold compound, RoHS compliant



RoHS
Green
Halogen-free
Lead-free

Potential applications

- Auxiliary power supply for 1-ph and 3-ph systems, e.g. solar inverter, energy storage, EV-charger, UPS, motor drives and consumer product.

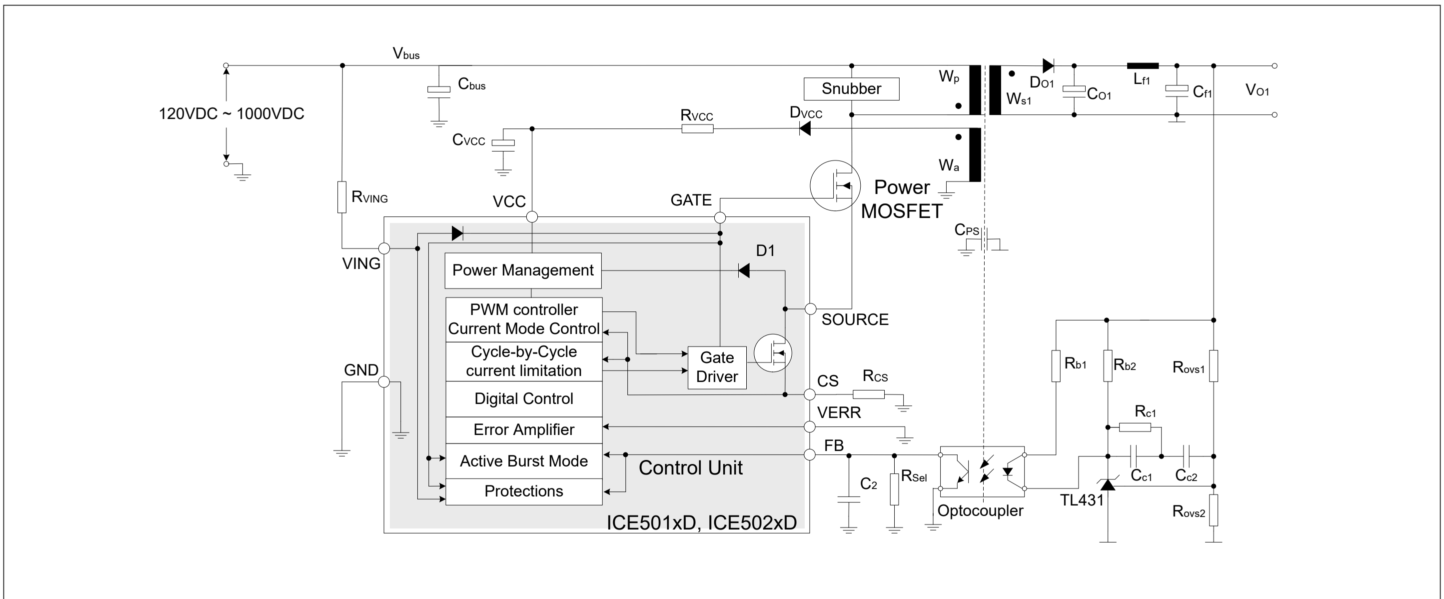
Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

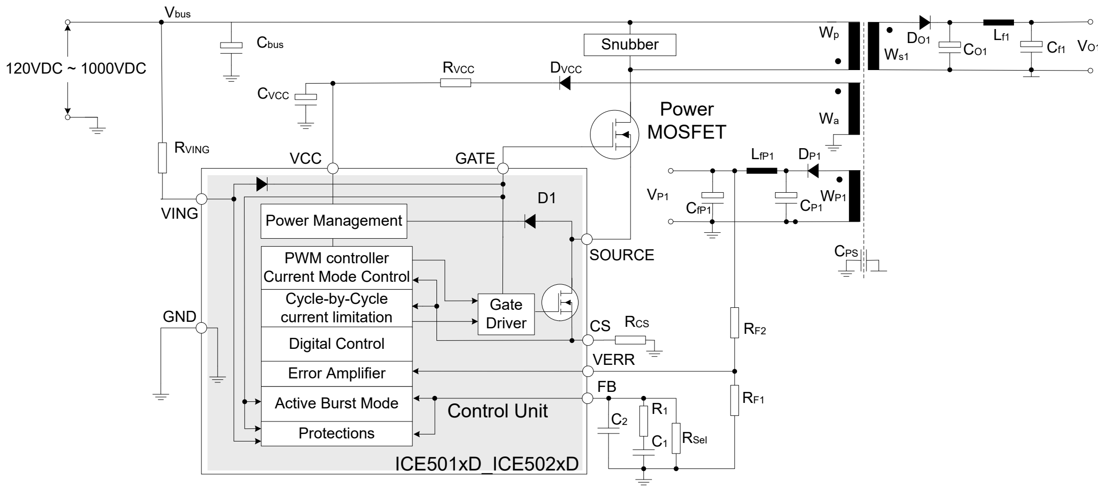
Description

The ICE501XD & ICE502XD CoolSET™ PWM FF Gen5 Pro are the latest 5th Generation Fixed Frequency PWM controller optimized for off-line switch mode power supply in cascode configuration and configurable gate clamp voltage for driving CoolSiC™ or CoolMOS™ MOSFET. The cascode configuration helps to achieve a fast startup time and avoid lossy startup resistor. The frequency reduction with frequency jitter operation offers low EMI and better efficiency across the load range. The product has a wide operating range (12.5 V ~ 29 V) of IC power supply and lower power consumption. The numerous protection functions together with line overvoltage protection can make the power supply system operate in a robust condition. All these make the PWM FF Gen5 Pro an outstanding PWM controller for fixed frequency flyback converter in the market.

Typical application circuit



Typical application in isolated fixed-frequency flyback converter



Typical application in non-isolated flyback utilizing integrated error amplifier

Output power of the ICE501xD and ICE502xD

Table 1 Output power of the ICE501xD and ICE502xD

Type	Package	Marking	fsw	85 V AC ~ 440 V AC[1]	200 V DC ~ 1000 V DC[2]
ICE501LD	PG-DSO-8	501L	65 kHz	70 W	79 W
ICE501MD	PG-DSO-8	501M	100 kHz	70 W	79 W
ICE502LD	PG-DSO-8	502L	65 kHz	105 W	114 W
ICE502MD	PG-DSO-8	502M	100 kHz	105 W	114 W

1. Calculated maximum output power rating in an open frame design at $T_a = 50°C$, $T_J = 125°C$ using minimum pin copper area in a 2 oz copper single sided PCB. The output power figure is for selection purpose only and vary based on ambient temperature - see section 5 for more details. The actual power can vary depending on particular designs. Please contact to a technical expert from Infineon for more information.

2. Calculated maximum output power rating in an open frame design at $T_a = 85°C$, $T_J = 125°C$ using minimum pin copper area in a 2 oz copper single sided PCB. The output power figure is for selection purpose only and vary based on ambient temperature - see section 5 for more details. The actual power can vary depending on particular designs. Please contact to a technical expert from Infineon for more information.

Table of contents

1 Pin configuration and functionality

The pin configuration is shown below and the functions are described in Table 3.

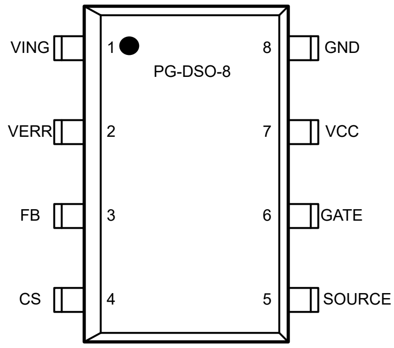


Figure 1 Pin configuration

Table 3 Pin definition and function

Pin	Symbol	Function
1	VING	**Input line overvoltage protection and startup** The pin is connected to the start up circuit internally. Once the VCC voltage reaches the startup threshold, the IC starts switching from soft start. The VING pin is connected to the bus via resistor (see Typical application circuit) to sense the line condition for protection. When the input voltage exceeds the maximum input voltage, the gate switching stops enters line OVP protection.
2	VERR	**Error amplifier** The VERR pin is internally connected to the transconductance error amplifier for non-isolated flyback application. Connect this pin to GND for isolated flyback application.
3	FB	**Feedback and ABM entry/exit control** The FB pin combines the functions of feedback control, burst entry/exit control, overload/open loop protection and selectable GATE voltage option.
4	CS	**Current sense** The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.
5	SOURCE	**SOURCE** The SOURCE pin is connected to the source of external power MOSFET which is in series connection with internal low side MOSFET and VCC charging diode.
6	GATE	**Gate driver output** The GATE pin is connected to the gate pin of the power MOSFET to control the on/off of the MOSFET.

(table continues...)

Table 3 (continued) Pin definition and function

Pin	Symbol	Function
7	VCC	**VCC (Positive voltage supply)** The VCC pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	GND	**Ground** The GND pin is the common ground of the controller.

2 Representative block diagram

***Note**: Junction temperature of the controller chip is sensed for overtemperature protection.*

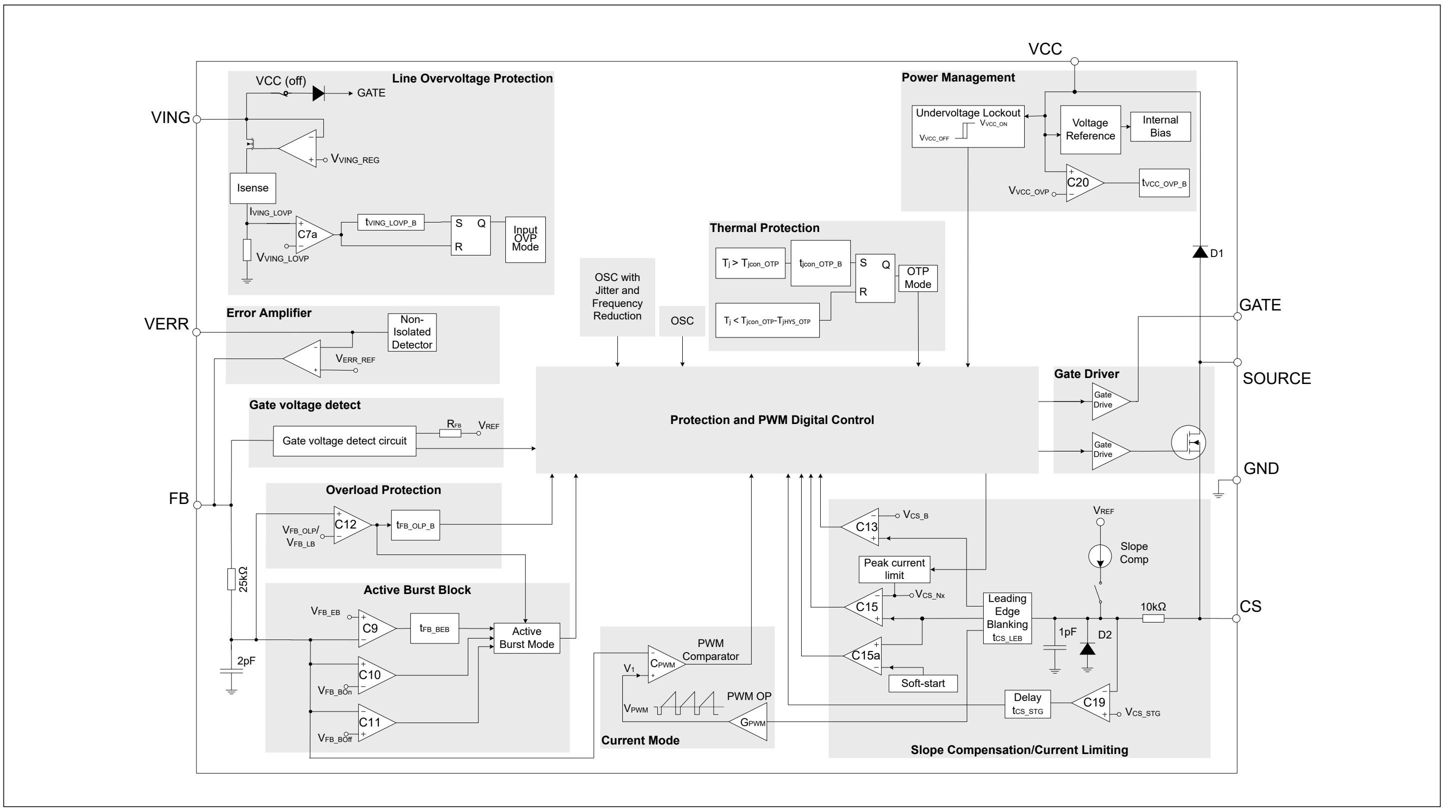


Figure 2 **Representative block diagram**

3 Functional description

3.1 VCC pre-charging and typical VCC voltage during start-up

As shown in the Typical application circuit, once the line input voltage is applied to the capacitor C_{BUS}, the pull-up resistor (R_{VING}) at VING pin provides a current to pull up the gate of the external power MOSFET. When the voltage at the gate of power MOSFET is higher than the gate turn on threshold, the VCC capacitor starts to be charged by the V_{BUS} voltage through the internal diode D_1 with the three steps constant current source $I_{VCC\_Charge1}$[1], $I_{VCC\_Charge2}$[1] and $I_{VCC\_Charge3}$[1]. The constant current is maintained by varying the gate voltage. A very small constant current source ($I_{VCC\_Charge1}$) is charged to the VCC capacitor until VCC reaches V_{VCC_SCP} to protect the controller from the VCC pin short to ground during the startup. After that, the second and third steps constant current source are provided to charge the VCC capacitor further until the VCC voltage exceeds the turned-on threshold V_{VCC_ON}. As shown in the time phase I in Figure 3, the VCC voltage increases almost linearly with three steps. The adopted startup method runs at the linear mode of the external MOSFET for typical 200 ms with 22 µF (recommended) VCC capacitor (pls refer to the design guide for more details).

1. $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during startup.
2. I_{VCC_Normal} is supply current from VCC capacitor or auxiliary winding to the controller during normal operation.

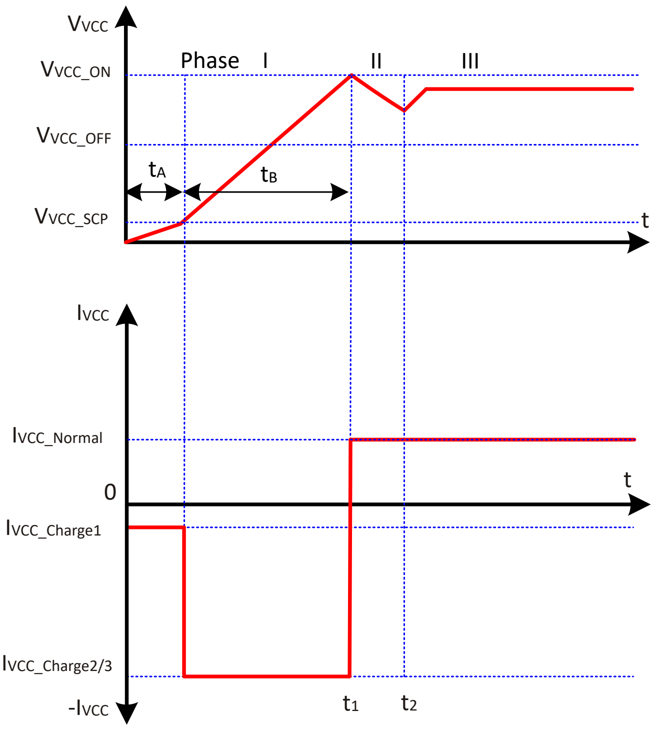


Figure 3 VCC voltage and current during start up

The time for the *V*CC pre-charging can then be calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \times C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \times C_{VCC}}{(I_{VCC\_Charge2} + I_{VCC\_Charge3})/2} \quad (1)$$

When the VCC voltage exceeds the VCC turn on threshold V_{VCC_ON} at time t_1, the IC starts to operate with soft start. Due to the power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the VCC capacitor before the output voltage is built up, the VCC voltage drops (phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the VCC capacitor from the time t_2 onward and delivering the $I_{VCC\_ Normal}$ to the controller. VCC then reaches a constant value depending on the output load.

3.2 Soft-start

As shown in the figure below, the IC begins to operate with a soft-start at time t_{on}. The switching stresses on the power MOSFET, diode and transformer are minimized during soft-start. The soft-start implemented in PWM FF Gen5 Pro is a digital time-based function. The preset soft-start time is t_{SS} (12 ms) with four steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to V_{CS_N} finally. The normal feedback loop will take over the control when the output voltage reaches its regulated value.

The frequency for the first 3 ms is $f_{OSC\_X\_MIN}$ in order to minimize current spikes due to CCM during start-up. After the first 3 ms, the switching frequency changes to f_{OSC_X} for the remaining duration of soft start.

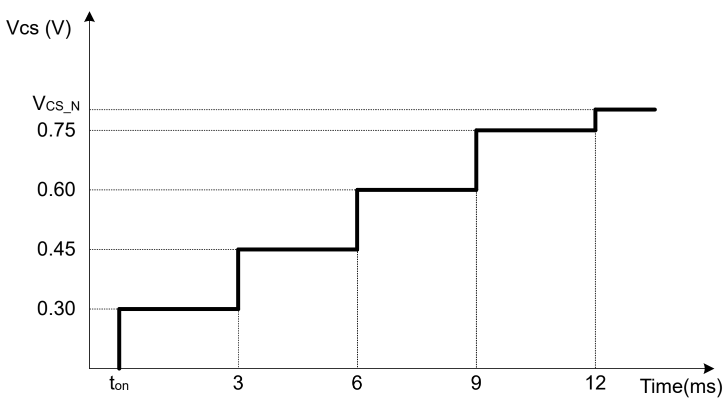


Figure 4 Maximum current sense voltage during soft start

3.3 Normal operation

The PWM controller during normal operation consists of a digital signal processing circuit including regulation control and an analog circuit including a current measurement unit and a comparator. Details about the full operation of the PWM FF Gen5 Pro controller in normal operation are illustrated in the following paragraphs.

3.3.1 PWM operation and peak current mode control

3.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator with a switching frequency f_{SW} that corresponds to the voltage level V_{FB}.

3.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage V_1 (see Figure 2) which is the representation of the instantaneous current of the power MOSFET. When V_1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the GATE of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the feedback voltage V_{FB}.

At switch on transient of the power MOSFET, a voltage spike across R_{CS} can cause V_1 to increase and exceed V_{FB}. To avoid a false switch off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn on time of the power MOSFET is t_{CS_LEB}.

For some reason that the voltage level at V_1 takes long time to exceed V_{FB}, the IC has implemented a maximum duty cycle control to force the power MOSFET to switch off when D_{MAX} = 0.75 is reached.

3.3.2 Current sense

The power MOSFET current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then, added with an offset V_{PWM} to become V_1 as described below in below equation.

$$V_{CS} = I_D \times R_{CS} \tag{2}$$

$$V_1 = V_{CS} \times G_{PWM} + V_{PWM} \tag{3}$$

where,

I_D : power MOSFET current
V_{CS} : CS pin voltage
R_{CS} : resistance of the current sense resistor
V_1 : voltage level compared to V_{FB} as described
G_{PWM} : PWM-OP gain
V_{PWM} : offset for voltage ramp

3.3.3 Frequency reduction

Frequency reduction is implemented in PWM FF Gen5 Pro to achieve a better efficiency during the light load.

At light load, the reduced switching frequency f_{SW} improves efficiency by reducing the switching losses.

When the load decreases, V_{FB} decreases as well. f_{SW} is dependent on the V_{FB} as shown in Figure 5. Therefore, f_{SW} decreases as the load decreases before entering the burst mode.

For example, f_{SW} at full load is f_{OSC_M} and it starts to decrease at V_{FB} = 1.7 V. There is no further frequency reduction once it reaches the $f_{OSC\_M\_MIN}$ even the load is further reduced.

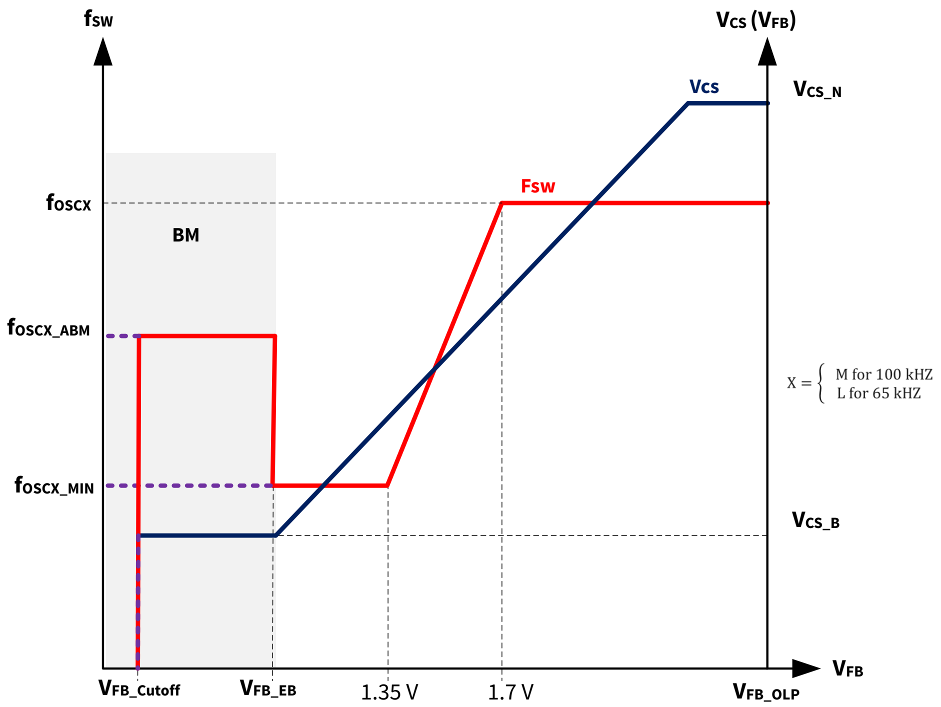


Figure 5 **Frequency reduction curve**

3.3.4 Slope compensation

PWM FF Gen5 Pro can operate at Continuous Conduction Mode (CCM). At CCM operation, duty cycle greater than 50% would cause a sub-harmonic oscillation. To avoid the sub-harmonic oscillation, slope compensation is added to V_{CS} pin when the turn on duty cycle is more than 40% of the switching period. The relationship between V_1 and the V_{CS} for CCM operation is described in below equation (refer to Figure 2):

$$V_1 = V_{CS} \times G_{PWM} + V_{PWM} + M_{COMP} \times (t_{ON} - 40\,\% \times t_{PERIOD}) \quad (4)$$

where,

M_{COMP} : slope compensation rate

t_{ON} : gate turn on time of the power MOSFET

t_{PERIOD} : switching cycle period

Slope compensation circuit is disabled and no slope compensation is added into the V_{CS} pin during active burst mode to save the power consumption.

3.3.5 Oscillator and frequency jittering

The oscillator generates a frequency f_{OSC} with frequency jittering range of f_{JITTER} at a jittering period of t_{JITTER}. The frequency jittering helps to reduce conducted EMI.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

3.4 Peak current limitation

There is a cycle by cycle peak current limitation realized by the current limit comparator to provide primary over-current protection. The primary current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

$$I_{PEAK\_PRI} = \frac{V_{CS\_N}}{R_{CS}} \tag{5}$$

To avoid mistriggering caused by MOSFET switch on transient voltage spikes, a leading edge blanking time (t_{CS_LEB}) is integrated in the current sensing path.

3.4.1 Propagation delay compensation

In case of overcurrent detection, there is always a propagation delay from sensing the V_{CS} to switching the power MOSFET off. An overshoot on the peak current *I*peak caused by the delay depends on the ratio of *d*I/*d*t of the primary current.

The overshoot of $Signal_2$ is larger than $Signal_1$ due to the steeper rising waveform. This change in the slope depends on the input voltage. Propagation delay compensation is integrated to reduce the overshoot due to *d*I/*d*t of the rising primary current. Thus the propagation delay time between the time exceeding the current sense threshold V_{CS_N} and the switching off of the power MOSFET is compensated over wide bus voltage range. Current limiting becomes more accurate which results in smaller difference of overload protection triggering power between low and high line input voltage.

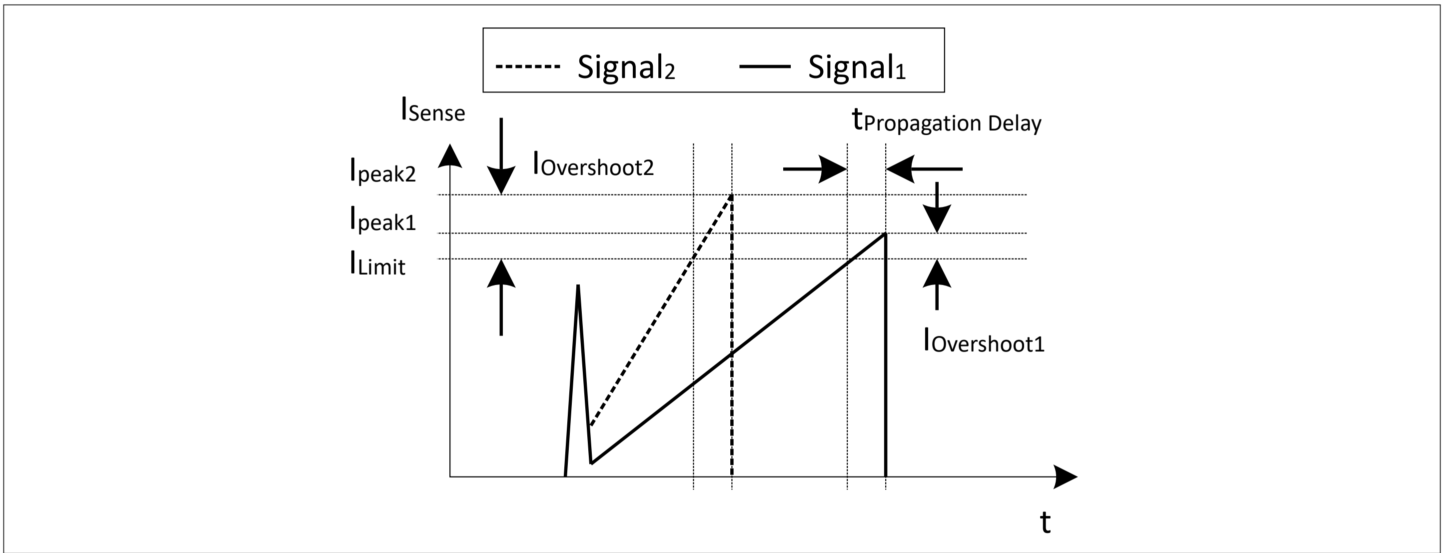


Figure 6 **Current limiting**

Under CCM operation, the same V_{CS} does not result in the same power. In order to achieve a close overload triggering level for CCM, PWM FF Gen5 Pro has implemented two different compensation curves as shown Figure 7. One of the curve is used for t_{ON} greater than 40% duty cycle and the other is for lower than 40% duty cycle.

Similarly, the same concept of propagation delay compensation is also implemented in active burst mode (ABM) with reduced level. With this implementation, the entry and exit burst mode power can be close between low and high AC line input voltage.

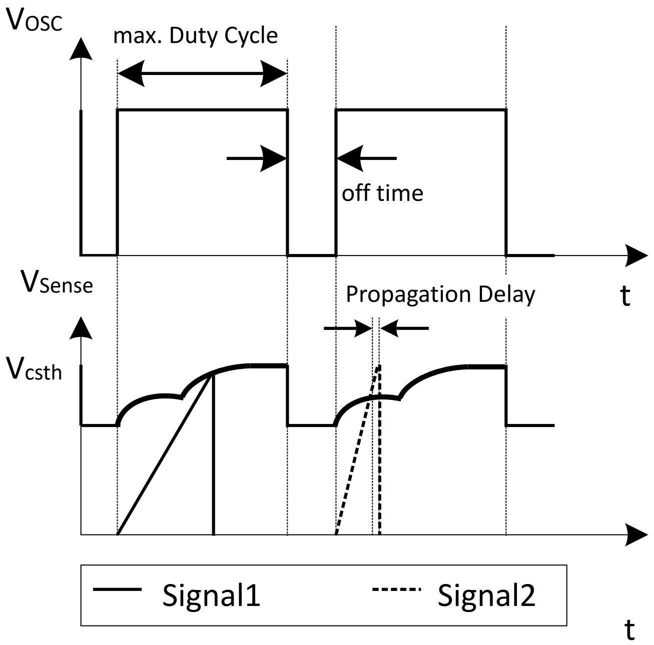


Figure 7 **Dynamic voltage threshold V_{CS_N}**

3.5 Active burst mode (ABM)

At light load condition, the IC enters ABM operation to minimize the power consumption. Details about ABM operation are explained in the following paragraphs.

3.5.1 Entering ABM operation

The system will enter into ABM operation when the below two conditions are met:

- when the FB voltage is lower than the threshold of V_{FB_EB}
- and after the blanking time t_{FB_BEB}

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of entering ABM operation, so that the controller enters ABM operation only when the output power is really low.

3.5.2 During ABM operation

After entering ABM, the PWM section will be inactive making the V_{OUT} start to decrease. As the V_{OUT} decreases, V_{FB} rises. Once V_{FB} exceeds V_{FB_BOn}, the internal circuit is again activated by the internal bias to start with the switching.

If the PWM is still operating and the output load is still low, V_{OUT} increases and V_{FB} signal starts to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again and the PWM section is disabled with no switching until V_{FB} increases back to exceed V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn} shown in Figure 8.

During ABM, the switching frequency is $f_{OSC\_X\_ABM}$. The peak current I_{PEAK_ABM} of the power MOSFET is defined by:

$$I_{PEAK\_ABM} = \frac{V_{CS\_B}}{R_{CS}} \tag{6}$$

where V_{CS_B} is the peak current limitation in ABM.

3.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When V_{FB} exceeds V_{FB_LB}, it will leave ABM and the peak current limitation threshold voltage will return back to V_{CS_N} immediately.

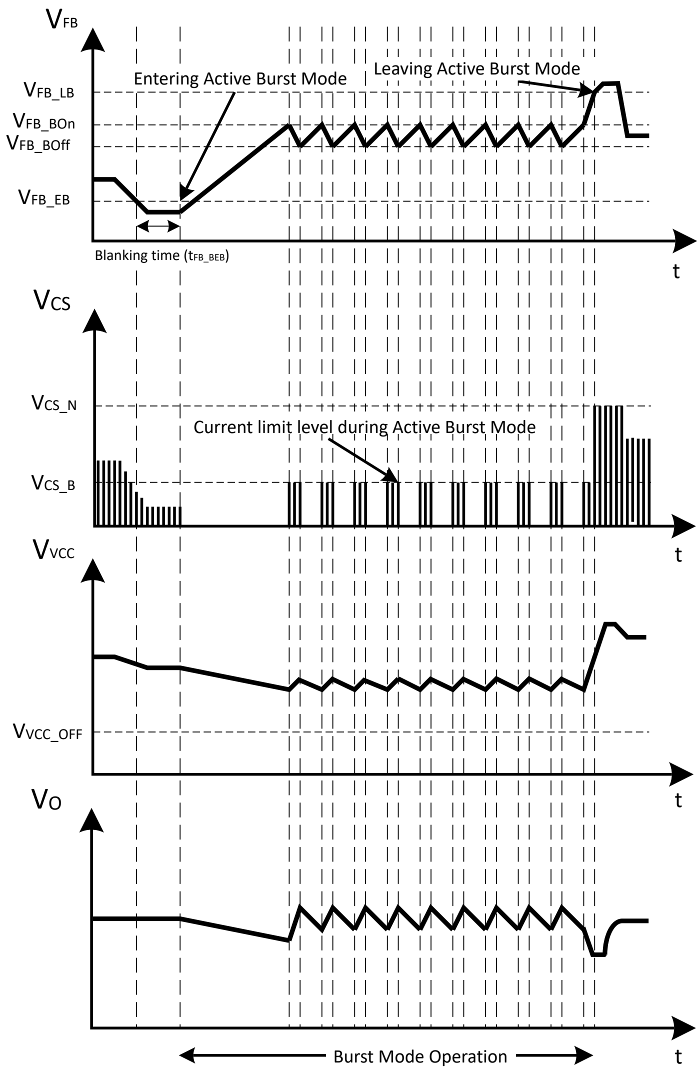


Figure 8 **Waveforms in ABM**

3.6 Non-isolated/isolated configuration

PWM FF Gen5 Pro has a VERR pin, which is connected to the input of an integrated error amplifier to support non-isolated converter (see non-isolated typical application circuit). When *VCC* is charging and before reaching the *V*CC on threshold, a current source $I_{ERR\_P\_BIAS}$ from the VERR pin together with R_{F1} and R_{F2} generates a voltage across it. If the *V*ERR voltage is more than $V_{ERR\_P\_BIAS}$, the non-isolated configuration is selected, otherwise, the isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

In case of non-isolated configuration, the voltage divider R_{F1} and R_{F2} is used to sense the output voltage and compared with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

3.7 Gate voltage selection

The gate voltage can be selected by changing the different resistance R_{Sel} at FB pin. There are three configuration options for different V_{GATE}. The table below shows the control logic for the selection of gate voltage with the $R_{Sel.}$

Table 4 Gate voltage selection table

Option	R_{sel}	V_{GATE}
1	300 kΩ ~ 502 kΩ	V_{GATE_HIGH1}
2	721 kΩ ~ 797 kΩ	V_{GATE_HIGH2}
3	> 1.14 MΩ or open	V_{GATE_HIGH3}

During the IC first startup, the controller preset the gate voltage selection to option 3. When the VCC reaches V_{VCC_ON}, the resistor R_{Sel} in the FB pin is sensed and the gate voltage option is chosen accordingly.

3.8 Protection functions

PWM FF Gen5 Pro provides numerous protection functions that considerably improve the power supply system robustness, safety, and reliability. The following table summarizes those protection functions and the corresponding protection mode; non-switch auto restart, auto restart or extended cycle skip auto restart mode. Refer to Figure 9, Figure 10 and Figure 11 for the illustrated waveform.

Table 5 Protection function table

Protection function	Normal mode	Burst mode	Burst mode	Protection mode
		Burst ON	Burst OFF	
Line overvoltage	Y	Y	Y	Non-switch auto restart
VCC overvoltage	Y	Y	NA	Extended cycle skip auto restart
VCC undervoltage	Y	Y	Y	Auto restart
Overload or open loop	Y	NA	NA	Extended cycle skip auto restart
Overtemperature	Y	Y	Y	Non-switch auto restart
VCC short to GND	Y	Y	Y	No start-up

3.8.1 VCC overvoltage and undervoltage

During operation, the VCC voltage is continuously monitored.

- If VCC voltage falls below V_{VCC_OFF} for a blanking time of $t_{VCC\_OFF\_B}$, MOSFET will be switched off and auto restart will be initiated.
- If VCC voltage exceeds V_{VCC_OVP} for a blanking time of $t_{VCC\_OVP\_B}$, MOSFET will be switched off and extended cycle skip auto restart will be initiated.

3.8.2 Overload or open loop

In case of open control loop or output overload, the FB voltage will be pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB\_OLP\_B}$, the IC enters extended cycle skip auto restart mode. The blanking time enables the converter to provide a peak power in case the increase in V_{FB} is due to a sudden load increase.

3.8.3 Overtemperature

If the junction temperature of controller exceeds T_{jCon_OTP}, the IC enters into overtemperature protection (OTP) auto restart mode. The IC has also implemented with a hysteresis temperature T_{jHYS_OTP}. That means the IC can only be recovered from OTP when the controller junction temperature is dropped T_{jHYS_OTP} lower than the overtemperature trigger point.

3.8.4 VCC short to GND

To limit the power dissipation of the startup circuit at V_{CC} short to GND condition, the V_{CC} charging current is limited to a minimum level of $I_{VCC\_ Charge1}$. With such low current, the power loss of the IC is limited to prevent overheating.

3.8.5 Line overvoltage

The line overvoltage protection (LOVP) is detected by sensing the bus capacitor voltage through the VING pin via the resistor R_{VING}. When the bus voltage increase to a threshold where the fixed reference current I_{VING_LOVP} times the internal resistor is equal to the internal OVP reference V_{VING_LVOP}, the line OVP is triggered. The line overvoltage threshold is calculated by $I_{VING\_LOVP} \times R_{VING} + V_{VING\_REG}$. Once the V_{BUS} voltage is higher than the line overvoltage threshold, the system enters into LOVP protection mode until the V_{BUS} drops below the overvoltage limit.

3.8.6 Three different auto restart modes

All the protections are in auto restart mode with a new soft start sequence. The three auto restart modes are illustrated in the following figures.

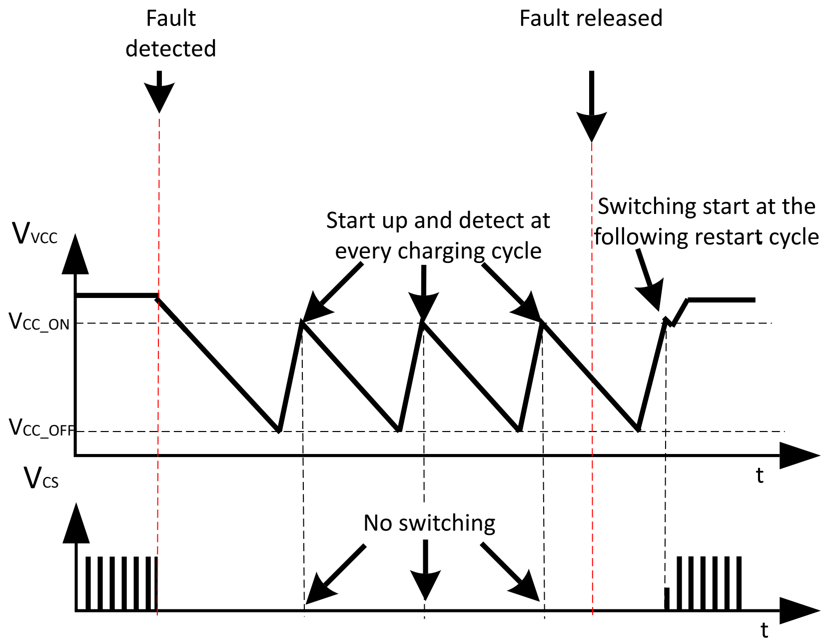


Figure 9 Non-switch auto restart mode

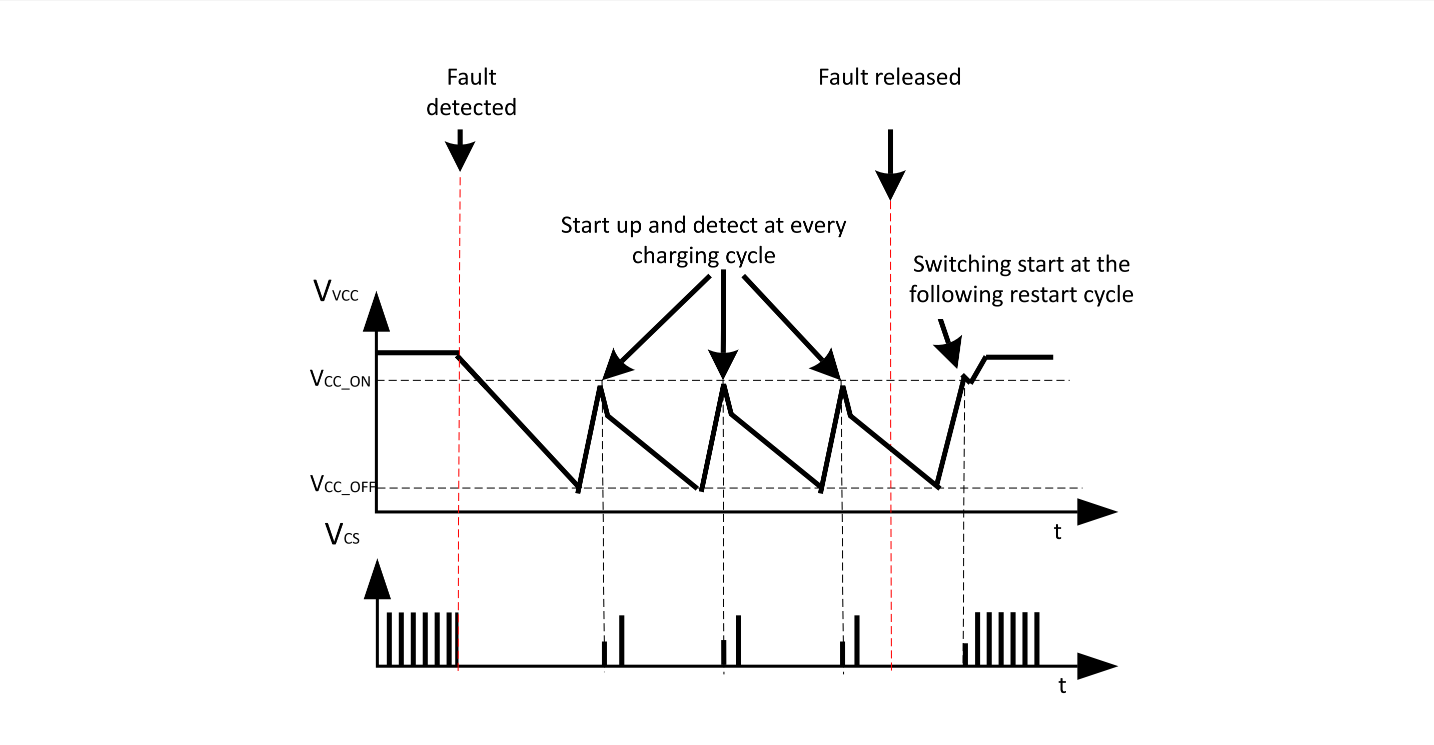


Figure 10 **Auto restart mode**

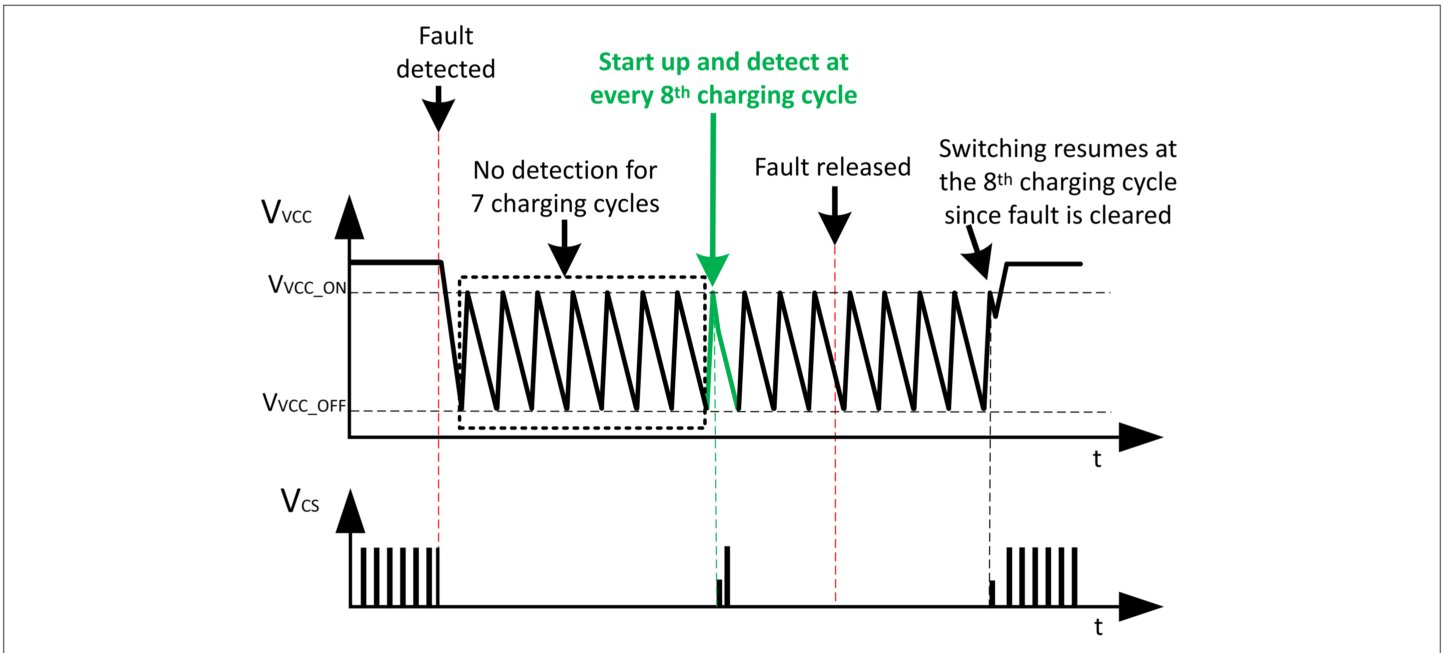


Figure 11 **Extended cycle skip auto restart**

4 Electrical characteristics

Attention: ***All voltages are measured with respect to ground (pin 8). The voltage levels are valid if other ratings are not violated.***

[1.] Not subject to production test, specified by design.

4.1 Absolute maximum ratings

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. For the same reason, make sure that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.*** T_a***=25 °C unless otherwise specified.***

Table 6 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pin rating						
VCC supply voltage	V_{VCC}	-0.3	–	35	V	
Source voltage	V_{SOURCE}	-0.3	–	27	V	
GATE voltage	V_{GATE}	-0.3	–	32	V	
FB voltage	V_{FB}	-0.3	–	5.5	V	
VERR voltage	V_{ERR}	-0.3	–	5.5	V	
CS voltage	V_{CS}	-0.3	–	3.6	V	
VING voltage	V_{VING}	-0.3	–	35	V	Limited by VING absolute maximum current
DC current at SOURCE pin, ICE501XD				0.9	A	Limited by $T_J$max
DC current at SOURCE pin, ICE502XD	I_{SOURCE}	–	–	1.2	A	Limited by T_J max
Single pulse current at SOURCE pin	I_{S_pulse}	–	–	5.8	A	Pulse width t_p = 20 µs and limited by T_J max.
Maximum DC current on any pin	I_{PIN_MAX}	-10	–	10	mA	Except VING, SOURCE and CS pin
VING maximum current	I_{VING_max}	–	–	300	µA	
ESD robustness HBM	V_{ESD_HBM}	-2000	–	2000	V	According to ANSI/ESDA/JEDEC JS-001
ESD robustness CDM	V_{ESD_CDM}	-500	–	500	V	According to ANSI/ESDA/JEDEC JS-002
Junction temperature range	T_j	-40	–	150	°C	
Storage temperature	T_{STORE}	-55	–	150	°C	

4.2 Package characteristics

Table 7

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance (Junction-ambient)	R_{thJA}	–	168	–	K/W	Setup according to the JEDEC standard JESD51

4.3 Operating range

***Note**: Within the operating range, the IC operates as described in the functional description.*

Table 8 Operating range

Within the operating range, the IC operates as described in the functional description.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC supply voltage	V_{VCC}	V_{VCC_OFF}	–	V_{VCC_OVP}	V	
Junction temperature of controller	T_{jCon_op}	-40	–	T_{jCon_OTP}	˚C	

4.4 Operating conditions

***Note**: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40°C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{VCC} = 22 V is assumed.*

Table 9 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC charge current	$I_{VCC\_Charge1}$	-0.35	-0.15	-0.07	mA	V_{VCC} = 0 V, R_{VING} = 20 MΩ and V_{DRAIN} = 90 V
VCC charge current	$I_{VCC\_Charge2}$	–	-3.4	–	mA	V_{VCC} = 3 V, R_{VING} = 20 MΩ and V_{DRAIN} = 90 V
VCC charge current	$I_{VCC\_Charge3}$	-5	-3.6	-1	mA	V_{VCC} = 15 V, R_{VING} = 20 MΩ and V_{DRAIN} = 90 V
Current consumption, startup current	$I_{VCC\_Startup}$	–	0.25	–	mA	V_{VCC} = 15 V
Current consumption, normal	I_{VCC_Normal}	–	1.25	–	mA	I_{FB} = 0 A (No gate switching)
Current consumption, auto restart	I_{VCC_AR}	–	470	–	µA	
Current consumption, burst mode – isolated	$I_{VCC\_BurstMode\_ISO}$	–	0.64	–	mA	
Current consumption, burst mode – non-isolated	$I_{VCC\_BurstMode\_NISO}$	–	0.75	–	mA	
VCC turn-on threshold voltage	V_{VCC_ON}	18.4	19.0	19.8	V	
VCC turn-off threshold voltage	V_{VCC_OFF}	12.0	12.5	13.0	V	

(table continues...)

Table 9 (continued) Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC short circuit protection	V_{VCC_SCP}	–	1.1	1.9	V	
VCC turn-off blanking	$t_{VCC\_OFF\_B}$	–	50	–	µs	

4.5 Internal voltage reference

Table 10 Internal voltage reference

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Internal reference voltage	V_{REF}	3.15	3.27	3.39	V	Measured at FB pin I_{FB} = 0 A

4.6 Gate driver

Table 11 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage at logic low	V_{GATE_LOW} [1]	–	0.09	0.18	V	I_{sink} = 20 mA
Output voltage at logic high 1	$V_{GATE\_HIGH\_1}$	8	10	12	V	V_{VCC} = 22 V, C_{GATE} = 1 nF
Output voltage at logic high 2	$V_{GATE\_HIGH\_2}$	15.5	18.0	20.5	V	V_{VCC} = 22 V, C_{GATE} = 1 nF
Output voltage at logic high 3	$V_{GATE\_HIGH\_3}$	13	15	17	V	V_{VCC} = 22 V, C_{GATE} = 1 nF
Rise time for logic high 1	$t_{GATE\_RISE\_GH1}$ [1]	–	93	–	ns	C_{GATE} = 1 nF
Fall time for logic high 1	$t_{GATE\_FALL\_GH1}$ [1]	–	15	–	ns	C_{GATE} = 1 nF
Rise time for logic high 2	$t_{GATE\_RISE\_GH2}$ [1]	–	161	–	ns	C_{GATE} = 1 nF
Fall time for logic high 2	$t_{GATE\_FALL\_GH2}$ [1]	–	23	–	ns	C_{GATE} = 1 nF
Rise time for logic high 3	$t_{GATE\_RISE\_GH3}$ [1]	–	135	–	ns	C_{GATE} = 1 nF
Fall time for logic high 3	$t_{GATE\_FALL\_GH3}$ [1]	–	20	–	ns	C_{GATE} = 1 nF

[1]. Note subject to production test, specified by design.

4.7 PWM section

Table 12 PWM section

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fixed oscillator frequency – 65 kHz	f_{OSC_L}	59.8	65	70.2	kHz	Operating temperature range
Fixed oscillator frequency – 65 kHz 25°C	$f_{OSC\_L\_25C}$	61.1	65	68.9	kHz	T_j = 25°C
Fixed oscillator frequency – 100 kHz	f_{OSC_M}	92	100	108	kHz	Operating temperature range
Fixed oscillator frequency – 100 kHz 25°C	$f_{OSC\_M\_25C}$	94	100	106	kHz	T_j = 25°C
Fixed oscillator frequency – 65 kHz (ABM)	$f_{OSC\_L\_ABM}$	46.2	54	61.1	kHz	T_j = 25°C
Fixed oscillator frequency – 100 kHz (ABM)	$f_{OSC\_M\_ABM}$	71	83	94	kHz	T_j = 25°C
Fixed oscillator frequency – 65 kHz (minimum fsw)	$f_{OSC\_L\_MIN}$	23.4	28	33.2	kHz	T_j = 25°C
Fixed oscillator frequency – 100 kHz (minimum fsw)	$f_{OSC\_M\_MIN}$	36	43	51	kHz	T_j = 25°C
Frequency jittering range	f_{JITTER} [1]	–	± 4	–	%	T_j = 25°C
Frequency jittering period	t_{JITTER} [1]	–	4	–	ms	T_j = 25°C
Maximum duty cycle	D_{MAX}	70	75	80	%	
Feedback pull-up resistor	R_{FB}	11	15	20	kΩ	
PWM-OP gain	G_{PWM}	1.85	2.03	2.2		
Offset for voltage ramp	V_{PWM}	0.42	0.5	0.58	V	
Slope compensation rate - 65 kHz	M_{COMP_L}	–	60	–	mV/μs	Vcs = 0 V
Slope compensation rate - 100 kHz	M_{COMP_M}	–	93.5	–	mV/μs	Vcs = 0 V
Feedback cutoff voltage	V_{FB_Cutoff}	–	0.41	–	V	When $V_{FB} < V_{FB\_Cutoff}$, no PWM switching.

1. Not subject to production test, specified by design.

4.8 Error amplifier

Table 13 Error amplifier

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transconductance	G_{ERR_M}	2.14	2.90	3.77	mA/V	
Transconductance – Burst mode	G_{ERR_BM}	6.9	9.5	11.6	mA/V	
Error amplifier source current	I_{ERR_SOURCE}	85	150	223	µA	
Error amplifier sink current	I_{ERR_SINK}	85	150	223	µA	
Error amplifier reference voltage	V_{ERR_REF}	1.76	1.80	1.84	V	
Error amplifier output dynamic range of transconductance	V_{ERR_DYN}	0.05	–	3.15	V	
Error amplifier mode bias current	$I_{ERR\_P\_BIAS}$	9.5	14.0	18.5	µA	
Error amplifier mode threshold	$V_{ERR\_P\_BIAS}$	0.16	0.20	0.24	V	

4.9 Current sense

Table 14 Current sense

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CS_N}	0.72	0.80	0.88	V	$dV_{sense}/dt = 0.41$ V/µs
Peak current limitation in normal operation, 15% duty cycle	V_{CS_N15}	0.74	0.79	0.84	V	
Leading edge-blanking time	t_{CS_LEB}	205	260	315	ns	
Peak current limitation in ABM	V_{CS_B}	0.18	0.22	0.26	V	

4.10 Soft start

Table 15 Soft start

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Soft start time	t_{SS}	7.3	11.5	–	ms	
Soft start time step	t_{SS_S}[1]	–	3	–	ms	
CS peak voltage at first step of soft start	V_{SS1}[1]	–	0.30	–	V	
Step increment of CS peak voltage in soft start	V_{SS_S}[1]	–	0.15	–	V	

1. Not subject to production test, specified by design.

4.11 Active burst mode

Table 16 Active burst mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Feedback voltage for entering ABM	V_{FB_EB}	–	0.95	–	V	
Blanking time for entering ABM	t_{FB_BEB}	–	34	–	ms	
Feedback voltage for leaving ABM	V_{FB_LB}	2.63	2.73	2.83	V	
Feedback voltage for burst-on – isolated case	$V_{FB\_Bon\_ISO}$	2.26	2.35	2.45	V	
Feedback voltage for burst-off – isolated case	$V_{FB\_BOff\_ISO}$	1.88	2.00	2.05	V	
Feedback voltage for burst-on – non-isolated case	$V_{FB\_Bon\_NISO}$	1.88	2.00	2.05	V	
Feedback voltage for burst-off – non-isolated case	$V_{FB\_BOff\_NISO}$	1.50	1.55	1.64	V	

4.12 Line overvoltage protection

Table 17 Line overvoltage protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Line overvoltage threshold	I_{VING_LOVP}	21	22	23	µA	
Line overvoltage blanking	$t_{VING\_LOVP\_B}$	–	250	–	µs	

(table continues...)

Table 17 **(continued) Line overvoltage protection**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VING regulation voltage	V_{VING_REG}	1.77	1.80	1.87	V	With V_{VCC} = 22 V, I_{VING} = 10 µA
VING voltage in LOVP protection	V_{VING_LOVP}	–	1.5	3.6	V	V_{VCC} = 22V , I_{VING} = 300 µA

4.13 VCC overvoltage protection

Table 18 **VCC overvoltage protection**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC overvoltage threshold	V_{VCC_OVP}	29	30.5	32.5	V	
VCC overvoltage blanking	$t_{VCC\_OVP\_B}$	–	54	–	µs	

4.14 Overload protection

Table 19 **Overload protection**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overload detection threshold for OLP protection at FB pin	V_{FB_OLP}	2.63	2.73	2.83	V	
Overload protection blanking time	$t_{FB\_OLP\_B}$	30	54	–	ms	

4.15 Thermal protection

Table 20 **Thermal protection**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature protection	T_{jcon_OTP}[1]	129	140	150	°C	
Overtemperature hysteresis	T_{jHYS_OTP}	–	40	–	°C	
Overtemperature blanking time	$t_{jcon\_OTP\_B}$	–	54	–	µs	

1. Not subject to production test, specified by design.

4.16 Low side MOSFET

Table 21 Low side MOSFET

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain source on-resistance, ICE501XD 25C	$R_{dson\_01\_25C}$	–	–	0.256	Ω	T_j = 25°C
Drain source on-resistance, ICE501XD 125C	$R_{dson\_01\_125C}$[1]	–	–	0.404	Ω	T_j = 125°C
Drain source on-resistance, ICE502XD 25C	$R_{dson\_02\_25C}$	–	–	0.125	Ω	T_j = 25°C
Drain source on-resistance, ICE502XD 125C	$R_{dson\_02\_125C}$[1]	–	–	0.196	Ω	T_j = 125°C

1. Not subject to production test, specified by design.

5 Output power curve

The calculated output power curves versus ambient temperature are shown below. The curves are derived based on a typical DCM flyback in an open frame design setting the maximum T_j of the low side integrated MOSFET at 125°C, using minimum drain pin copper area in a 2 oz copper single-sided PCB and steady state operation only (no design margins for abnormal operation modes are included).

The output power figure is for selection purpose only. The actual power can vary depending on a particular design. In a power supply system, appropriate thermal design margins must be considered to make sure that the operation of the device is within the maximum ratings given in Chapter 4.1.

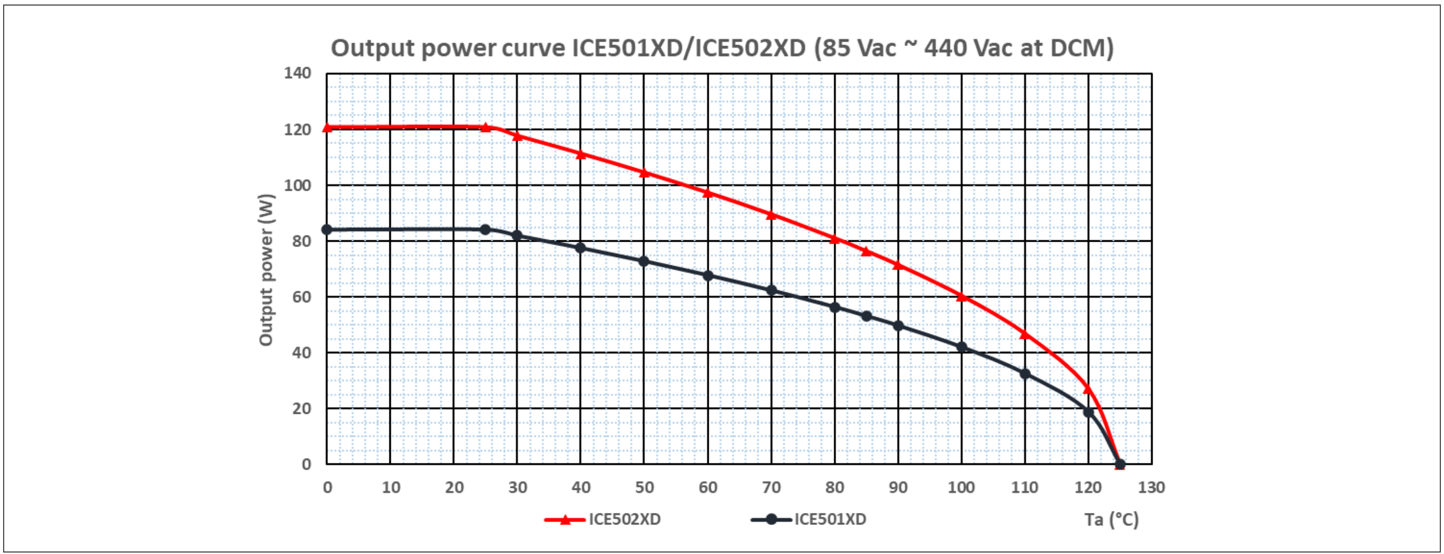


Figure 12 **Output power curve ICE501XD/ICE502XD (85 Vac ~ 440 Vac)**

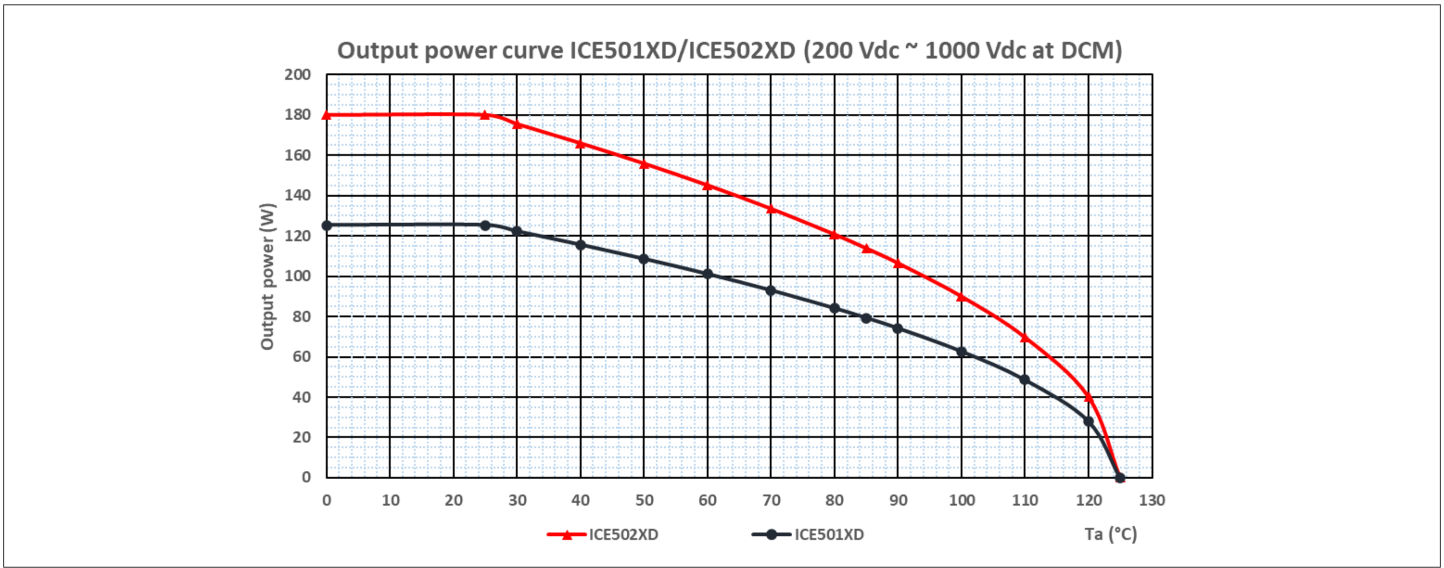
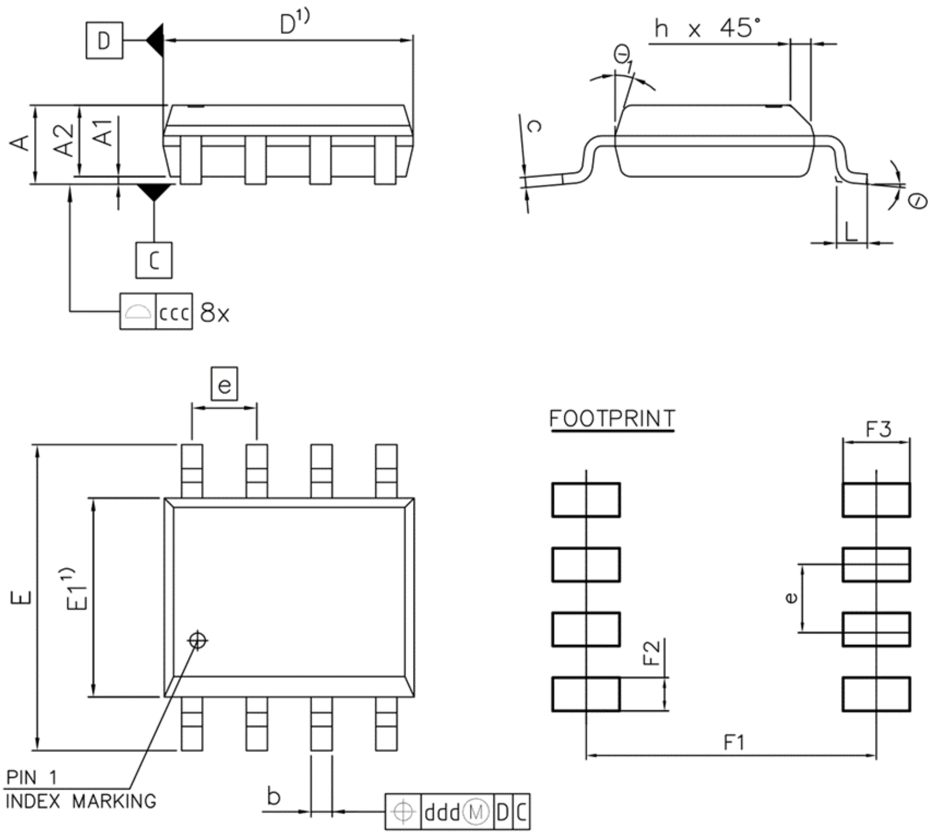


Figure 13 **Output power curve ICE501XD/ICE502XD (200 Vdc ~ 1000 Vdc)**

6 Package information

Dimension of PG-DSO-8:



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
$Θ_1$	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

Figure 14 **PG-DSO-8**

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (i.e., Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

6.1 Marking

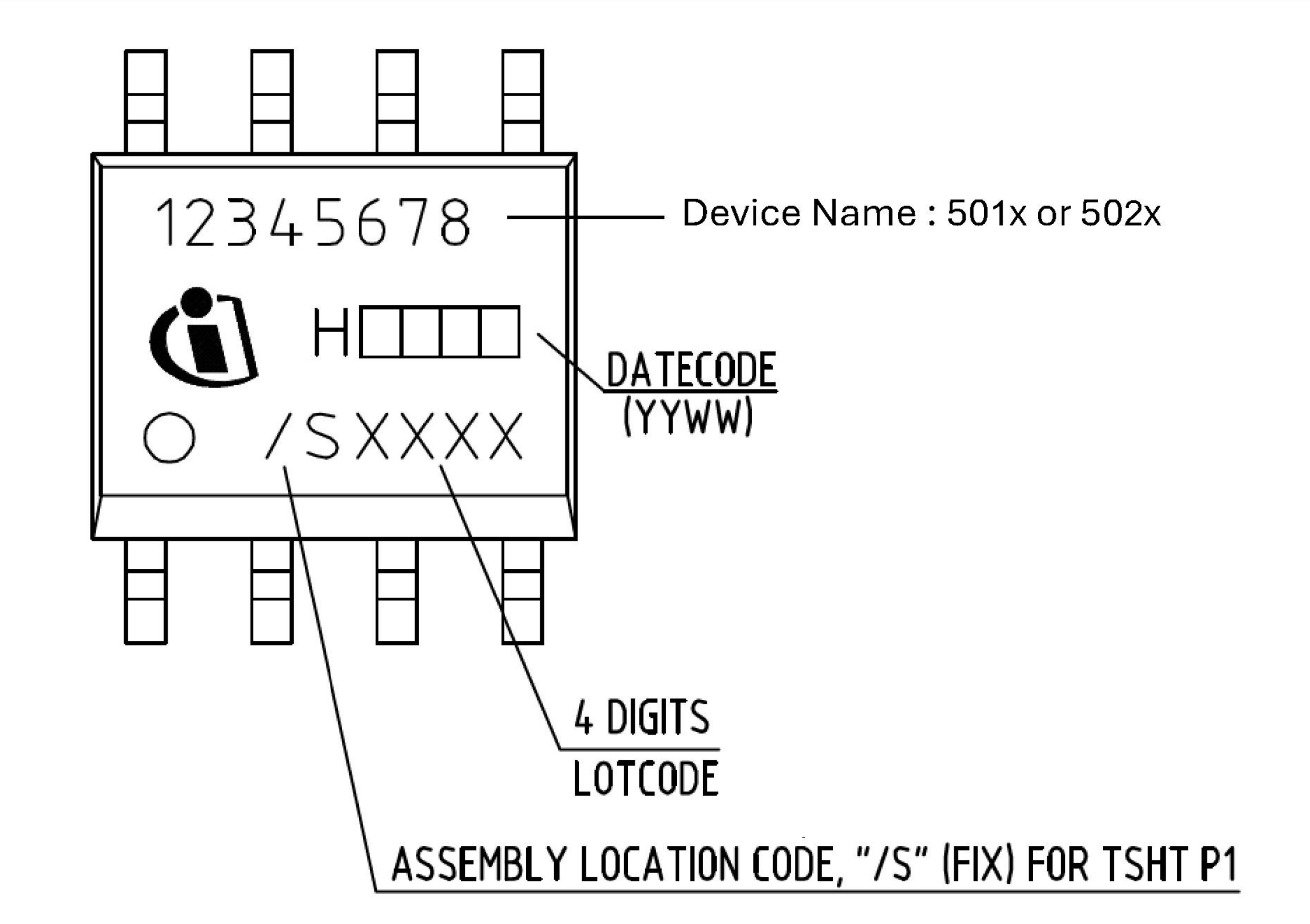


Figure 15 Marking for ICE501LD/ICE501MD/ICE502LD/ICE502MD

7 Revision history

Revision	Date	Changes
Rev 1.0	2025-12-03	Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-12-03

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-exh1758540006256