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# CoolSET®-F3R80

## ICE3AR10080CJZ

## Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS® and Startup cell (brownout & CCM) in DIP-7

Power Management & Supply

Never stop thinking.

Previous Version: 0.1

| | |
|---|---|
| 19 | Revise typo in tie up resistor at BRL pin to disable brownout feature. |
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# Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS® and Startup cell (brownout & CCM) in DIP-7

PG-DIP7

**Product Highlights**

- **800V avalanche rugged CoolMOS® with startup cell**
- **CCM and DCM operation with slope compensation**
- **Active Burst Mode to reach the lowest Standby Power <100mW**
- **Active burst mode with selectable entry and exit burst mode level**
- **Frequency jitter and soft driving for low EMI**
- **Brownout feature**
- **Latch enable and fast AC reset**
- **Auto Restart protection for over load, over temperature and over voltage**
- **Pb-free lead plating; RoHS compliant**

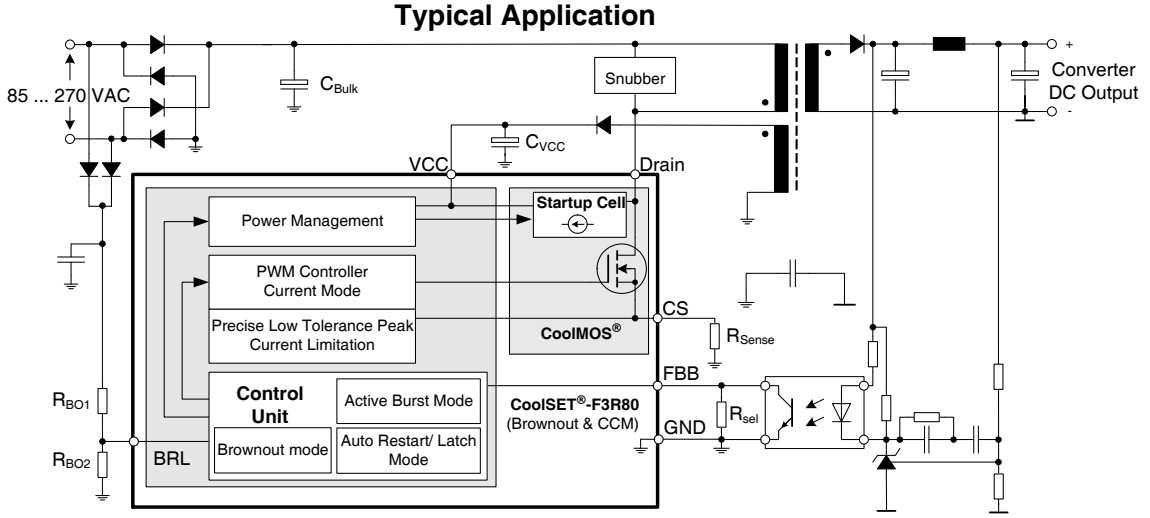
## Features

- 800V avalanche rugged CoolMOS® with Startup Cell
- Active Burst Mode for lowest Standby Power
- Slope compensation for CCM operation
- Selectable entry and exit burst mode level
- 100kHz internally fixed switching frequency with jittering feature
- Auto Restart Protection for Over load, Open Loop, VCC Under voltage & Over voltage and Over temperature
- External latch enable pin and fast AC reset
- Over temperature protection with 50°*C* hysteresis
- Built-in 10ms Soft Start
- Built-in 40ms blanking time for short duration peak power
- Propagation delay compensation for both maximum load and burst mode
- Brownout feature
- BiCMOS technology for low power consumption and wide VCC voltage range
- Soft gate drive with 50Ω turn on resistor

## Description

The ICE3ARxx80CJZ is an enhanced version of ICE3ARxx80JZ (CoolSET®-F3R80). The PWM controller is based on F3R80 with new and enhanced features. The major new features include slope compensation for CCM operation and fast AC reset after latch enabled. The major enhanced features include fixed voltage brownout detect and voltage detect for the burst selection. In particular it is a device running at 100KHz, implemented with brownout features, installing 800V CoolMOS® with startup cell and packaged into DIP-7. It targets for the low power SMPS with increased MOSFET voltage margin requirement such as Off-Line battery adapters, DVD R/W, DVD Combi, Blue ray, set top box, auxiliary power supply for PC and server, etc. In summary, this enhanced ICE3ARxx80CJZ provides 800V MOSFET, lowest standby power, CCM opeation, selectable burst level, brownout feature, maximum power compensated for both maximum and standby load, low EMI with frequency jittering and soft gate drive, built-in and flexible protections, etc. Therefore, ICE3ARxx80CJZ is a complete solution for the low power SMPS application.

**Typical Application**




| Type | Package | Marking | $V_{DS}$ | $F_{OSC}$ | $R_{DSon}$ [1] | 230VAC ±15% [2] | 85-265 VAC [2] |
|---|---|---|---|---|---|---|---|
| ICE3AR10080CJZ | PG-DIP-7 | 3AR10080CJZ | 800V | 100kHz | 10.0Ω | 22W | 15W |

[1] typ @ T=25°C

[2] Calculated maximum input power rating at $T_a$=50°C, $T_j$=125°C and without copper area as heat sink.

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# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration with PG-DIP-7

| Pin | Symbol | Function |
|---|---|---|
| 1 | BRL | Brownout, fast AC Reset & Latch enable |
| 2 | FBB | Feedback & Burst entry/exit control |
| 3 | CS | Current Sense/ 800V CoolMOS® Source |
| 4 | n.c. | not connected |
| 5 | Drain | 800V CoolMOS® Drain |
| 6 | - | (no pin) |
| 7 | VCC | Controller Supply Voltage |
| 8 | GND | Controller Ground |

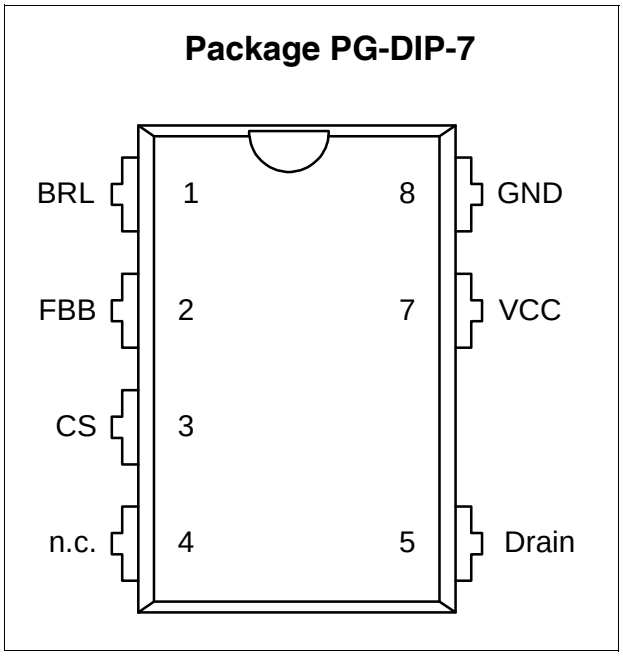


*Figure 1 Pin Configuration PG-DIP-7 (top view)*

## 1.2 Pin Functionality

**BRL (Brownout, fast AC Reset & Latch enable)**

The BRL pin combines the functions of brownout, fast AC reset and the external latch enable. The brownout feature is to stop the switching pulse when the input voltage is dropped to lower than 1V. The Fast AC reset feature is to recover from latch feature when the voltage of BRL pin has a rising rate of <1.33V/ms from 0.4V to 1V. The external latch enable function is an external access to stop the gate switching and force the IC to enter latch mode. It is triggered by pulling the pin voltage to less than 0.4V.

**FBB (Feedback & Burst entry select)**

The FBB pin combines the feedback function and the burst entry/exit control. The regulation information is provided by the FBB pin to the internal Protection Unit and the internal PWM-Comparator to control the duty cycle. The FBB-signal is the only control signal in case of light load at the Active Burst Mode. The burst entry select provides an access to select the entry/exit burst mode level.

**CS (Current Sense)**

The Current Sense pin senses the voltage developed on the shunt resistor inserted in the source of the integrated CoolMOS®. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode operation.

**Drain (Drain of integrated CoolMOS®)**

The Drain pin is the connection to the Drain of the integrated CoolMOS®.

**VCC (Power Supply)**

The VCC pin is the power supply of the IC. The voltage operating range is between 10.5V and 24.7V.

**GND (Ground)**

The GND pin is the ground of the controller.

# 2 Representative Blockdiagram

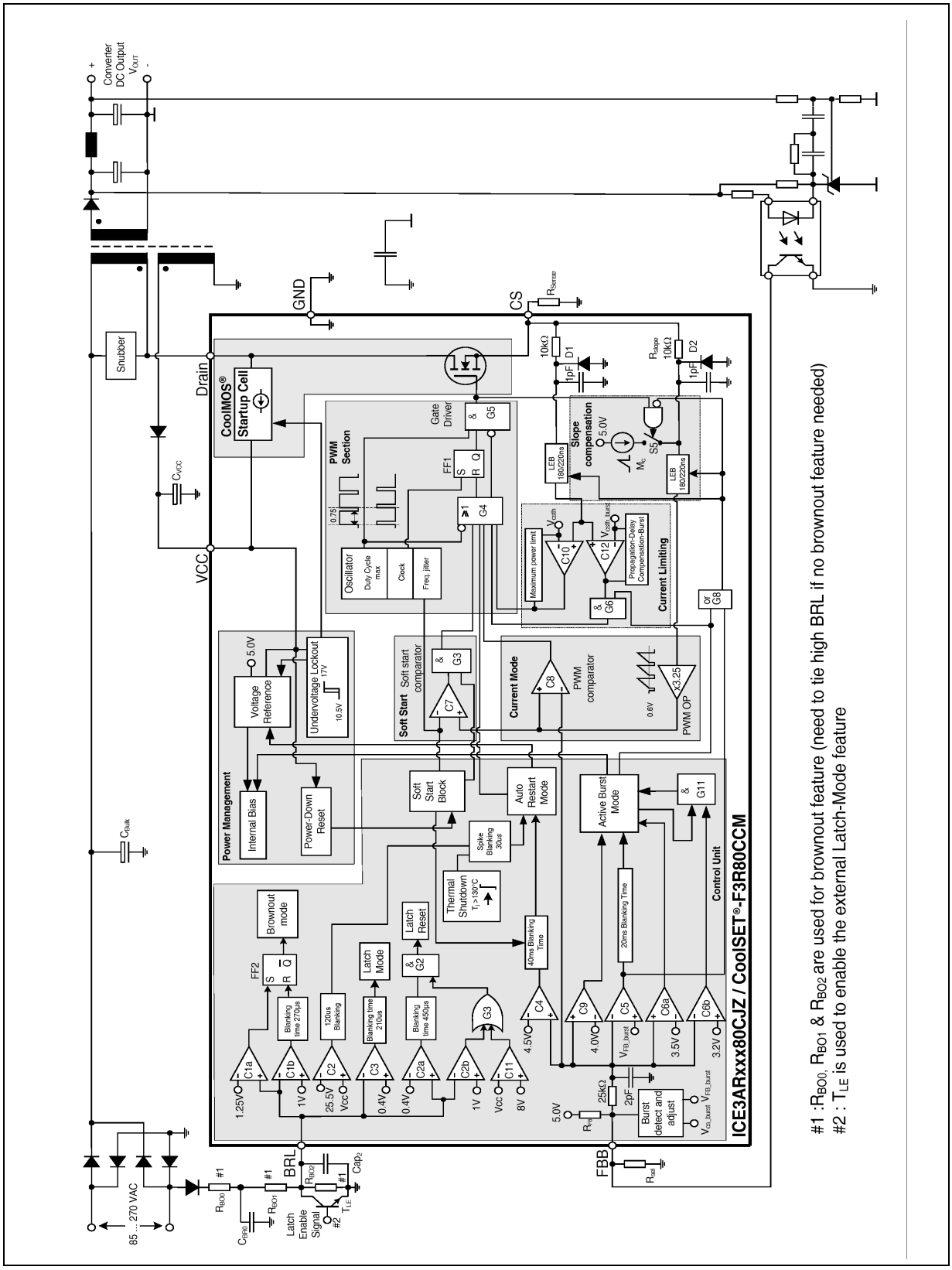


*Figure 2 Representative Blockdiagram*

# 3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

## 3.1 Introduction

ICE3ARxx80CJZ brownout and CCM 800V version is an enhanced version of the CoolSET®-F3R80. The major new and enhanced features include slope compensation for CCM operation, fast AC reset after latch enabled, fixed voltage brownout detect and voltage detect for the burst selection. It is particular good for high voltage margin low power SMPS application such as auxiliary power supply for PC and server. The major characteristics are that the IC is developed with 800V CoolMOS® with start up cell, having adjustable brownout feature, running at 100KHz switching frequency, CCM operation and packed in DIP-7 package.

The features include BiCMOS technology to reduce power consumption and increase the Vcc voltage range, cycle by cycle current mode control, built-in 10ms soft start to reduce the stress of switching elements during start up, built-in 40ms for short period of peak power before entering protection, active burst mode for lowest standby power, propagation delay compensation for close power limit between high line and low line which also takes into consideration of slope compensation, frequency jittering for low EMI performance, the built-in auto-restart mode protections for open loop, over load, Vcc OVP, Vcc under voltage, and latch enable feature etc.

The other features include narrowing the feedback voltage swing to 0.3V (from 0.5V) during burst mode so that the output voltage ripple can be reduced by 40%, reduction of the fast voltage fall time of the MOSFET by increasing the soft turn-on time and addition of 50Ω turn-on resistor, faster start up time by optimizing the Vcc capacitor to 10uF and over temperature protection with 50°C hysteresis.

The new features include slope compensation for stable operation in CCM mode when duty is larger than 0.5, fixed voltage triggering for the bronwout feature for easier design, voltage levels select for entry/exit burst level, fast AC reset fto reset the latch feature, etc.

In summary, the CoolSET® ICE3ARxx80CJZ provides good voltage margin of MOSFET, lowest standby power, flexible burst level, CCM operation, reduced output ripple during burst mode, accurate power limit for both maximum power and burst power, low EMI with frequency jittering and soft gate drive, built-in and flexible protections, etc. Therefore, CoolSET® ICE3ARxx80CJZ is a complete solution for the low power SMPS application.

## 3.2 Power Management

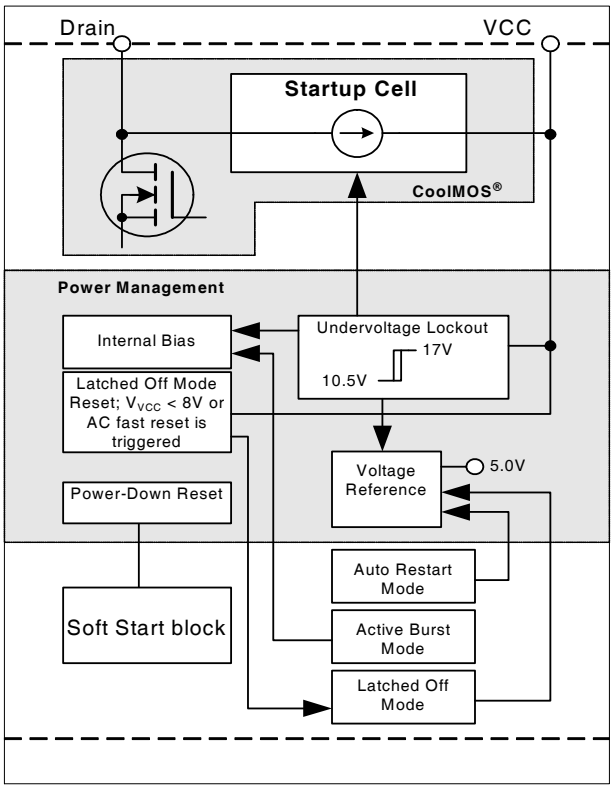


*Figure 3 Power Management*

The Undervoltage Lockout monitors the external supply voltage $V_{VCC}$. When the SMPS is plugged to the main line the internal Startup Cell is biased and starts to charge the external capacitor $C_{VCC}$ which is connected to the VCC pin. This VCC charge current is controlled to 1.0mA by the Startup Cell. When the $V_{VCC}$ exceeds the on-threshold $V_{CCon}$=17V the bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the Drain voltage. To avoid uncontrolled ringing at switch-on, a hysteresis start up voltage is implemented. The switch-off of the controller can only take place when $V_{VCC}$ falls below 10.5V after normal operation was entered. The maximum current consumption before the controller is activated is about 210µA.

When $V_{VCC}$ falls below the off-threshold $V_{CCoff}$=10.5V, the bias circuit is switched off and the soft start counter is reset. Thus it ensures that at every startup cycle the soft start starts at zero.

The internal bias circuit is switched off if Latched Off Mode or Auto Restart Mode is entered. The current consumption is then reduced to 420µA.

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require re-cycling the AC line. In case Latched Off Mode is entered, VCC needs to be lowered below 8V or having AC fast reset triggered to reset the

Latched Off Mode. This is done usually by re-cycling the AC line.

When Active Burst Mode is entered, the internal Bias is switched off most of the time but the Voltage Reference is kept alive in order to reduce the current consumption below 620µA.

### 3.3 Improved Current Mode

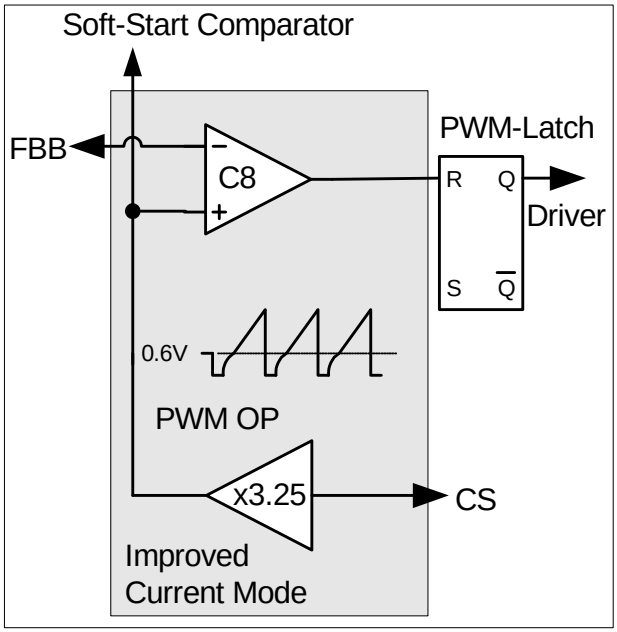


*Figure 4 Current Mode*

Current Mode means the duty cycle is controlled by the slope of the primary current. This is done by comparing the FBB signal with the amplified current sense signal.

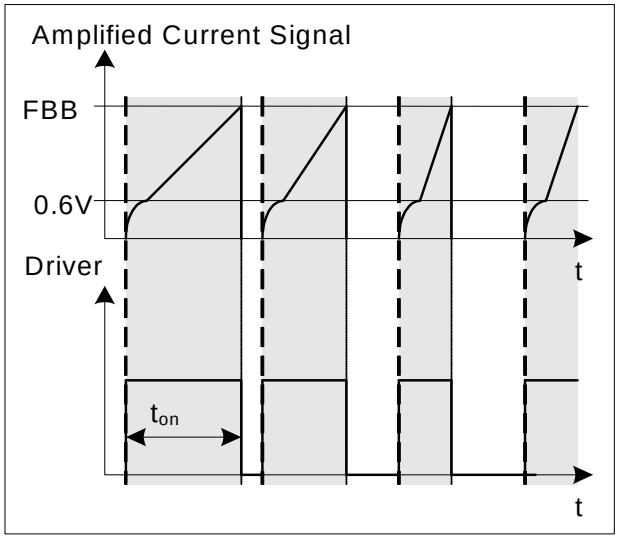


*Figure 5 Pulse Width Modulation*

In case the amplified current sense signal exceeds the FBB signal the on-time $t_{on}$ of the driver is finished by resetting the PWM-Latch (Figure 5).

The primary current is sensed by the external series resistor $R_{Sense}$ inserted in the source of the integrated CoolMOS®. By means of Current Mode regulation, the secondary output voltage is insensitive to the line variations. The current waveform slope will change with the line variation, which controls the duty cycle.

The external $R_{Sense}$ allows an individual adjustment of the maximum source current of the integrated CoolMOS®.

To improve the Current Mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch T2, the voltage source V1 and a resistor R1 (see Figure 6). Every time the oscillator shuts down for maximum duty cycle limitation the switch T2 is closed by $V_{OSC}$. When the oscillator triggers the Gate Driver, T2 is opened so that the voltage ramp can start.

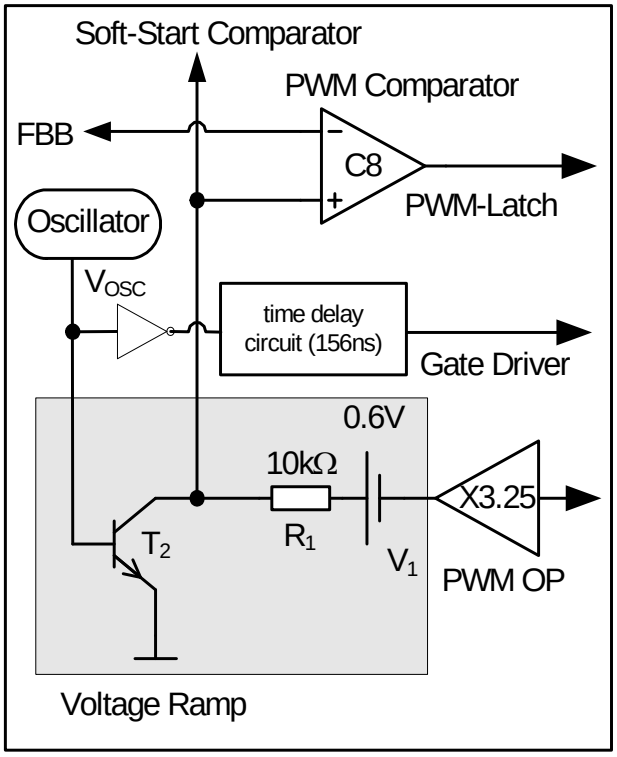


*Figure 6 Improved Current Mode*

In case of light load the amplified current ramp is too small to ensure a stable regulation. In that case the Voltage Ramp is a well defined signal for the comparison with the FBB-signal. The duty cycle is then controlled by the slope of the Voltage Ramp.

By means of the time delay circuit which is triggered by the inverted $V_{OSC}$ signal, the Gate Driver is switched-off until it reaches approximately 156ns delay time (Figure

7). It allows the duty cycle to be reduced continuously till 0% by decreasing $V_{FBB}$ below that threshold.

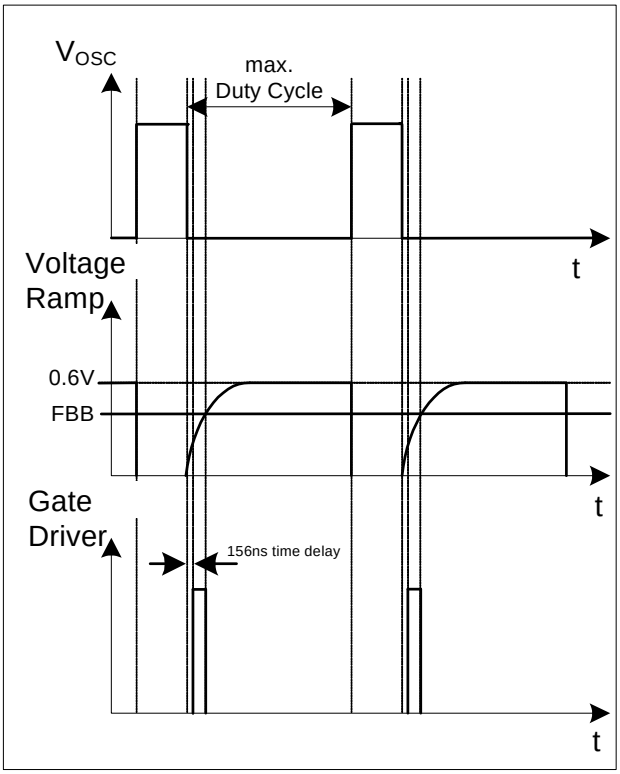


*Figure 7 Light Load Conditions*

### 3.3.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor $R_{Sense}$ connected to pin CS. $R_{Sense}$ converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.25 by PWM OP. The output of the PWM-OP is connected to the voltage source $V_1$. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM-Comparator C8 and the Soft-Start-Comparator (Figure 8).

### 3.3.2 PWM-Comparator

The PWM-Comparator compares the sensed current signal of the integrated CoolMOS® with the feedback signal $V_{FBB}$ (Figure 8). $V_{FBB}$ is created by an external optocoupler or external transistor in combination with the internal pull-up resistor $R_{FB}$ and provides the load information of the feedback circuitry. When the amplified current signal of the integrated CoolMOS® exceeds the signal $V_{FBB}$ the PWM-Comparator switches off the Gate Driver.

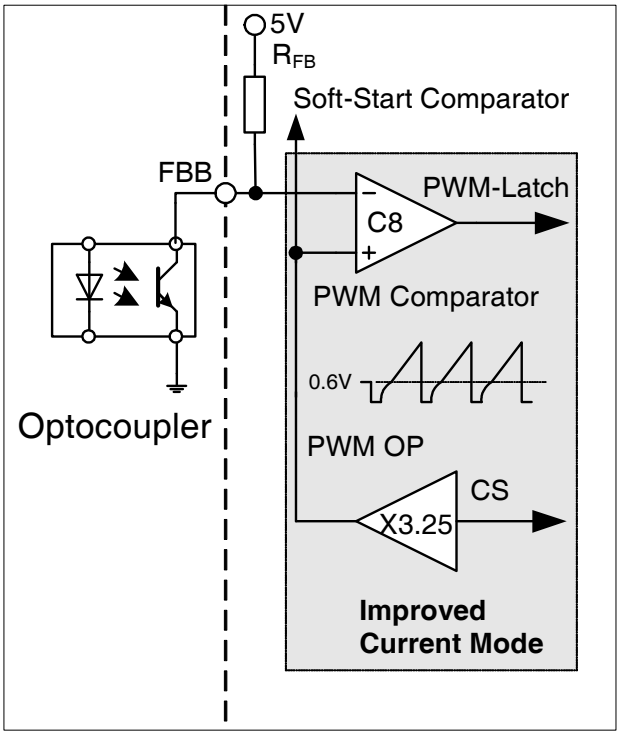


*Figure 8 PWM Controlling*

### 3.3.3 Slope Compensation

Due to the sub harmonic oscillation of CCM operation when duty cycle is larger than 50%, the slope compensation is added.

The slope Mc; 50mV/µs is added to the current sense pin when gate is on.

During burst mode operation, the Mc slope is shut down and no slope added into the current sense signal. This can save the power consumption at burst mode.

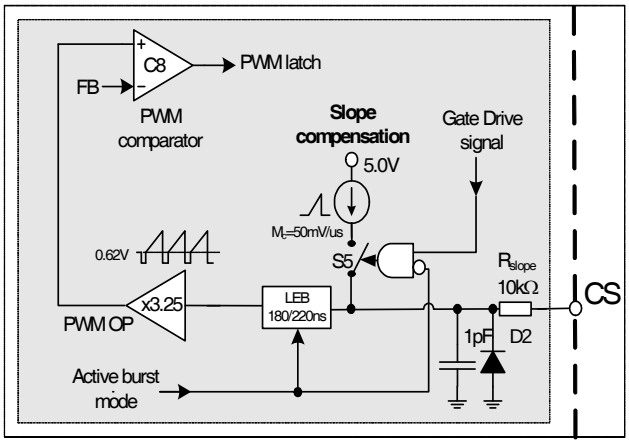


*Figure 9 Slope compesnation*

## 3.4 Startup Phase

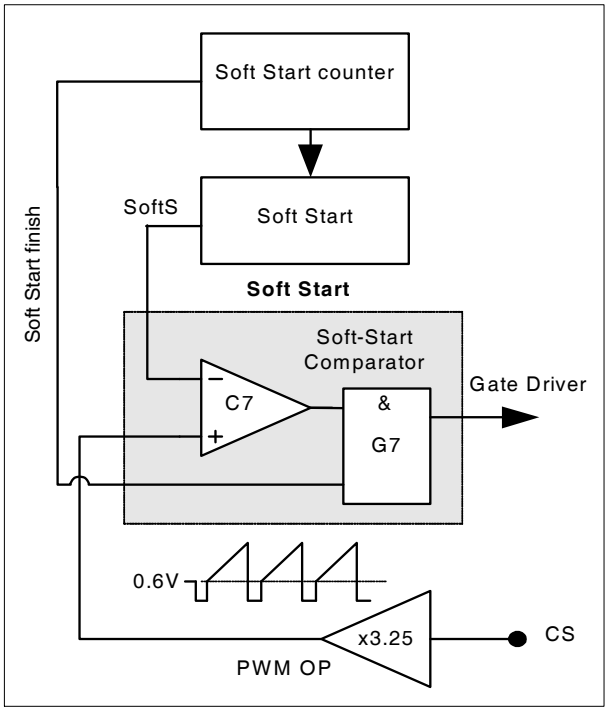


*Figure 10 Soft Start*

In the Startup Phase, the IC provides a Soft Start period to control the primary current by means of a duty cycle limitation. The Soft Start function is a built-in function and it is controlled by an internal counter.

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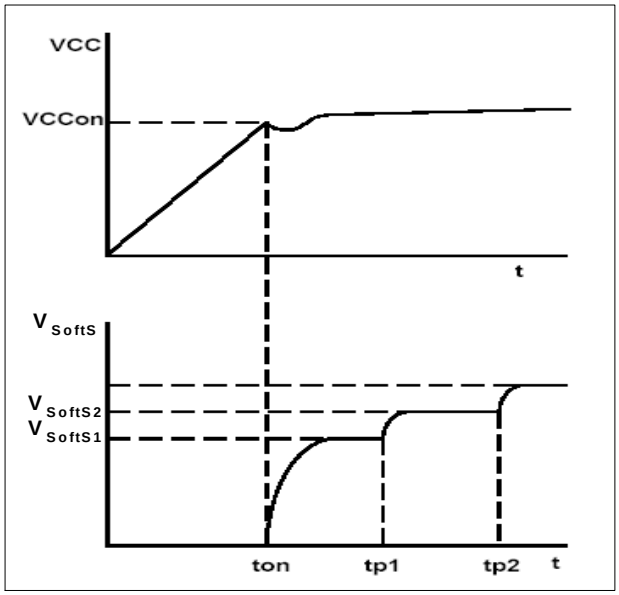



*Figure 11 Soft Start Phase*

When the $V_{VCC}$ exceeds the on-threshold voltage, the IC starts the Soft Start mode (Figure 11).

The function is realized by an internal Soft Start resistor, an current sink and a counter. And the amplitude of the current sink is controlled by the counter (Figure 12).

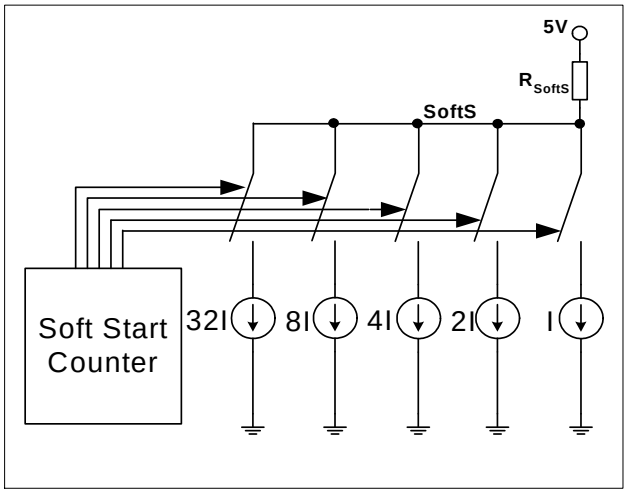



*Figure 12 Soft Start Circuit*

After the IC is switched on, the $V_{SoftS}$ voltage is controlled such that the voltage is increased step-wisely (32 steps) with the increase of the counts. The Soft Start counter would send a signal to the current sink control in every 300µs such that the current sink decrease gradually and the duty ratio of the gate drive increases gradually. The Soft Start will be finished in 10ms ($t_{Soft\text{-}Start}$) after the IC is switched on. At the end of the Soft Start period, the current sink is switched off.

Within the soft start period, the duty cycle is increasing from zero to maximum gradually (see Figure 13).

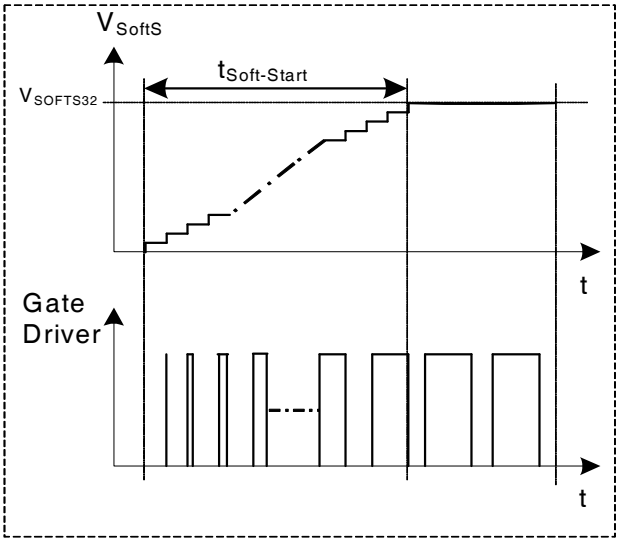



*Figure 13 Gate drive signal under Soft-Start Phase*

In addition to Start-Up, Soft-Start is also activated at each restart attempt during normal Auto Restart.

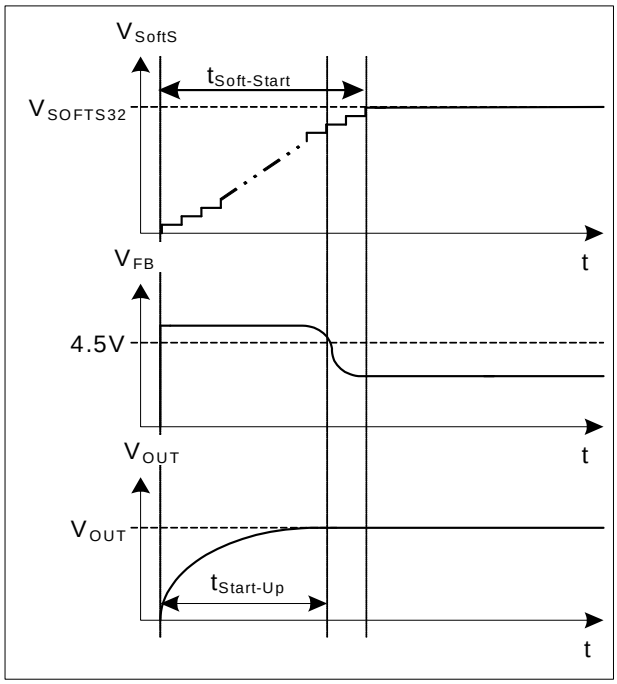



*Figure 14 Start Up Phase*

The Start-Up time $t_{Start-Up}$ before the converter output voltage $V_{OUT}$ is settled, must be shorter than the Soft-Start Phase $t_{Soft-Start}$ (Figure 14). By means of Soft-Start there is an effective minimization of current and voltage stresses on the integrated CoolMOS®, the clamp circuit and the output rectifier and it helps to prevent saturation of the transformer during Start-Up.

## 3.5 PWM Section

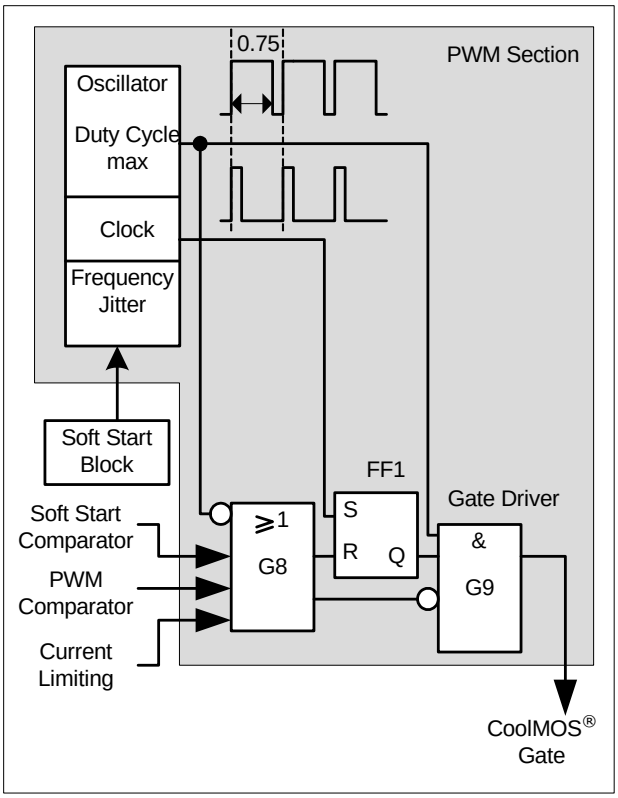



*Figure 15 PWM Section Block*

### 3.5.1 Oscillator

The oscillator generates a fixed frequency of 100KHz with frequency jittering of ±4% (which is ±4KHz) at a jittering period of 4ms.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of $D_{max}$=0.75.

Once the Soft Start period is over and when the IC goes into normal operating mode, the switching frequency of the clock is varied by the control signal from the Soft Start block. Then the switching frequency is varied in range of 100KHz ± 4KHz at period of 4ms.

### 3.5.2 PWM-Latch FF1

The output of the oscillator block provides continuous pulse to the PWM-Latch which turns on/off the integrated CoolMOS®. After the PWM-Latch is set, it is reset by the PWM comparator, the Soft Start comparator or the Current -Limit comparator. When it is in reset mode, the output of the driver is shut down immediately.

### 3.5.3 Gate Driver

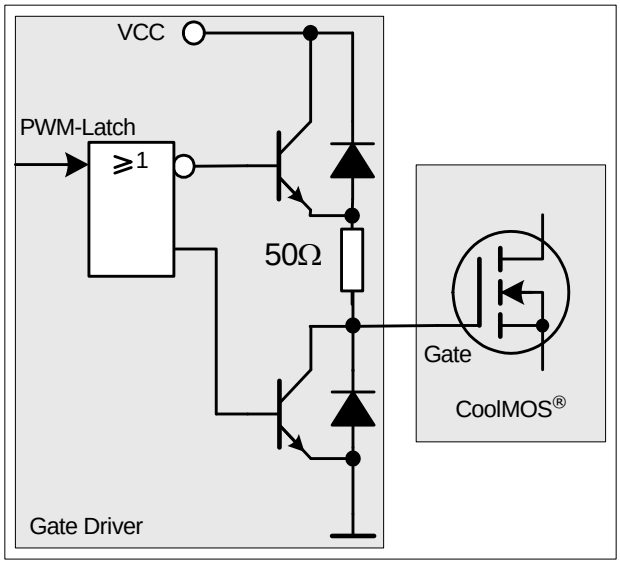



*Figure 16 Gate Driver*

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the integrated CoolMOS® threshold. This is achieved by a slope control of the rising edge at the driver's output (Figure 17) and adding a 50Ω gate turn on resistor (Figure 16). Thus the leading switch on spike is minimized.

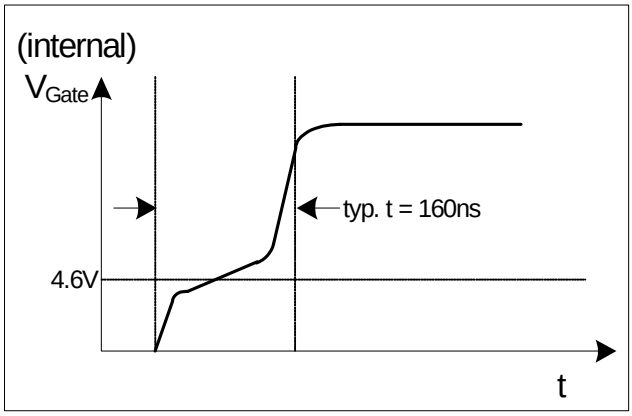



*Figure 17 Gate Rising Slope*

Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

During power up, when VCC is below the undervoltage lockout threshold $V_{VCCoff}$, the output of the Gate Driver is set to low in order to disable power transfer to the secondary side.

## 3.6 Current Limiting

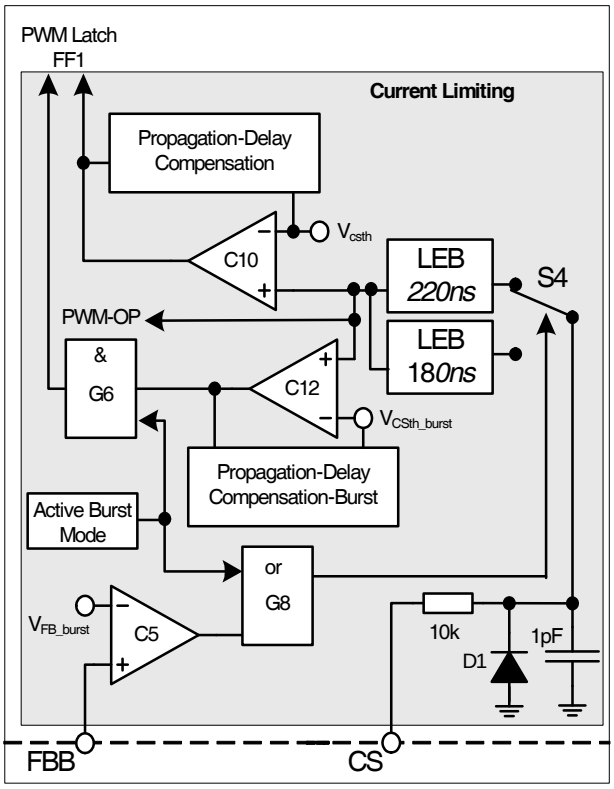



*Figure 18 Current Limiting Block*

There is a cycle by cycle peak current limiting operation realized by the Current-Limit comparator C10. The source current of the integrated CoolMOS® is sensed via an external sense resistor $R_{Sense}$. By means of $R_{Sense}$ the source current is transformed to a sense voltage $V_{Sense}$ which is fed into the pin CS. If the voltage $V_{Sense}$ exceeds the internal threshold voltage $V_{csth}$, the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1.

A Propagation Delay Compensation is added to support the immediate shut down of the integrated CoolMOS® with very short propagation delay. Thus the influence of the AC input voltage on the maximum output power can be reduced to minimal. This compensation applies to both the peak load and burst mode.

In order to prevent the current limit from distortions caused by leading edge spikes, a Leading Edge Blanking (LEB) is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the Gate G6 if Active Burst Mode is entered. When it is activated, the current limiting is reduced to $V_{csth_burst}$. This voltage level determines the maximum power level in Active Burst Mode.

### 3.6.1 Leading Edge Blanking

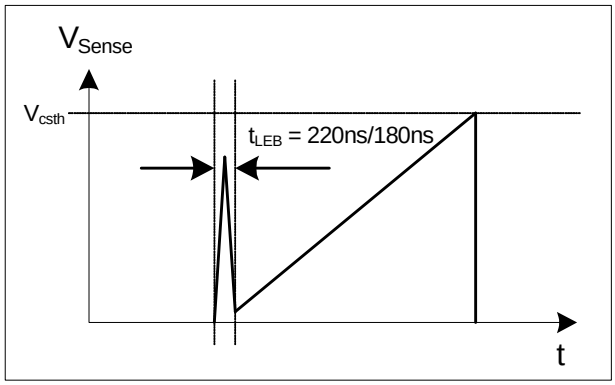



*Figure 19 Leading Edge Blanking*

Whenever the integrated CoolMOS® is switched on, a leading edge spike is generated due to the primary-side capacitances and reverse recovery time of the secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of $t_{LEB}$ = 220ns for normal load and $t_{LEB}$ = 180ns for burst mode.

### 3.6.2 Combined OPP curve considering Propagation Delay and Slope Compensation

The ICE3ARxx80CJZ has combined the propagation delay, CCM inherit reduced power effect and the slope compensation effect for the overcurrent control.

It employs the dynamic threshold voltage $V_{csth}$ with 2 steps slope compensation to achieve the closed over current for whole input voltage range.

In case of overcurrent detection, there is always propagation delay to switch off the integrated CoolMOS®. An overshoot of the peak current $I_{peak}$ is induced to the delay, which depends on the ratio of dI/dt of the peak current (Figure 20).

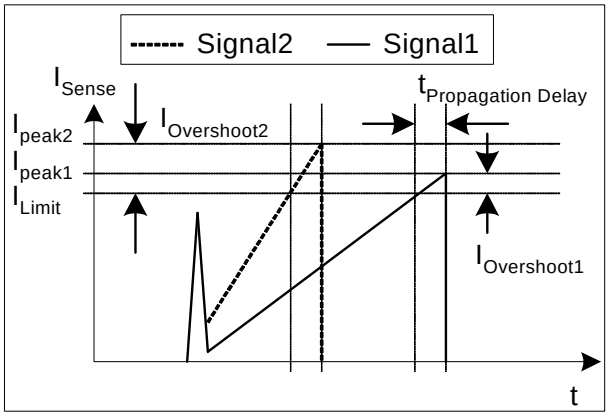



*Figure 20 Current Limiting*

The overshoot of Signal2 is larger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold $V_{csth}$ and the switching off of the integrated CoolMOS® is compensated over temperature within a wide input range. Current Limiting is then very accurate.

For the inherit influence of the CCM operation, the final Vcs can not be constant in whole line range as in DCM. This ICE3ARxx80CJZ has implemented with 2 compensation curves for the compensation so that the maximum power can be close. One of the curve is used when the time range is larger than 4µs and the other is for lower than 4µs.

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage $V_{csth}$ (Figure 21). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

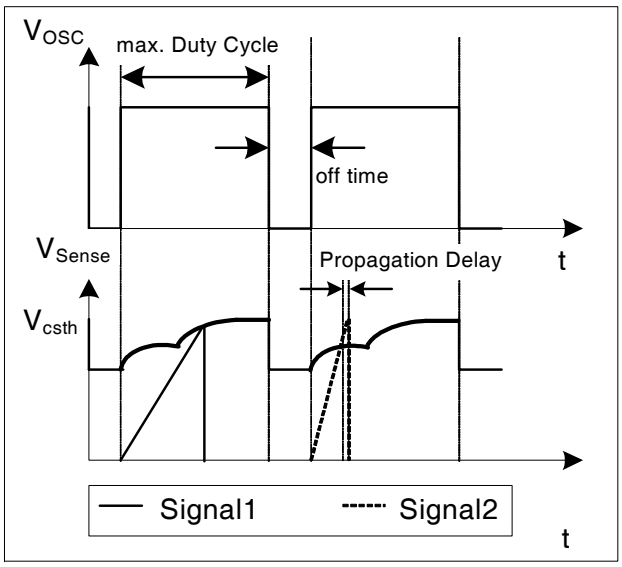



*Figure 21 Dynamic Voltage Threshold $V_{csth}$*

A typical measured Vsense vs dVsense/dt is plotted in Figure 22 for reference.

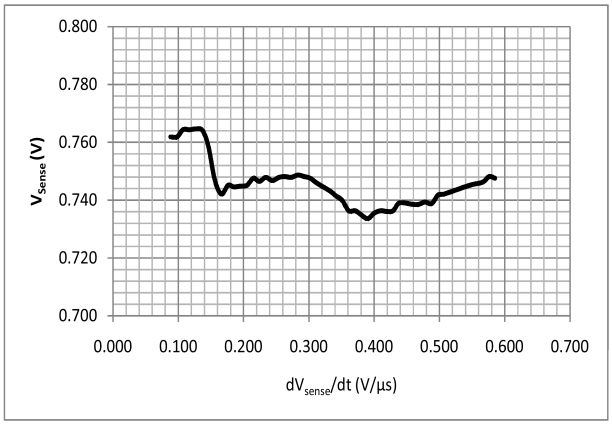



*Figure 22 Overcurrent Shutdown*

Similarly, the same concept of propagation delay compensation is also implemented in burst mode with reduced level, $V_{csth_burst}$ (Figure 18). With this implementation, the entry and exit burst mode power can be close between low line and high line input voltage.

## 3.7 Control Unit

The Control Unit contains the functions for Active Burst Mode, Auto Restart Mode and Latch Mode. The Active Burst Mode, Latch Mode and the Auto Restart Mode both have internal blanking time. With the blanking time, the IC avoids entering into those two modes accidentally. Those buffer time is very useful for the application which works in short duration of peak power occasionally.

### 3.7.1 Active Burst Mode (patented)

To increase the efficiency of the system at light load, the most effective way is to operate at burst mode. Starting from CoolSET® F3, the IC has been employing the active burst mode and it can achieve the lowest standby power. ICE3ARxx80CJZ adopts the same concept with some more innovative improvements to the feature. It includes the adjustable entry burst level, close power control between high line and low line and the smaller output ripple during burst mode.

Most of the burst mode design in the market will provide a fixed entry burst mode level which is a ratio to the maximum power of the design. ICE3ARxx80CJZ provides a more flexible level which can be selected externally.

Propagation delay is the major contributor for the power control variation for DCM flyback converter. It is proved to be effective in the maximum power control. ICE3ARxx80CJZ also apply the same concept in the burst mode. Therefore, the entry and exit burst mode power is also finely controlled during burst mode.

The feedback control swing during burst mode will affect the output ripple voltage directly. ICE3ARxx80CJZ reduces the swing to 0.3V (from 0.5V). Therefore, it would have around 40% improvement for the output ripple.

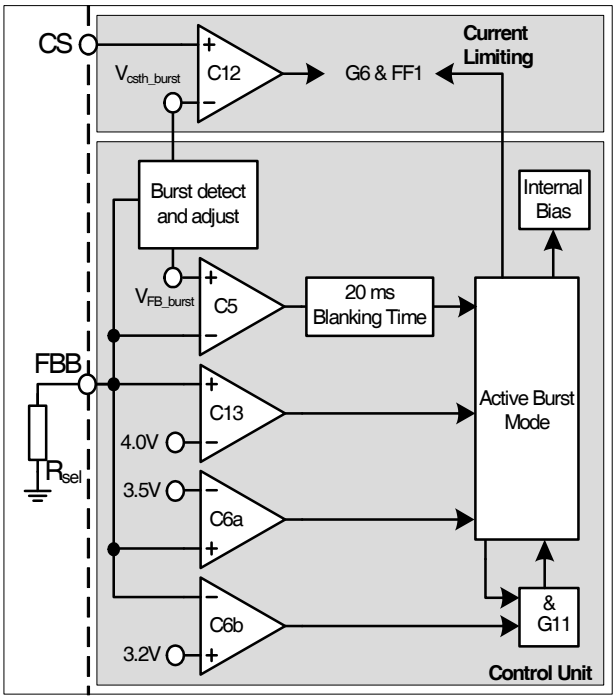



*Figure 23 Active Burst Mode*

The Active Burst Mode is located in the Control Unit. Figure 23 shows the related components.

#### 3.7.1.1 Selectable burst entry level

The burst mode entry level can be selected by changing the different Resistor $R_{sel}$ at FBB pin. There are 3 levels to be selected with different resistor which are targeted for 15%, 10% and 5% of the maximum input power. At the same time, the exit burst level are targeted to 27%, 20% and 11% of the maximum power accordingly. The below table is the control logic for the entry and exit level with the FBB voltage.

| Level | $V_{FBB}$ | $R_{sel}$ |
|---|---|---|
| 1 | $V_{FBB} < V_{ref1}$ (1.8V) | < 405kΩ |
| 2 | $V_{ref1}$ (1.8V) $< V_{FBB} < V_{ref2}$ (4.0V) | 685kΩ ~ 900kΩ |
| 3 | $V_{FBB} > V_{ref2}$ (4.0V) | > 1530kΩ |

| | Entry level | | Exit level | |
|---|---|---|---|---|
| Level | % of $P_{in_max}$ | $V_{FB_burst}$ | % of $P_{in_max}$ | $V_{csth_burst}$ |
| 1 | 5% | 1.29V | 11% | 0.21V |
| 2 | 10% | 1.61V | 20% | 0.29V |
| 3 | 15% | 1.84V | 27% | 0.34V |

During IC first startup, the $Ref_{good}$ signal is logic low when Vcc<8V. The low $Ref_{good}$ signal will reset the Burst Mode level Detection latch. When the Burst Mode Level Detection latch is low and IC is in OFF state, the FBB resistor is isolated from the FBB pin and a current source $I_{sel}$ (3.5µA) is turned on instead.

From Vcc=8V to Vcc on threshold(17V), the FBB pin will start to charge to a voltage level associated with $R_{sel}$ resistor. When Vcc reaches Vcc on threshold, the FBB voltage is sensed. The burst mode thresholds are then chosen according to the FBB voltage level. The Burst Mode Level Detection latch is then set to high. Once the detection latch is set high, any change of the FBB level will not change the threshold level. When Vcc reaches Vcc on threshold, a timer of 2µs is started. After the 2µs ends, the $I_{sel}$ is turned off while the FBB resistor is connected to FBB pin (Figure 24).

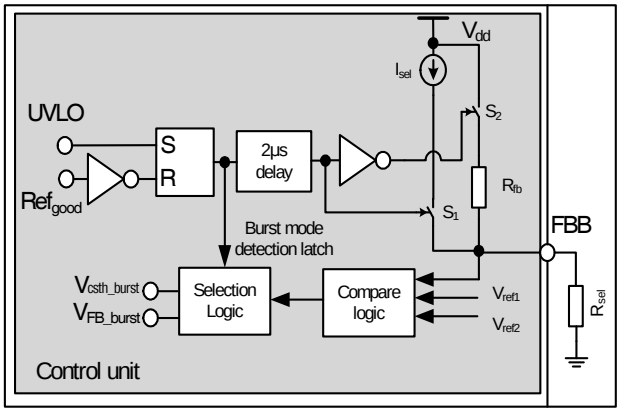



*Figure 24 Burst mode detect and adjust*

#### 3.7.1.2 Entering Active Burst Mode

The FBB signal is kept monitoring by the comparator C5 (Figure 23). During normal operation, the internal blanking time counter is reset to 0. When FBB signal falls below $V_{FB_burst}$, it starts to count. When the counter reaches 20ms and FBB signal is still below $V_{FB_burst}$, the system enters the Active Burst Mode. This time window prevents a sudden entering into the Active Burst Mode due to large load jumps.

After entering Active Burst Mode, a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC to about 620µA.

It needs the application to enforce the VCC voltage above the Undervoltage Lockout level of 10.5V such that the Startup Cell will not be switched on accidentally. Or otherwise the power loss will increase drastically. The minimum VCC level during Active Burst Mode depends on the load condition and the application. The lowest VCC level is reached at no load condition.

#### 3.7.1.3 Working in Active Burst Mode

After entering the Active Burst Mode, the FBB voltage rises as VOUT starts to decrease, which is due to the inactive PWM section. The comparator C6a monitors the FBB signal. If the voltage level is larger than 3.5V, the internal circuit will be activated; the Internal Bias circuit resumes and starts to provide switching pulse. In Active Burst Mode the gate G6 is released and the current limit is reduced to Vcsth_burst (Figure 2 and 23). In one hand, it can reduce the conduction loss and the other hand, it can reduce the audible noise. If the load at VOUT is still kept unchanged, the FBB signal will drop to 3.2V. At this level the C6b deactivates the internal circuit again by switching off the Internal Bias. The gate G11 is active again as the burst flag is set after entering Active Burst Mode. In Active Burst Mode, the FBB voltage is changing like a saw tooth between 3.2V and 3.5V (Figure 25).

#### 3.7.1.4 Leaving Active Burst Mode

The FBB voltage will increase immediately if there is a high load jump. This is observed by the comparator C13 (Figure 23). Since the current limit is reduced to 0.21V~0.34V during active burst mode, it needs a certain load jump to rise the FBB signal to exceed 4.0V. At that time the comparator C5 resets the Active Burst Mode control which in turn blocks the comparator C12 by the gate G6. The maximum current can then be resumed to stabilize $V_{OUT}$.

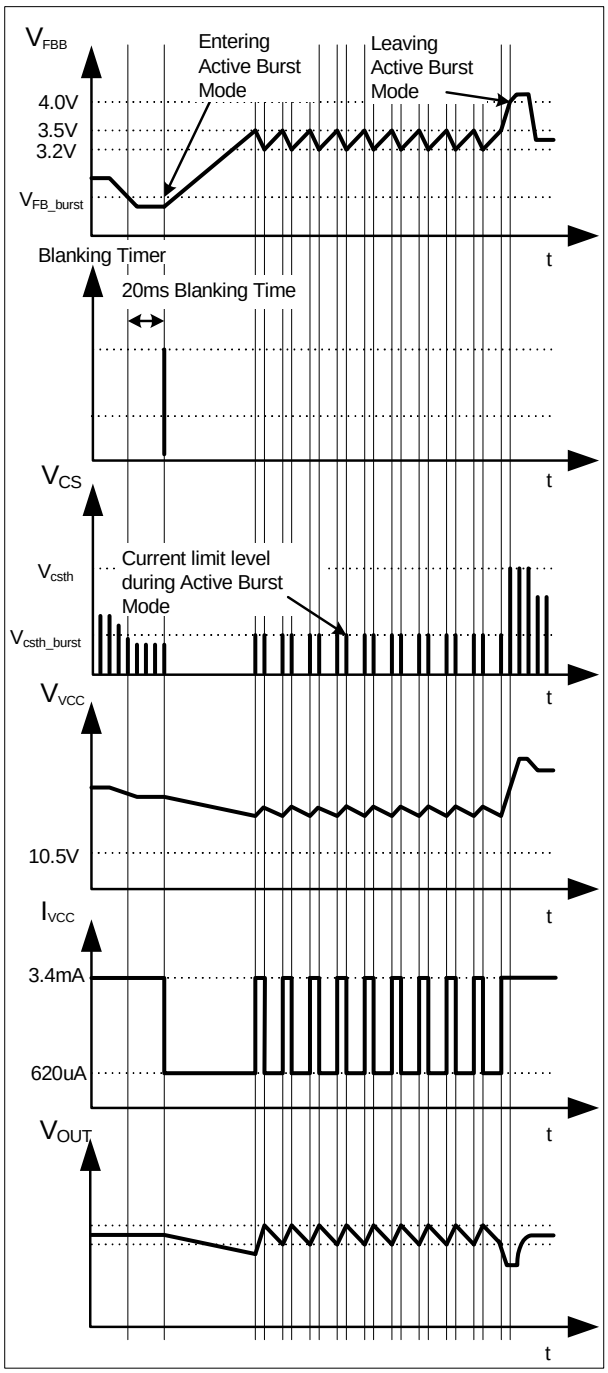



*Figure 25 Signals in Active Burst Mode*

### 3.7.2 Protection Modes

The IC provides Auto Restart mode as the major protection feature. Auto Restart mode can prevent the SMPS from destructive states. There are 3 kinds of auto restart mode; normal auto restart mode, odd skip auto restart mode and non switch auto restart mode. Odd skip auto restart mode (Figure 26) is that there is no detect of fault and no switching pulse for the odd number restart cycle. At the even number of restart cycle the fault detect and soft start switching pulses are maintained. If the fault persists, it would continue the auto-restart mode. However, if the fault is removed, it can release to normal operation only at the even number auto restart cycle .

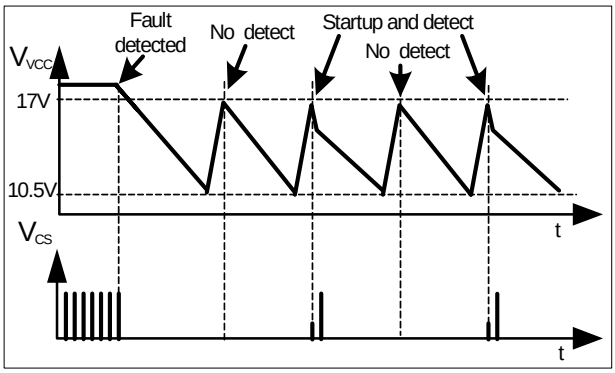



*Figure 26 Odd skip auto restart waveform*

Non switch auto restart mode is similar to odd skip auto restart mode except the start up switching pulses are also suppressed at the even number of the restart cycle. The detection of fault still remains at the even number of the restart cycle. When the fault is removed, the IC will resume to normal operation at the even number of the restart cycle (Figure 27).

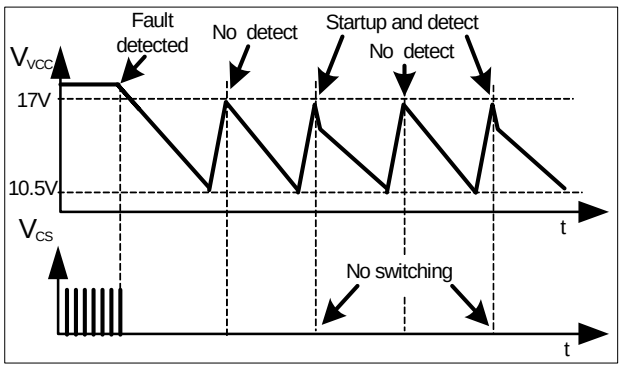



*Figure 27 non switch auto restart waveform*

The main purpose of the odd skip auto restart is to extend the restart time such that the power loss during auto restart protection can be reduced. This feature is particularly good for smaller Vcc capacitor where the restart time is shorter.

The following table lists the possible system failures and the corresponding protection modes.

| | |
|---|---|
| VCC Over voltage | Odd skip Auto Restart Mode |
| Over load | Odd skip Auto Restart Mode |
| Open Loop | Odd skip Auto Restart Mode |
| VCC Undervoltage | Normal Auto Restart Mode |
| Short Optocoupler | Normal Auto Restart Mode |
| Over temperature | Non switch Auto Restart Mode |
| External protection enable | Latch Mode |

#### 3.7.2.1 Vcc OVP, OTP, external protection enable and Vcc under voltage

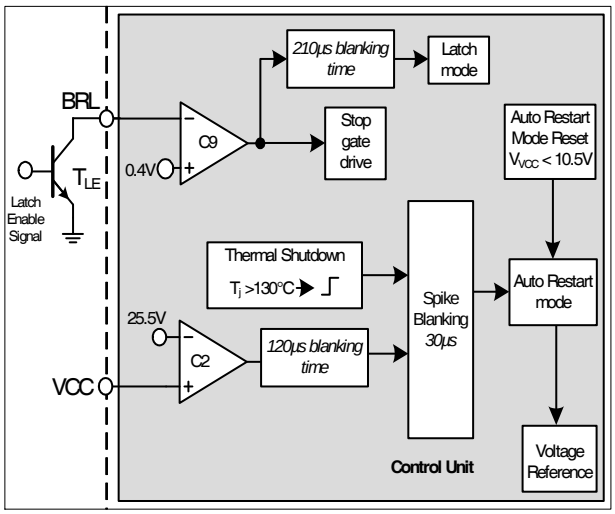



*Figure 28 Vcc OVP, OTP, external protection enable*

Vcc OVP condition is when $V_{VCC}$ voltage is > 25.5V, the IC enters into odd skip Auto Restart Mode (Figure 28).

The over temperature protection OTP is sensed inside the controller IC. The Thermal Shutdown block keeps on monitoring the junction temperature of the controller. After detecting a junction temperature higher than 130°C, the IC will enter into the non switch Auto Restart mode. The ICE3ARxx80CJZ has also implemented with a 50°C hysteresis. That means the IC can only be recovered when the controller junction temperature is dropped 50°C lower than the over temperature trigger point (Figure 28).

The external latch enable feature can provide a flexibility to a customer's self-defined protection feature. This function can be triggered by pulling down the $V_{BRL}$ voltage to < 0.4V. Or it can simply trigger the base pin of an external transistor, $T_{LE}$ at the BRL pin. When this function is enabled, it will enter into latch mode after 210µs blanking time. The gate drive is stopped and there is no switching pulse before it is recovered .

The Vcc undervoltage and short opto-coupler will go into the normal auto restart mode inherently.

In case of VCC undervoltage, the Vcc voltage drops indefinitely. When it drops below the Vcc under voltage lock out "OFF" voltage (10.5V), the IC will turn off the IC and the startup cell will turn on again. Then the Vcc voltage will be charged up to UVLO "ON" voltage (17V) and the IC turns on again provided the startup cell charge up current is not drained by the fault. If the fault is not removed, the Vcc will continue to drop until it hits UVLO "OFF" voltage and the restart cycle repeats.

Short Optocoupler can lead to Vcc undervoltage because once the opto-coupler (transistor side) is shorted, the feedback voltage will drop to zero and there will be no switching pulse. Then the Vcc voltage will drop same as the Vcc undervoltage.

#### 3.7.2.2 Over load, open loop protection

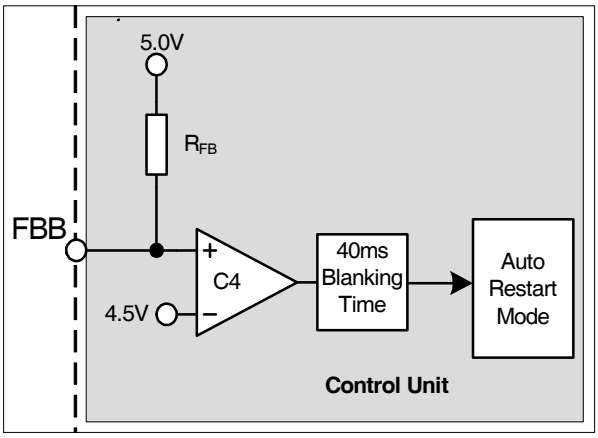



*Figure 29 Over load and open loop protection*

In case of Overload or Open Loop, the $V_{FBB}$ voltage exceeds 4.5V which will be observed by comparator C4. Then the built-in blanking time counter starts to count. When it reaches 40ms, the odd skip Auto Restart Mode is activated (Figure 29).

### 3.7.3 Brownout Mode

When the AC input voltage is removed, the voltage at the bulk capacitor will fall. When it reaches a point that the system is greater than the system allowed maximum power, the system may go into over load protection. However, this kind of protection is not expected for some of the applications such as auxiliary power for PC/server system because the output is in hiccup mode due to over load protection (auto restart mode). The brownout mode is to eliminate this phenomenon. The ICE3ARxx80CJZ will sense the

input AC voltage to the BRL pin by an AC hold up circuit and 2 potential divider resistors.

In some applications, it needs the IC to continue to work for certain time when AC voltage is disconnected. After that, the IC will stop working. If the brownout connection is taping from the bulk capacitor, the delay time is too short. Therefore, it needs the brown out detetction at the AC input (Figure 30). The $C_{BR0}$ is charged up by AC line voltage through $R_{BO0}$, which is then fed to BRL pin through a voltage divider. When the AC voltage drops, if the BRL pin voltage is lower than 1V for 270µs, the ICE3ARxx80CJZ will go into brownout mode. If, however, the AC line goes up again, the BRL voltage will be larger than 1.25V and the ICE3ARxx80CJZ will leave brown out mode and recover to normal operation.

The brownout mode is default "ON" during the system starts up. When the system is powered up, the bulk capacitor and the Vcc capacitor are charged up at the same time. When the Vcc voltage is charged to >8V, the brownout circuit starts to operate (Figure 30). Since the UVLO is still at low level as the Vcc voltage does not reach the 17V UVLO "ON" voltage. The NAND gate G20 will release a low signal to the flip flop FF2 and the negative output of FF2 will release a high signal. Hence it is in brownout mode during the system starts up.

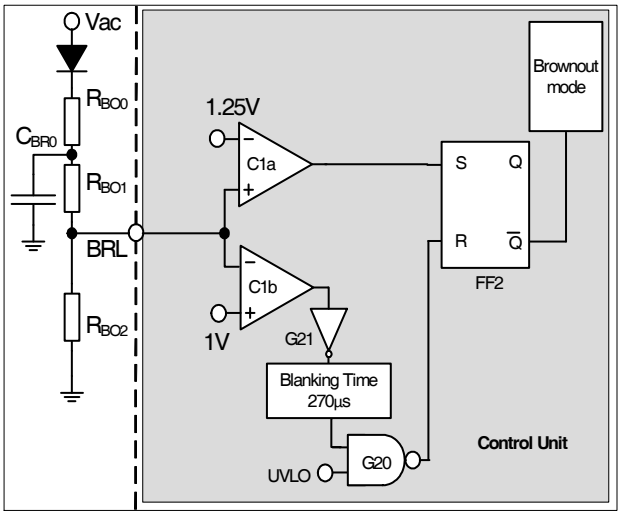



*Figure 30 Brownout detection circuit*

Once the system enters the brownout mode, there will be no switching pulse and the IC enters into another type auto-restart mode which is similar to the protection auto-restart mode but the IC will monitor the BRL signal in each restart cycle (Figure 31).

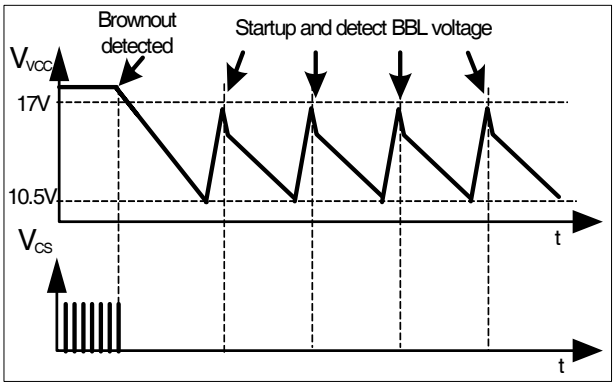



*Figure 31 Brownout mode waveform*

If the brownout feature is not needed, it needs to tie the BRL pin to the Vcc pin through a current limiting resistor, 5MΩ~10MΩ. The BRL pin cannot be in floating condition.

### 3.7.4 Fast AC reset

During normal operation, the ICE3ARxx80CJZ can be latched by pulling down the BRL voltage below 0.4V for 210µs. There are 2 condtions to reset the latch feature. The first one is to pull down the Vcc voltage to below 8V. However, the Vcc drop would take quite a long time if it is by normal AC power down. The second one is to have a slow rise time of the BRL voltage from 0.4V to 1V for at least 450µs after the BRL pin is pulled down. This timing can be achieved by the AC recycle. And it is also called the fast AC reset (Figure 32).

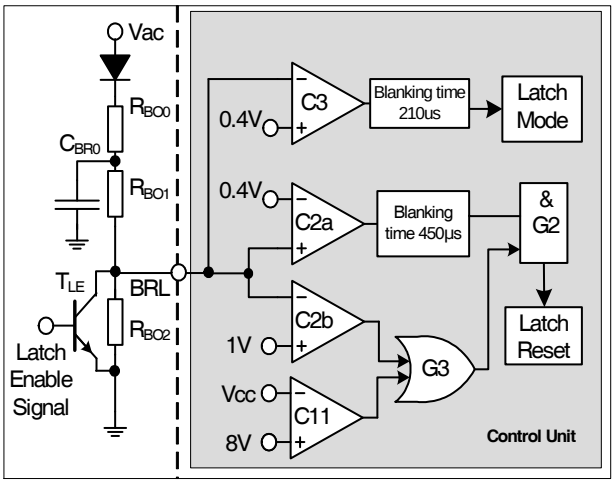



*Figure 32 Latch and fast AC reset*

Figure 33 shows different latch and reset cases.

Case a : not latched (solid line); the timing below 0.4V is 150µs and is less than 210µs.

Case b : latched (dashed line); the timing below 0.4V is 450µs which is larger than 210µs. No latch reset as the rise time from 0.4V to 1V is 300µs which is less than the 450µs.

Case c : latched and reset (dotted line); the timing below 0.4V is 710µs which is larger than 210µs. But the rise time from 0.4V to 1V is 560µs which is larger than the latch reset blanking time of 450µs.

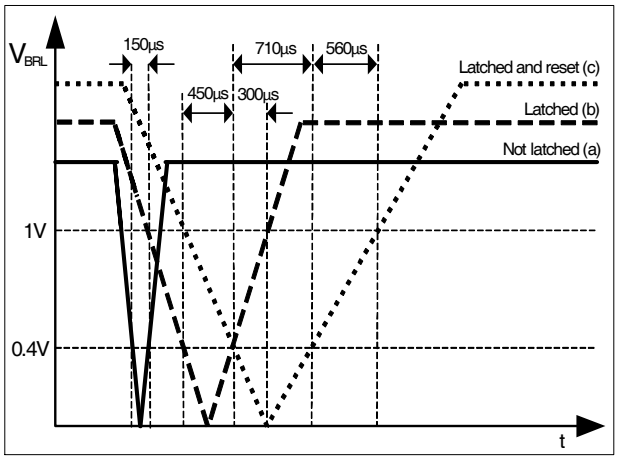



*Figure 33 Latch and fast AC reset example*

# 4 Electrical Characteristics

*Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.*

## 4.1 Absolute Maximum Ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit. $T_a$=25°C unless otherwise specified.*

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Drain Source Voltage | $V_{DS}$ | - | 800 | V | |
| Pulse drain current, $t_p$ limited by $T_{jmax}$ | $I_{D_Puls}$ | - | 1.10 | A | |
| Avalanche energy, repetitive $t_{AR}$ limited by max. $T_j$=150°C[1)] | $E_{AR}$ | - | 0.011 | mJ | |
| Avalanche current, repetitive $t_{AR}$ limited by max. $T_j$=150°C | $I_{AR}$ | - | 0.44 | A | |
| VCC Supply Voltage | $V_{VCC}$ | -0.3 | 27 | V | |
| FBB Voltage | $V_{FBB}$ | -0.3 | 5.5 | V | |
| BRL Voltage | $V_{BRL}$ | -0.3 | 5.5 | V | |
| CS Voltage | $V_{CS}$ | -0.3 | 5.5 | V | |
| Junction Temperature | $T_j$ | -40 | 150 | °C | Controller & CoolMOS® |
| Storage Temperature | $T_S$ | -55 | 150 | °C | |
| Thermal Resistance Junction -Ambient | $R_{thJA}$ | - | 96 | K/W | |
| Soldering temperature, wavesoldering only allowed at leads | $T_{sold}$ | - | 260 | °C | 1.6mm (0.063in.) from case for 10s |
| ESD Capability (incl. Drain Pin) | $V_{ESD}$ | - | 2 | kV | Human body model[2)] |

1) Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$

2) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

## 4.2 Operating Range

*Note: Within the operating range the IC operates as described in the functional description.*

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| VCC Supply Voltage | $V_{VCC}$ | $V_{VCCoff}$ | 24.7 | V | Max value limited due to Vcc OVP |
| Junction Temperature of Controller | $T_{jCon}$ | -25 | 130 | °C | Max value limited due to thermal shut down of controller |
| Junction Temperature of CoolMOS® | $T_{jCoolMOS}$ | -25 | 150 | °C | |

## 4.3 Characteristics

### 4.3.1 Supply Section

*Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range $T_J$ from – 25 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of $V_{CC}$ = 17 V is assumed.*

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Start Up Current | $I_{VCCstart}$ | - | 210 | 300 | µA | $V_{VCC}$ =16V |
| VCC Charge Current | $I_{VCCcharge1}$ | - | - | 5.0 | mA | $V_{VCC}$ = 0V |
| | $I_{VCCcharge2}$ | 0.55 | 1.0 | 1.60 | mA | $V_{VCC}$ = 1V |
| | $I_{VCCcharge3}$ | 0.38 | 0.75 | - | mA | $V_{VCC}$ =16V |
| Leakage Current of Start Up Cell and CoolMOS® | $I_{StartLeak}$ | - | 0.2 | 50 | µA | $V_{Drain}$ = 650V at $T_j$=100°C [1)] |
| Supply Current with Inactive Gate | $I_{VCCsup1}$ | - | 1.9 | 3.2 | mA | |
| Supply Current with Active Gate | $I_{VCCsup2}$ | - | 3.4 | 4.8 | mA | $I_{FBB}$ = 0A |
| Supply Current in Latched Off Mode with Inactive Gate | $I_{VCClatch}$ | - | 420 | - | µA | $I_{FBB}$ = 0A |
| Supply Current in Auto Restart Mode with Inactive Gate | $I_{VCCrestart}$ | - | 420 | - | µA | $I_{FBB}$ = 0A |
| Supply Current in Active Burst Mode with Inactive Gate | $I_{VCCburst1}$ | - | 620 | 950 | µA | $V_{FBB}$ = 2.5V |
| | $I_{VCCburst2}$ | - | 620 | 950 | µA | $V_{VCC}$ = 11.5V, $V_{FBB}$ = 2.5V |
| VCC Turn-On Threshold<br>VCC Turn-Off Threshold<br>VCC Turn-On/Off Hysteresis | $V_{VCCon}$<br>$V_{VCCoff}$<br>$V_{VCChys}$ | 16.0<br>9.8<br>- | 17.0<br>10.5<br>6.5 | 18.0<br>11.2<br>- | V<br>V<br>V | |

[1)] The parameter is not subjected to production test - verified by design/characterization

### 4.3.2 Internal Voltage Reference

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Trimmed Reference Voltage | $V_{REF}$ | 4.90 | 5.00 | 5.10 | V | measured at pin FBB $I_{FBB}$ = 0A |

### 4.3.3 PWM Section

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Fixed Oscillator Frequency | $f_{OSC1}$ | 87 | 100 | 113 | kHz | |
| | $f_{OSC2}$ | 92 | 100 | 108 | kHz | $T_j$ = 25°C |
| Frequency Jittering Range | $f_{jitter}$ | - | ±4.0 | - | kHz | $T_j$ = 25°C |
| Frequency Jittering period | $T_{jitter}$ | - | 4.0 | - | ms | $T_j$ = 25°C |
| Max. Duty Cycle | $D_{max}$ | 0.70 | 0.75 | 0.80 | | |
| Min. Duty Cycle | $D_{min}$ | - | - | 0 | | $V_{FBB}$ < 0.3V |
| PWM-OP Gain | $A_V$ | 3.17 | 3.25 | 3.33 | | |
| Voltage Ramp Offset | $V_{Offset\text{-}Ramp}$ | - | 0.60 | - | V | |
| $V_{FBB}$ Operating Range Min Level | $V_{FBmin}$ | - | 0.7 | - | V | |
| $V_{FBB}$ Operating Range Max level | $V_{FBmax}$ | - | - | 4.4 | V | $dV_{sense}/dt$ = 0.134V/µs , limited by Comparator C4[1)] |
| FBB Pull-Up Resistor | $R_{FB}$ | 9.0 | 15.4 | 22.0 | kΩ | |
| Slope Compensation rate | $M_C$ | 45 | 50 | 55 | mV/µs | CS=0V |

1) The parameter is not subjected to production test - verified by design/characterization

### 4.3.4 Soft Start time

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Soft Start time | $t_{SS}$ | - | 10 | - | ms | |

### 4.3.5 Control Unit

| Parameter | | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| Brownout reference voltage for comparator C1a | | $V_{BO_L}$ | 1.14 | 1.25 | 1.36 | V | |
| Brownout reference voltage for comparator C1b | | $V_{BO_E}$ | 0.91 | 1 | 1.09 | V | |
| Leakage current of BRL pin | | $I_{leakage}$ | -0.5 | - | 0.5 | µA | |
| Blanking time to enter brownout mode | | $V_{BKC1b}$ | 190 | 270 | 310 | µs | |
| Fast AC reset voltage for comparator C2a | | $V_{C2a}$ | 0.3 | 0.4 | 0.5 | V | |
| Fast AC reset voltage for comparator C2b | | $V_{C2b}$ | 0.91 | 1 | 1.09 | V | |
| Blanking time for comparator C2a | | $V_{BKC2a}$ | 315 | 450 | 585 | µs | |
| Charging current to select burst mode | | $I_{sel}$ | 2.8 | 3.5 | 4.2 | µA | |
| Burst mode selection reference voltage | | $V_{ref1}$ | 1.69 | 1.80 | 1.91 | V | |
| | | $V_{ref2}$ | 3.78 | 4.00 | 4.22 | V | |
| Over Load Limit for Comparator C4 | | $V_{FBC4}$ | 4.40 | 4.50 | 4.72 | V | |
| Active Burst Mode Entry level for Comparator C5 | 15% $P_{in_max}$ | $V_{FB_burst1}$ | 1.77 | 1.84 | 1.91 | V | $V_{fbb}>V_{ref2}$ |
| | 10% $P_{in_max}$ | $V_{FB_burst2}$ | 1.50 | 1.61 | 1.72 | V | $V_{ref1}<V_{fbb}<V_{ref2}$ |
| | 5% $P_{in_max}$ | $V_{FB_burst3}$ | 1.20 | 1.29 | 1.38 | V | $V_{fbb}<V_{ref1}$ |
| Active Burst Mode High Level for Comparator C6a | | $V_{FBC6a}$ | 3.35 | 3.50 | 3.65 | V | In Active Burst Mode |
| Active Burst Mode Low Level for Comparator C6b | | $V_{FBC6b}$ | 3.06 | 3.20 | 3.34 | V | |
| Active Burst Mode Level for Comparator C9 | | $V_{FBC9}$ | 3.85 | 4.00 | 4.15 | V | |
| Overvoltage Detection Limit for Comparator C2 | | $V_{VCCOVP}$ | 24.7 | 25.5 | 26.3 | V | |
| Latch enable reference voltage for Comparator C3 | | $V_{LE}$ | 0.3 | 0.4 | 0.5 | V | |
| Built-in Blanking Time to enter Latch Mode | | $t_{BK_latch}$ | 140 | 210 | 295 | µs | |
| Thermal Shutdown[1)] | | $T_{jSD}$ | 130 | 140 | 150 | °C | Controller |
| Hysteresis for thermal Shutdown[1)] | | $T_{jSD_hys}$ | - | 50 | - | °C | |
| Built-in Blanking Time for Overload Protection | | $t_{BK}$ | - | 40 | - | ms | |
| Built-in Blanking Time for entering Active Burst Mode | | $t_{BK_burst}$ | - | 20 | - | ms | |
| Spike Blanking Time for Vcc OVP | | $t_{Spike}$ | - | 150 | - | µs | |

[1] The parameter is not subjected to production test - verified by design/characterization. The thermal shutdown temperature refers to the junction temperature of the controller.

*Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except* $V_{VCCOVP}$.

### 4.3.6 Current Limiting

| Parameter | | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| Peak Current Limitation | | $V_{csth1}$ | 0.69 | 0.73 | 0.77 | V | $dV_{sense}/dt = 0.41V/\mu s$ |
| | | $V_{csth2}$ | 0.72 | 0.76 | 0.80 | V | $dV_{sense}/dt = 0.134V/\mu s$ |
| Peak Current Limitation in Active Burst Mode | 27% $P_{in_max}$ | $V_{csth_burst1}$ | 0.313 | 0.34 | 0.368 | V | $V_{fbb}>V_{ref2}$ |
| | 20% $P_{in_max}$ | $V_{csth_burst2}$ | 0.264 | 0.29 | 0.320 | V | $V_{ref1}<V_{fbb}<V_{ref2}$ |
| | 11% $P_{in_max}$ | $V_{csth_burst3}$ | 0.184 | 0.21 | 0.238 | V | $V_{fbb}<V_{ref1}$ |
| Leading Edge Blanking | Normal mode | $t_{LEB_normal}$ | - | 220 | - | ns | |
| | Burst mode | $t_{LEB_burst}$ | - | 180 | - | ns | |
| CS Input Bias Current | | $I_{CSbias}$ | -1.5 | -0.2 | - | µA | $V_{CS}$ =0V |

### 4.3.7 CoolMOS® Section

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Drain Source Breakdown Voltage | $V_{(BR)DSS}$ | 800<br>870 | -<br>- | -<br>- | V<br>V | $T_j$ = 25°C<br>$T_j$ = 110°C[1] |
| Drain Source On-Resistance | $R_{DSon}$ | -<br>-<br>- | 10.0<br>22.4<br>27.3 | 11.1<br>24.6<br>30.0 | Ω<br>Ω<br>Ω | $T_j$ = 25°C<br>$T_j$=125°C[1]<br>$T_j$=150°C[1]<br>at $I_D$ = 0.27A |
| Effective output capacitance, energy related | $C_{o(er)}$ | - | 3.3 | - | pF | $V_{DS}$ = 0V to 480V |
| Rise Time | $t_{rise}$ | - | 30[2] | - | ns | |
| Fall Time | $t_{fall}$ | - | 30[2] | - | ns | |

[1] The parameter is not subjected to production test - verified by design/characterization

[2] Measured in a Typical Flyback Converter Application

# 5 CoolMOS® Perfromance Characteristic

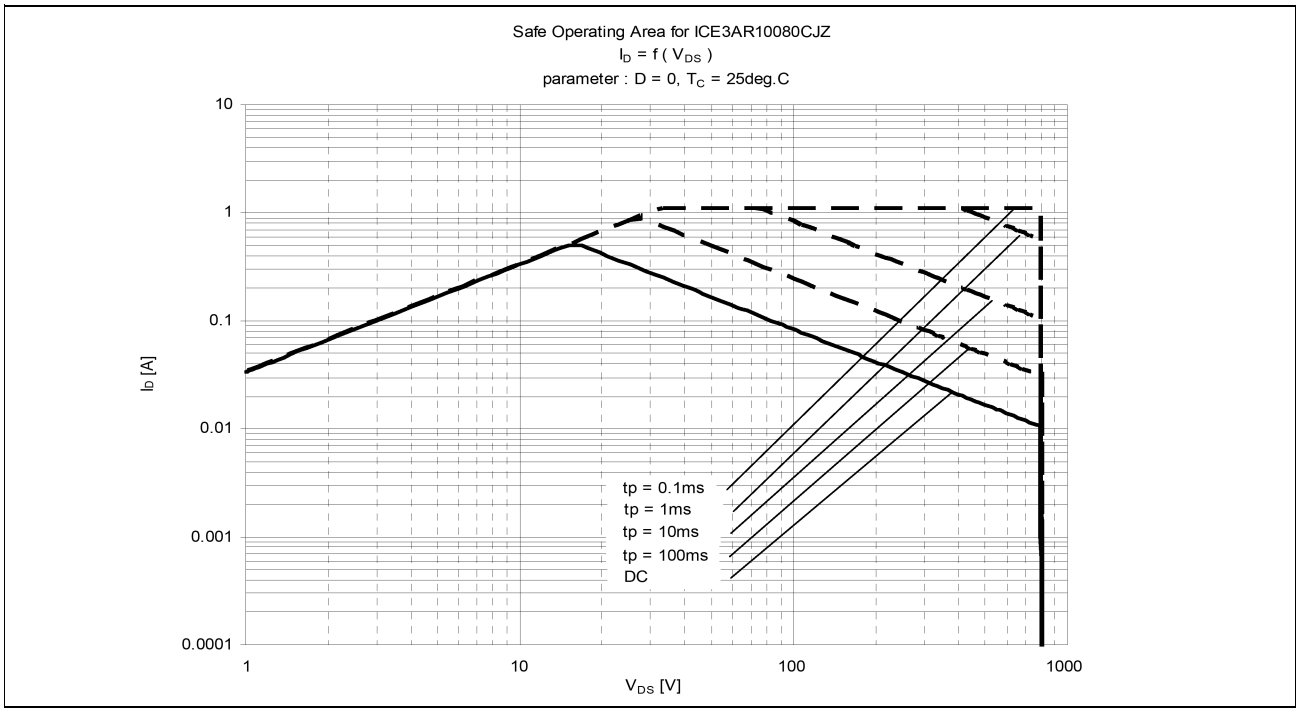



*Figure 34 Safe Operating Area (SOA) curve for ICE3AR10080CJZ*

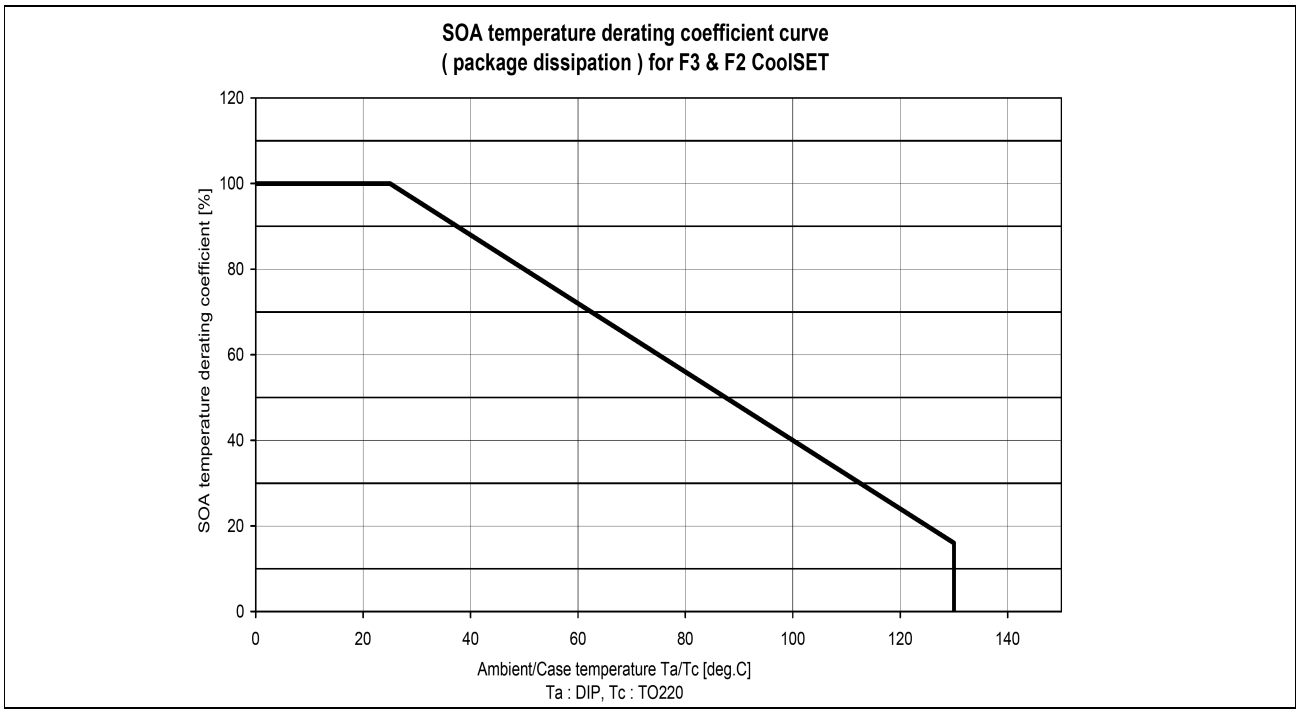



*Figure 35 SOA temperature derating coefficient curve*

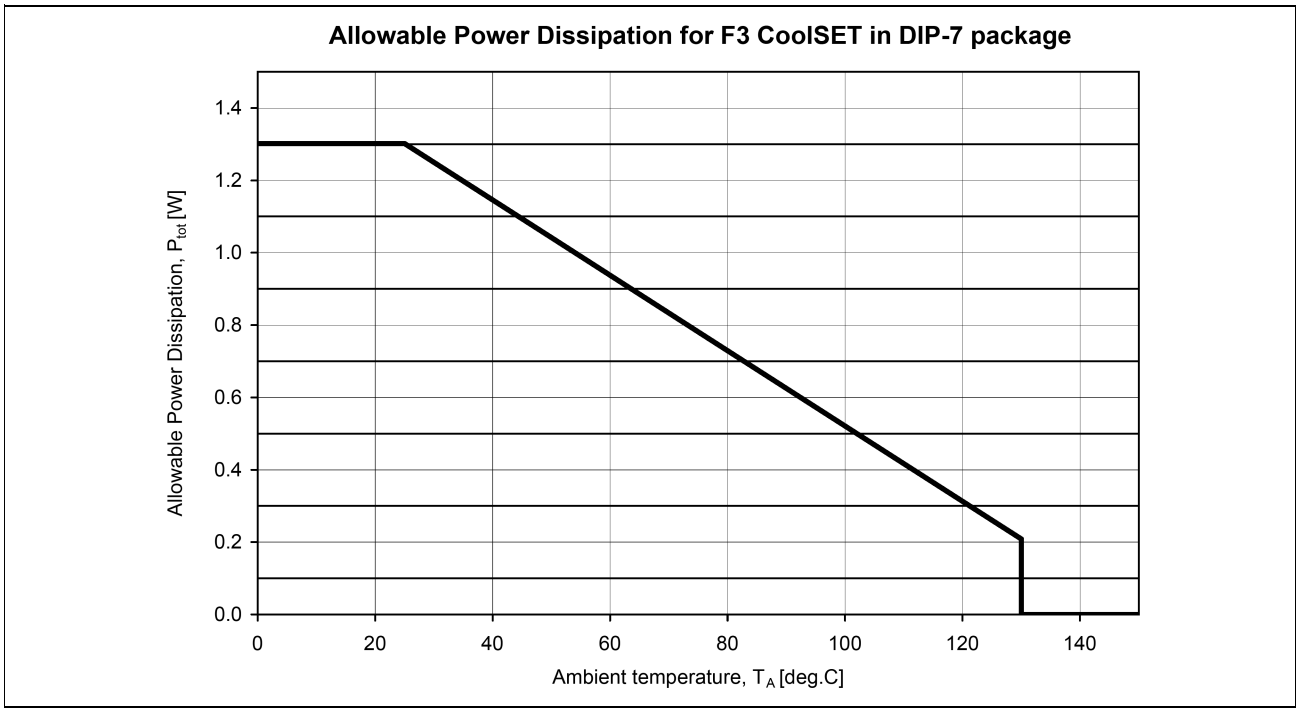



*Figure 36 Power dissipation; $P_{tot}=f(T_a)$*

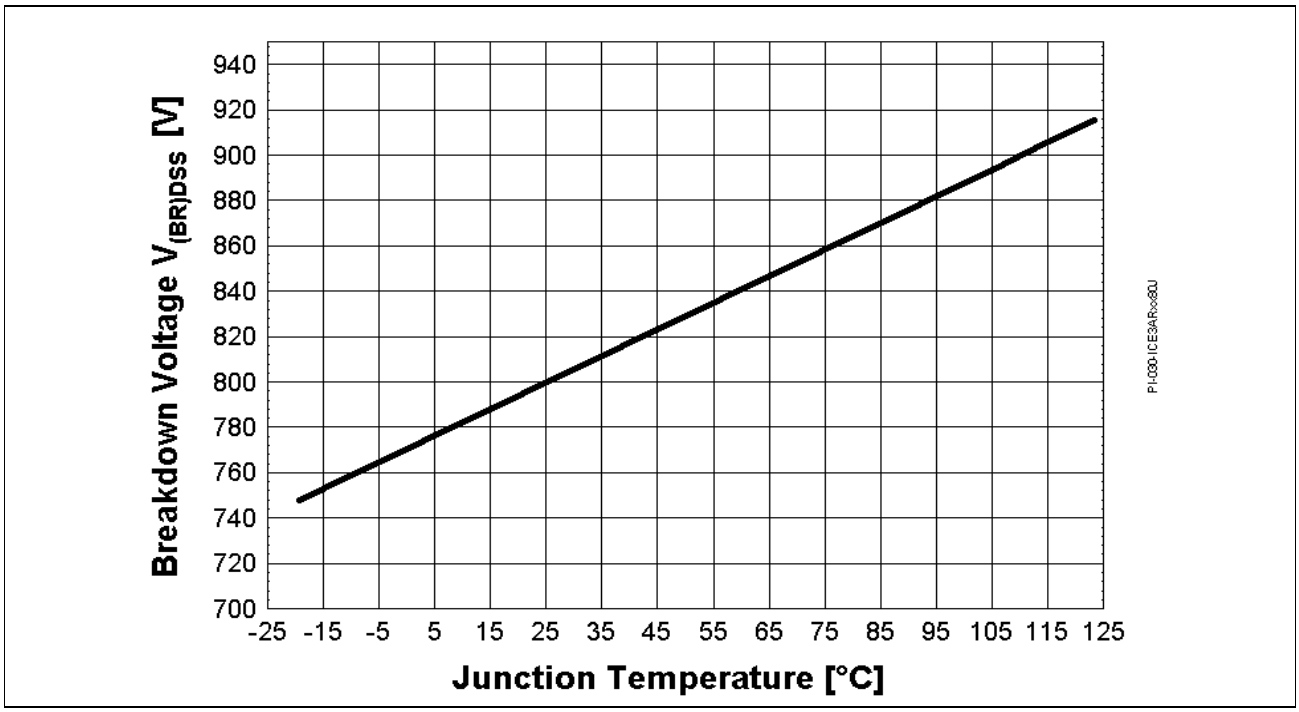



*Figure 37 Drain-source breakdown voltage; $V_{BR(DSS)}=f(T_j)$, $I_D$=0.25mA*

# 6 Input Power Curve

Two input power curves giving the typical input power versus ambient temperature are showed below; Vin=85Vac~265Vac (Figure 38) and Vin=230Vac+/-15% (Figure 39). The curves are derived based on a typical discontinuous mode flyback model which considers either 60% maximum duty ratio or 150V maximum secondary to primary reflected voltage (higher priority). The calculation is based on no copper area as heatsink for the device. The input power already includes the power loss at input common mode choke, bridge rectifier and the CoolMOS.The device saturation current ($I_{D_Puls}$ @ $T_j$=125°C) is also considered.

To estimate the output power of the device, it is simply multiplying the input power at a particular operating ambient temperature with the estimated efficiency for the application. For example, a wide range input voltage (Figure 38), operating temperature is 50°C, estimated efficiency is 85%, then the estimated output power is 12W (15W * 85%).

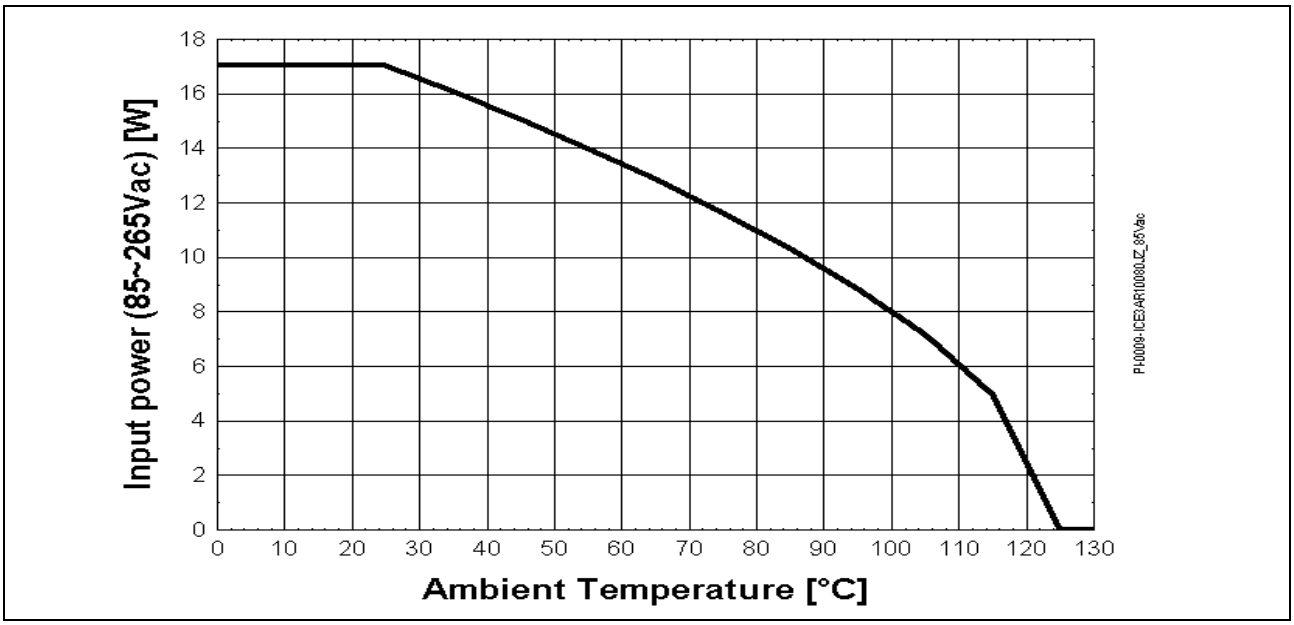



*Figure 38 Input power curve Vin=85~265Vac; $P_{in}=f(T_a)$*

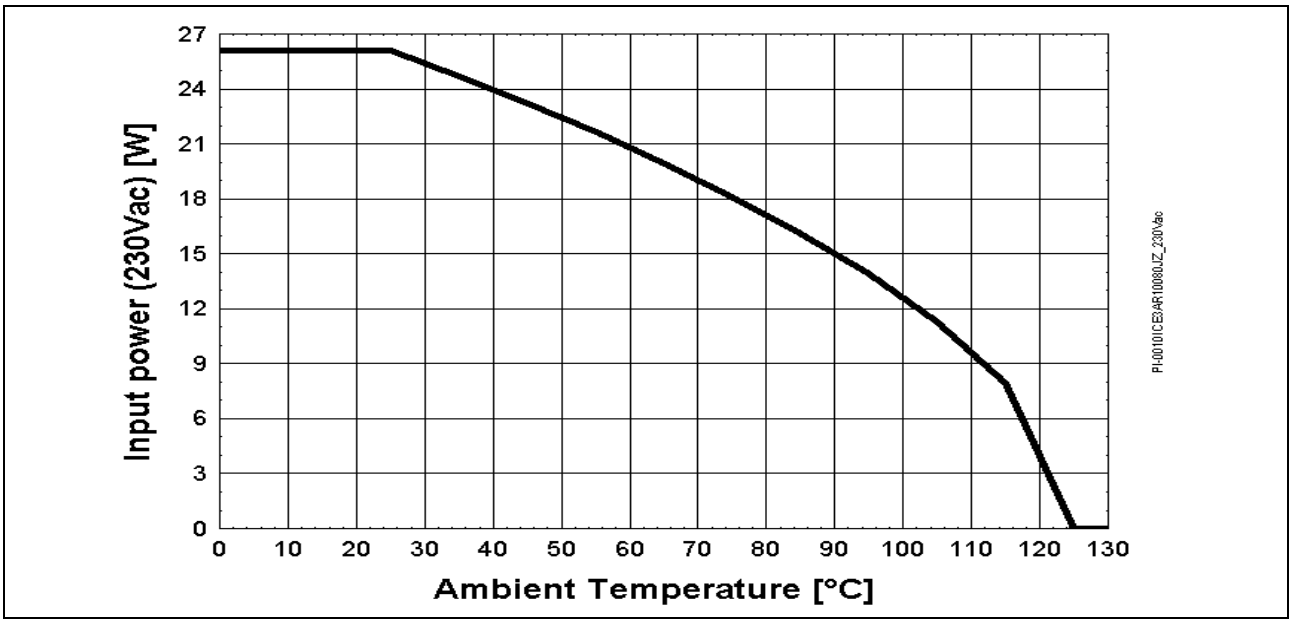
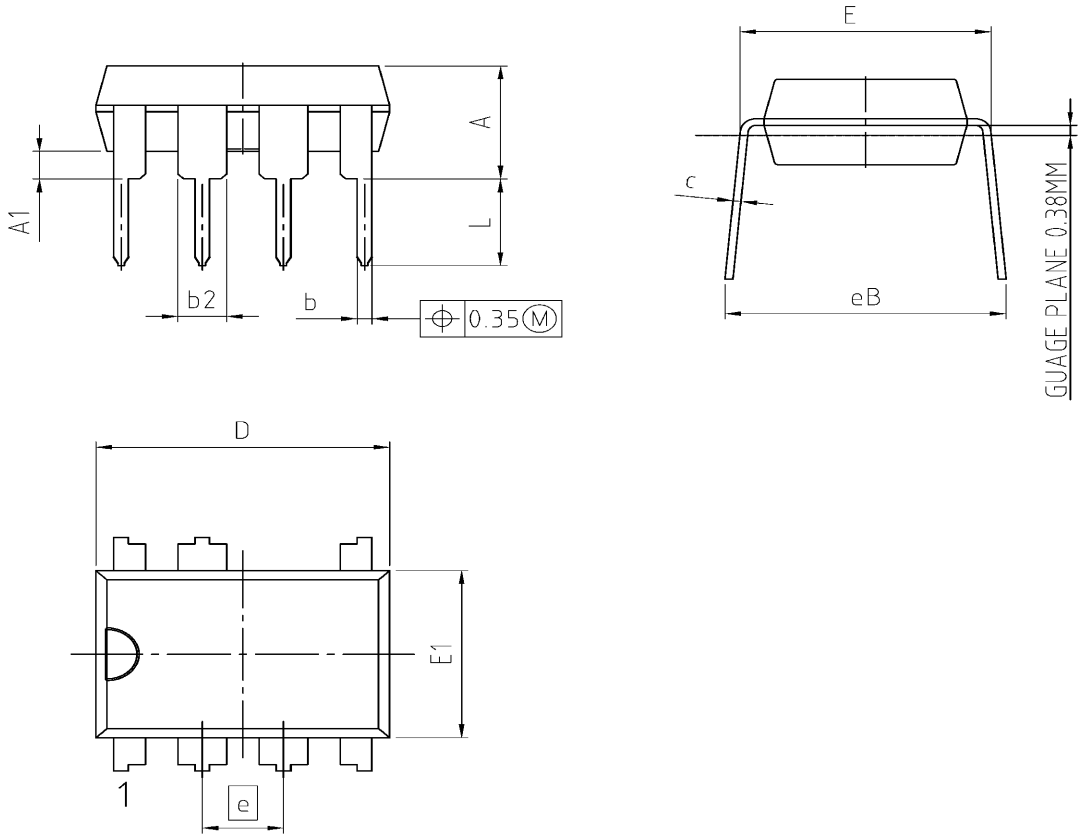



*Figure 39 Input power curve Vin=230Vac+/-15%; $P_{in}=f(T_a)$*

# 7 Outline Dimension

**PG-DIP-7**
**(Plastic Dual In-Line Outline)**




1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | - | 4.57 | - | 0.180 |
| A1 | 0.38 | - | 0.015 | - |
| b | 0.36 | 0.56 | 0.014 | 0.022 |
| b2 | - | 1.70 | - | 0.067 |
| c | 0.20 | 0.36 | 0.008 | 0.014 |
| D | 9.10 | 9.77 | 0.358 | 0.385 |
| E | 7.49 | 8.26 | 0.295 | 0.325 |
| E1 | 6.10 | 6.60 | 0.240 | 0.260 |
| e | 2.54 BSC | | 0.1 BSC | |
| N | 7 | | 7 | |
| eB | 7.90 | 10.90 | 0.311 | 0.429 |
| L | 2.92 | - | 0.115 | - |

DOCUMENT NO.
Z8B00155542

SCALE 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
22.07.2011

REVISION
02

*Figure 40 PG-DIP-7 (Pb-free lead plating Plastic Dual-in-Line Outline)*

# 8 Marking

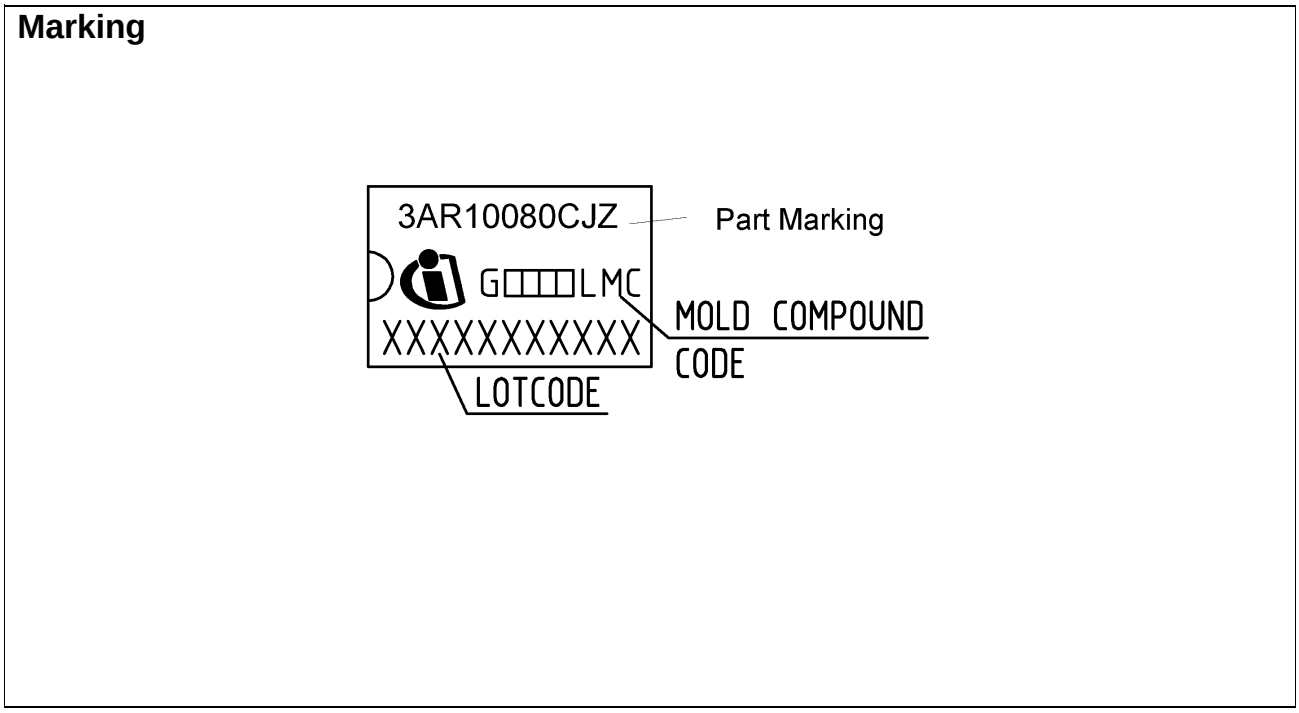



*Figure 41 Marking for ICE3AR10080CJZ*

# 9 Schematic for recommended PCB layout

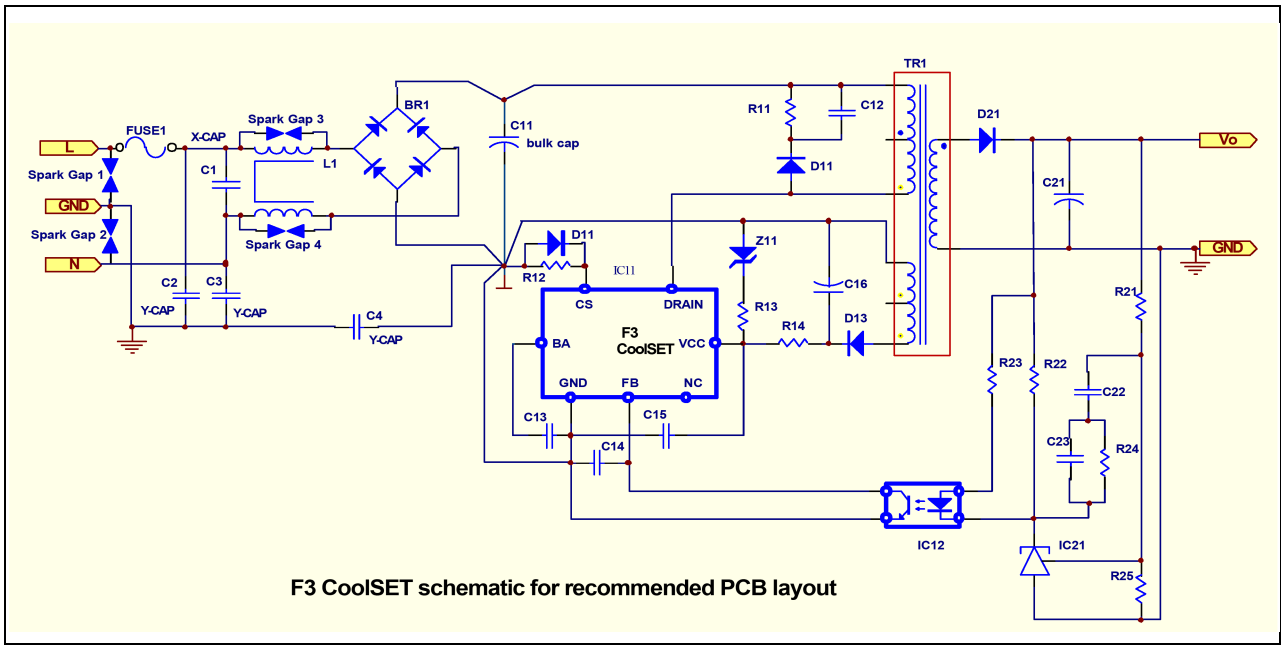



*Figure 42 Schematic for recommended PCB layout*

General guideline for PCB layout design using F3 CoolSET (refer to Figure 42):

1. “Star Ground “at bulk capacitor ground, C11:

   “Star Ground “means all primary DC grounds should be connected to the ground of bulk capacitor C11 separately in one point. It can reduce the switching noise going into the sensitive pins of the CoolSET device effectively. The primary DC grounds include the followings.

   a. DC ground of the primary auxiliary winding in power transformer, TR1, and ground of C16 and Z11.

   b. DC ground of the current sense resistor, R12

   c. DC ground of the CoolSET device, GND pin of IC11; the signal grounds from C13, C14, C15 and collector of IC12 should be connected to the GND pin of IC11 and then “star “connect to the bulk capacitor ground.

   d. DC ground from bridge rectifier, BR1

   e. DC ground from the bridging Y-capacitor, C4

2. High voltage traces clearance:

   High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.

   a. 400V traces (positive rail of bulk capacitor C11) to nearby trace: > 2.0mm

   b. 600V traces (drain voltage of CoolSET IC11) to nearby trace: > 2.5mm

3. Filter capacitor close to the controller ground:

   Filter capacitors, C13, C14 and C15 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.

Guideline for PCB layout design when >3KV lightning surge test applied (refer to Figure 42):

1. Add spark gap

   Spark gap is a pair of saw-tooth like copper plate facing each other which can discharge the accumulated charge during surge test through the sharp point of the saw-tooth plate.

   a. Spark Gap 3 and Spark Gap 4, input common mode choke, L1:

   Gap separation is around 1.5mm (no safety concern)

b. Spark Gap 1 and Spark Gap 2, Live / Neutral to GROUND:

These 2 Spark Gaps can be used when the lightning surge requirement is >6KV.

230Vac input voltage application, the gap separation is around 5.5mm

115Vac input voltage application, the gap separation is around 3mm

2. Add Y-capacitor (C2 and C3) in the Live and Neutral to ground even though it is a 2-pin input
3. Add negative pulse clamping diode, D11 to the Current sense resistor, R12:

The negative pulse clamping diode can reduce the negative pulse going into the CS pin of the CoolSET and reduce the abnormal behavior of the CoolSET. The diode can be a fast speed diode such as IN4148.

The principle behind is to drain the high surge voltage from Live/Neutral to Ground without passing through the sensitive components such as the primary controller, IC11.

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