CoolSET™ SiP System in Package ICE1 Family - 100EM series

Features

RoHS
Green
Halogen-free
Lead-free

- Integrated 800 V avalanche rugged CoolMOS™ P7
- Fast startup with integrated 950 V startup-cell
- Integrated synchronous rectification (SR) driver with typical 10 V output
- Integrated reinforced isolated communication from secondary to primary side
- Integrated general purpose isolated enable signal path from secondary to primary side
- Novel zero voltage switching (ZVS) flyback operation for lowest switching losses and low electromagnetic interference (EMI) signature
- Reliable pulse width modulation (PWM) switching operation by synchronized timing of primary and secondary side SR switch
- Supports primary side wide VCC operating range up to 29 V
- Optimized low supply currents for hysteretic mode operation to reach stand-by power < 50 mW
- Built-in secondary side feedback control loop with error amplifier
- Multi-mode control for optimized efficiency across the entire load range
- Auto-restart mode protection for VCC over/undervoltage, overload/open-loop, line/output overvoltage, overtemperature

Potential applications

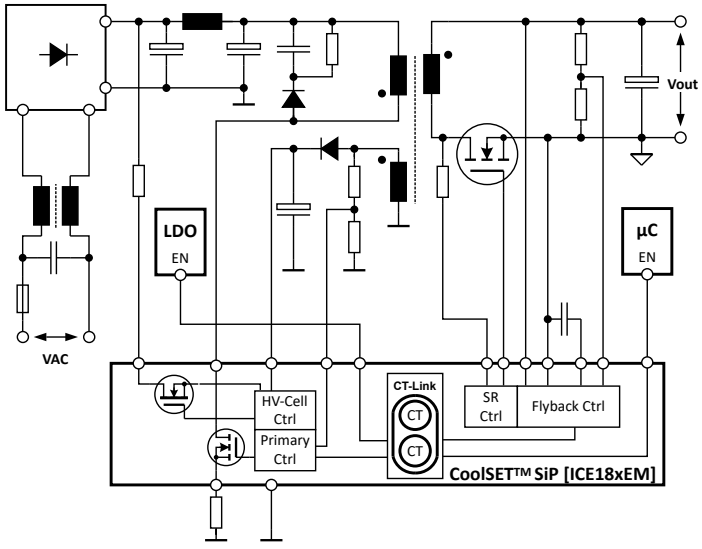
- Auxiliary power supply for home appliances
- General SMPS

Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22, and J-STD-020.
- Pending reinforced isolation certification according to IEC 60747-17 (VDE 0884-17), UL 1577, CQC (GB4943.1) to meet IEC 62368-1, IEC 61010-1, IEC 60355-1, CQC isolation requirements

Description

The CoolSET SiP 100EM series (ICE1xxEM-Vxxx) enables effective reduction of system complexity. A high amount of discrete system components can be removed due to system forward integration. Beside the integration of the high voltage power switch and control on primary side, also the secondary side SR control and regulation loop is integrated. The timings of primary side power switch control and secondary side SR control are matched and enable reliable and robust operation under all switching conditions. The used coreless transformer technology (CT-Link) provides reinforced and safe isolated communication between primary and secondary side. Advanced PWM switching pattern forces a quasi-resonant ZVS flyback operation, reducing the turn-on switching losses and optimizing EMI signature. An advanced set of protection features supports ease of design-in.



Output power table

Product[1]	$V_{(BR)DSS}$[2]	$R_{DS(on)(max)}$[3]	230 V_{AC} ± 15%[4]	85 to 320 V_{AC}[4]	385 V_{DC}[4]
ICE183EM	800 V	2.18 Ω	46 W	30 W	52 W
ICE184EM	800 V	0.84 Ω	73 W	48 W	84 W
ICE186EM	800 V	0.48 Ω	95 W	64 W	110 W

[1] PG-DSO-27-1 package
[2] CoolMOS™ P7
[3] at T_J = 25 °C
[4] Min. continous power in an open frame design at T_A = 40°C, T_J = 125°C, minimum copper area of 232 mm² in a 2 oz copper single sided PCB at DRAIN pin and GNDS pin. Max. power is dependent on the system design.

Typical application

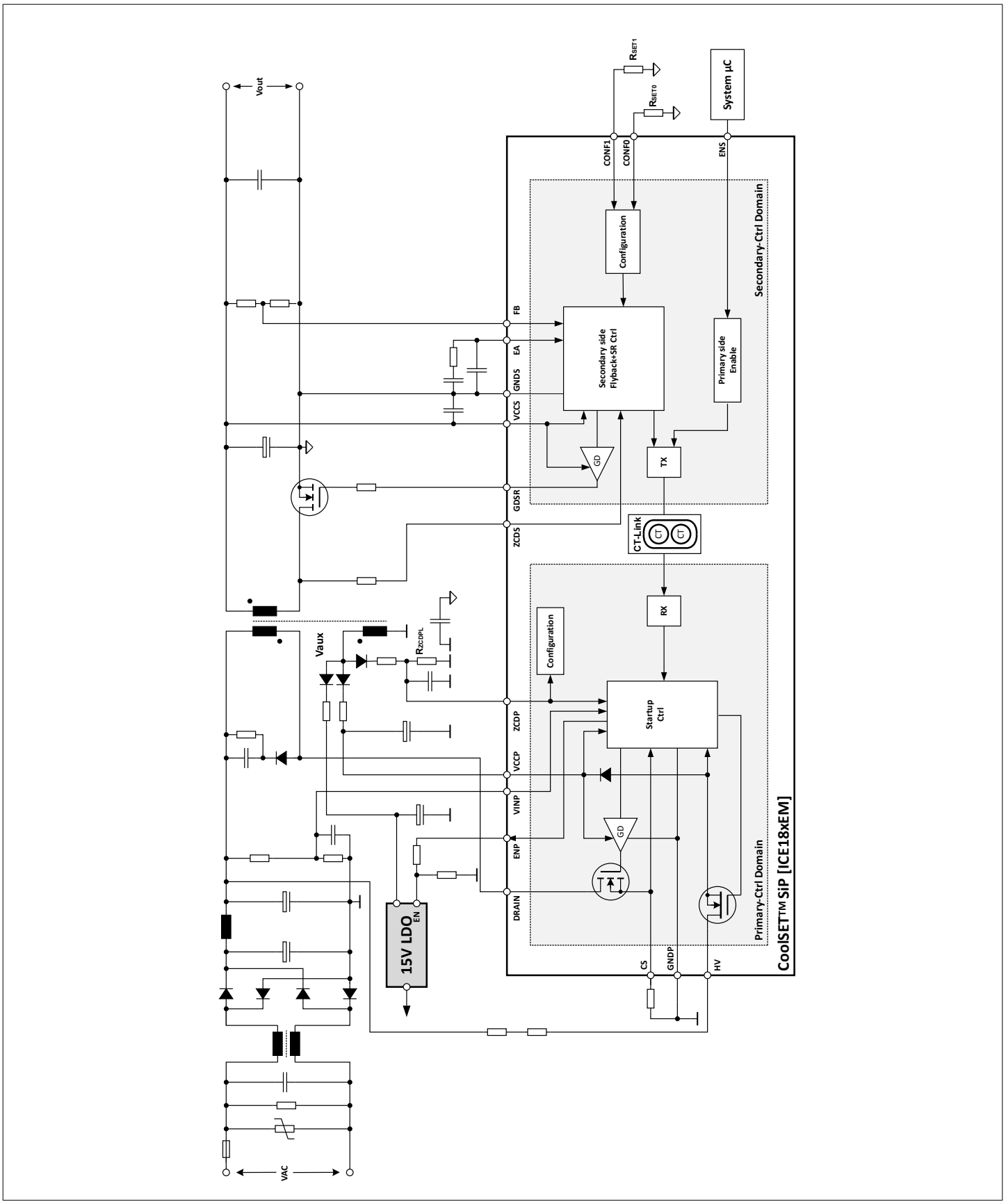


Table of contents

1 Pin configuration and functionality

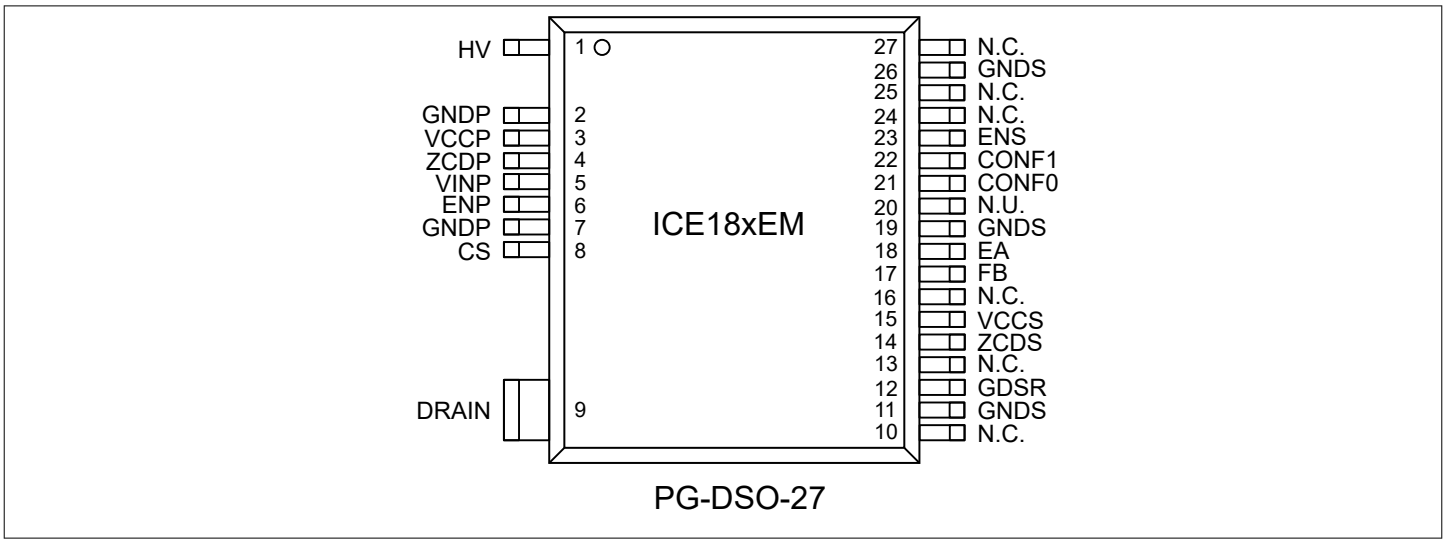


Figure 1 Pin configuration

Table 1 Pin functionality

Symbol	Pin	Type	Function
HV	1	I	**High voltage** HV pin is connected via a series resistor to VIN node.
GNDP	2	O	**Ground primary side** Power and signal ground.
VCCP	3	IO	**Voltage supply primary side** Primary side power supply.
ZCDP	4	I	**Zero-crossing detection primary side** ZCDP pin is connected to the auxiliary winding of the transformer via a resistor divider and diode.
VINP	5	I	**Input voltage sensing primary side** VINP pin is connected to a resistor divider for measuring the voltage at the bulk capacitor.
ENP	6	O	**Enable signal primary side** The signal from ENP pin can enable/disable an external component based on the input signal on secondary side at ENS pin.
GNDP	7	O	**Ground primary side** Power and signal ground.
CS	8	IO	**Current sensing primary side** CS pin is connected to a shunt resistor for measuring the primary side current ramp during turn-on phase.
DRAIN	9	I	**Drain** DRAIN of internal high voltage power switch.

(table continues...)

Table 1 (continued) Pin functionality

Symbol	Pin	Type	Function
N.C.	10	-	Keep open, must be not connected to ensure minimum creepage distance between primary and secondary side > 8 mm.
GNDS	11	O	**Ground secondary side** Power and signal ground.
GDSR	12	O	**SR gate driver** GDSR pin is connected to the gate of the SR power switch.
N.C.	13	-	Not connected. Connect to GNDS.
ZCDS	14	I	**Zero-crossing detection secondary side** ZCDS pin is connected to the secondary side output winding of the transformer via a resistor.
VCCS	15	I	**Voltage supply secondary side** Controller secondary side power supply
N.C.	16	-	Not connected. Connect to GNDS.
FB	17	I	**Feedback** FB pin is connected via resistor divider to the output voltage rail.
EA	18	IO	**Error amplifier** EA pin is connected to the external compensation network.
GNDS	19	O	**Ground secondary side** Power and signal ground.
N.U.	20	-	Not used. Connect to GNDS.
CONF0	21	I	**Configuration setting 0** CONF0 pin is connected to a resistor for setting the transformer winding ratio parameter.
CONF1	22	I	**Configuration setting 1** CONF1 pin is connected to a resistor for setting the target parameter table.
ENS	23	I	**Enable signal secondary side** The signal at ENS pin is internally sent to the primary side ENP pin.
N.C.	24, 25	-	Not connected. Connect to GNDS.
GNDS	26	O	**Ground secondary side** Power and signal ground.
N.C.	27	-	Keep open, must not be connected to ensure minimum creepage distance between primary and secondary side > 8 mm.

2 Representative block diagram

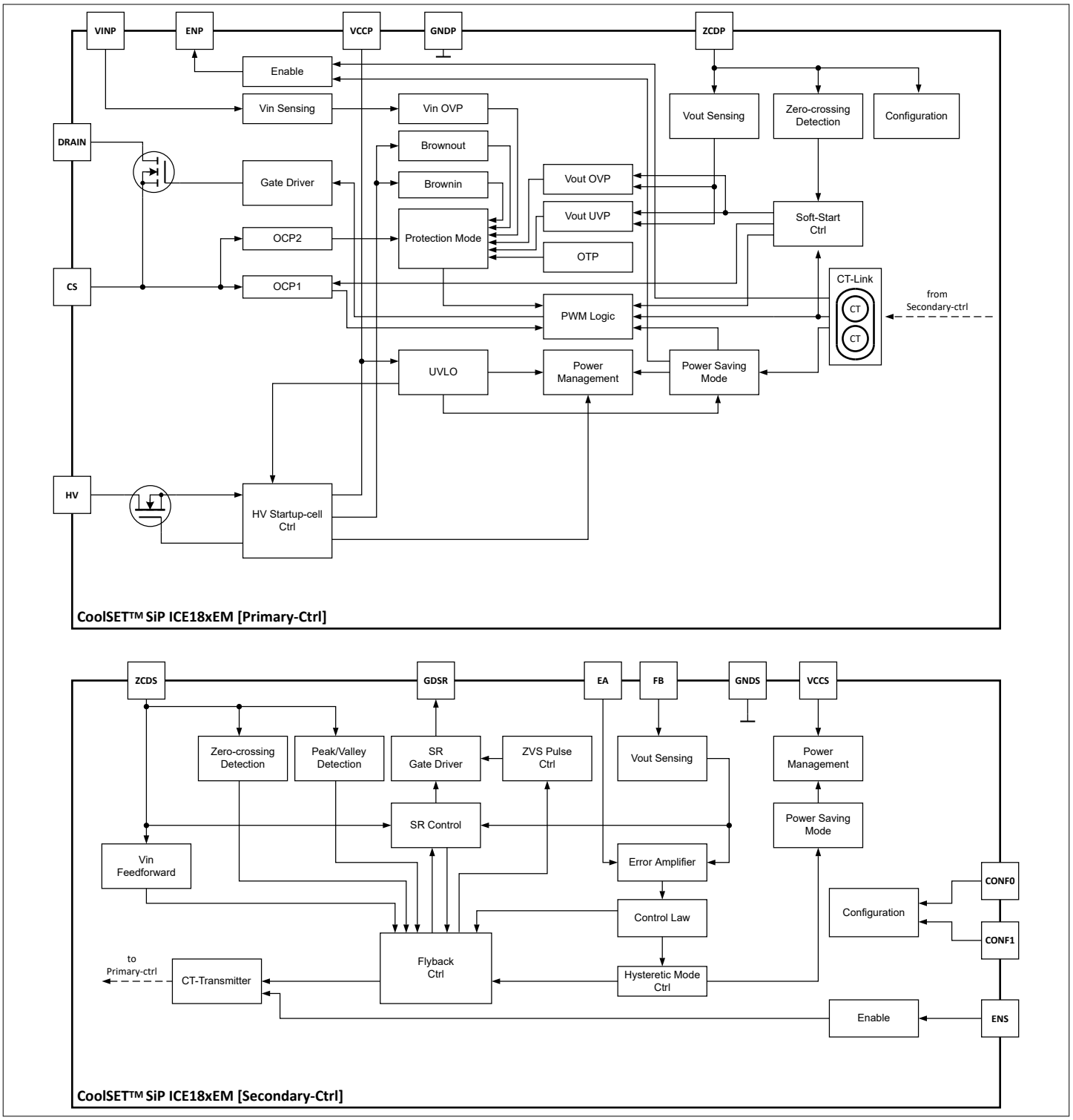


Figure 2 Block diagram CoolSET™ SiP ICE18xEM

3 Functional description

The functional description gives an overview about the integrated functions and features and their relationship. The numerical values of the mentioned parameters are shown in Chapter 4.

3.1 Introduction

The CoolSET™-SiP ICE1 product enables significant system forward integration for a flyback topology based switching mode power supply (SMPS). In one package it integrates the primary side control, the primary side power switch, the secondary side control for feedback loop and synchronous rectification (SR). Furthermore, the HV startup-cell is providing a switchable high voltage low impedance sensing path. The communication from secondary side to primary side is performed via coreless transformer reinforced isolation barrier.

3.2 Power supply management

The power supply management is separated for the primary and secondary side isolated power supply domains (VCCP, GNDP) and (VCCS, GNDS).

3.2.1 Primary VCCP capacitor charge-up and startup sequence

A 950 V HV startup-cell charges up the VCCP capacitor with a two steps constant current source $I_{VCCPCharge1}$ and $I_{VCCPCharge2}$. In phase I, a smaller constant current source $I_{VCCPCharge1}$ charges the VCCP capacitor until V_{VCCP} reaches $V_{VCCPstart}$. After this phase, the phase II higher constant current source $I_{VCCPCharge2}$ charges the VCCP capacitor further, until V_{VCCP} exceeds the turn on threshold $V_{VCCPon.}$ Once V_{VCCP} has reached the V_{VCCPon} level, the primary side controller power management module is powered up and the configuration is loaded according defined hardware configuration in phase II. After phase II, the primary controller starts switching with soft-start if VIN is higher than the threshold sensed with I_{HV_BI} and lower than the threshold V_{VINP_LOVP}, and the primary side controller die junction temperature is lower than the overtemperature threshold T_{JPOTP}.

3.2.2 Secondary VCCS startup sequence

The secondary side controller is supplied by the VCCS pin. When connected to the output voltage, the supply voltage ramps up during the primary side soft-start phase. After V_{VCCS} exceeds the threshold V_{VCCSon} and additionally V_{FB} exceeds the threshold $V_{FBstart}$, the secondary side starts to take over the PWM control.

3.3 Control features

This chapter describes the flyback control features for the primary and secondary side.

3.3.1 High voltage sensing via HV startup-cell at HV pin

The controller senses the rectified input voltage through the HV pin using the integrated HV startup-cell and the external HV resistor R_{HV} connected to the input voltage V_{IN} as shown in Figure 3. The sensing is based on a periodic sampling instead of continuous sampling to reduce the power loss. The corresponding input voltage to the internal brownin and brownout current thresholds I_{HV_BI} and I_{HV_BO} can be adjusted via the external HV resistor R_{HV}.

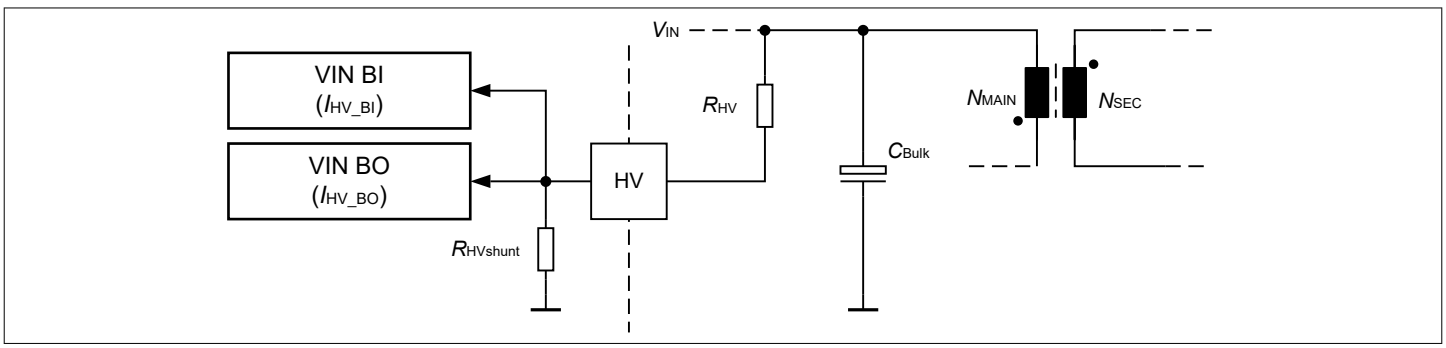


Figure 3 HV pin sensing for brownin/brownout protection

3.3.2 HV sensing via VINP pin

The controller senses the rectified input line voltage via the VINP pin for line overvoltage protection by two resistors, R_{VINH} and R_{VINL} as shown in Figure 4.

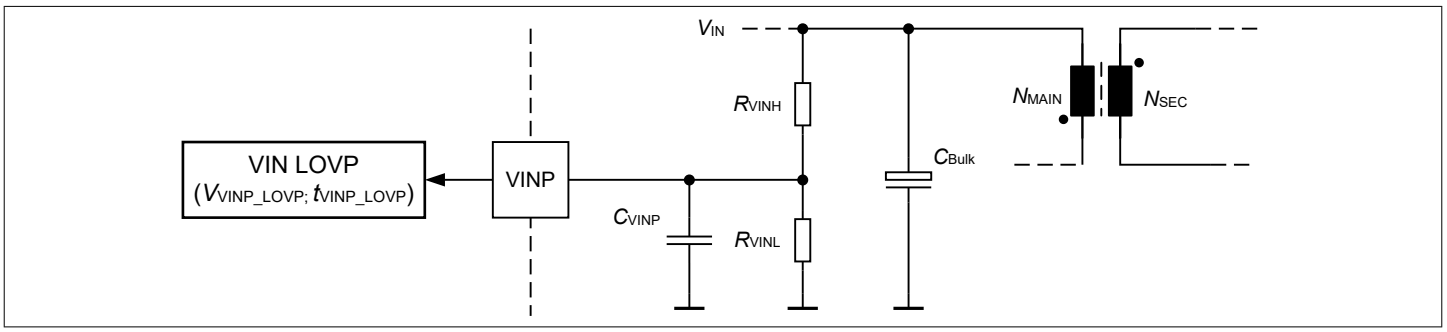


Figure 4 VINP pin sensing

3.3.3 Primary current sensing at CS pin

In the primary side controller, the primary transformer winding current is monitored by converting it to a voltage using the external shunt resistor R_{CS} as shown in Figure 5.

This information is used for the following features:

- Peak current limitation during soft-start
- Maximum peak current limitation OCP1 during normal operation
- Primary overcurrent protection OCP2 during fault condition

To avoid mis-triggering caused by a voltage spike across the external shunt resistor at the turn-on of the primary side power switch, a leading edge blanking (LEB) filter with $t_{OCP1LEB}$ is integrated.

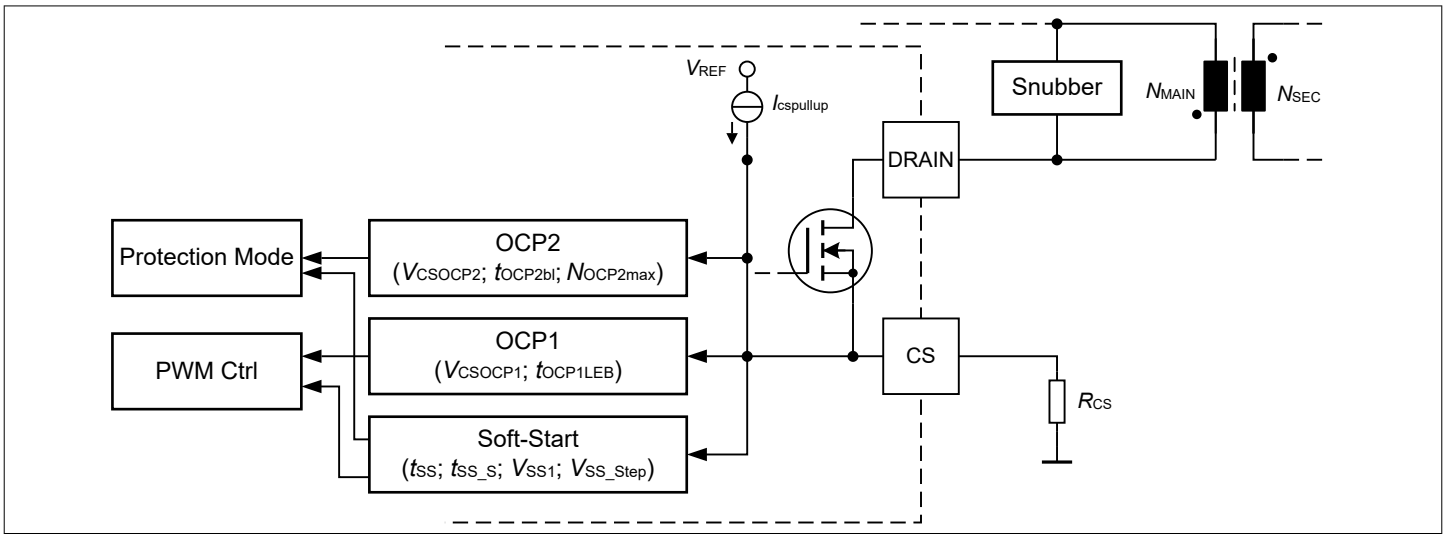


Figure 5 Primary current sensing at CS pin

3.3.4 Primary ZCDP sensing

The ZCDP pin enables the detection of zero-crossing during soft-start and also provides reflected output protection sensing via the auxiliary transformer winding (see Figure 6).

In the system, the voltage from the auxiliary winding is applied to the ZCDP pin through an RC network (R_{ZCDPH}, R_{ZCDPL} and C_{ZCDP}), which provides a time delay to the voltage from the auxiliary winding. Internally, this pin is connected to a zero-crossing detector, an output over/undervoltage detector and a ringing suppression time controller. The external diode D_{AUX} is added to block the negative voltage from the auxiliary winding.

During off-time of the primary power switch, the voltage at the ZCDP pin is monitored for output overvoltage and output undervoltage detection. The latter is only enabled after the soft-start. If the voltage is higher than the

threshold V_{ZCDP_OVP} for $N_{ZCDPovp}$ consecutive switching pulses, the controller enters primary output overvoltage protection. If the voltage is lower than the threshold V_{ZCDP_UVP} for $N_{ZCDPuvp}$ consecutive switching pulses, the controller enters primary output undervoltage protection.

Ringing suppression time

After the primary switch is turned off, the voltage at V_{DRAIN} oscillates, which also appears on $V_{ZCDP.}$ To avoid mis-triggering by such oscillations to turn on the primary switch, a ringing suppression timer is implemented.

If the voltage V_{ZCDP} is lower than the V_{ZCDPRS} threshold, a longer preset time t_{ZCDPrs_SS} is applied. However, if the voltage V_{ZCDP} is higher than the V_{ZCDPRS} threshold, a shorter time t_{ZCDPrs} is set.

ZCDP pin short to ground

In the event of ZCDP pin is shorted before startup, if the voltage at the ZCDP pin is less than the ZCDP short to GNDP threshold V_{ZCDP_short} during configuration loading, the primary ZCDP short to GND protection is triggered and auto-restart mode is entered. To avoid an unknown state at the ZCDP pin, a high impedance path is provided via an integrated R_{ZCDP}. In the event of a floating ZCDP pin, the pin is discharged to GNDP via R_{ZCDP}. After a soft-start, it triggers the primary output undervoltage protection.

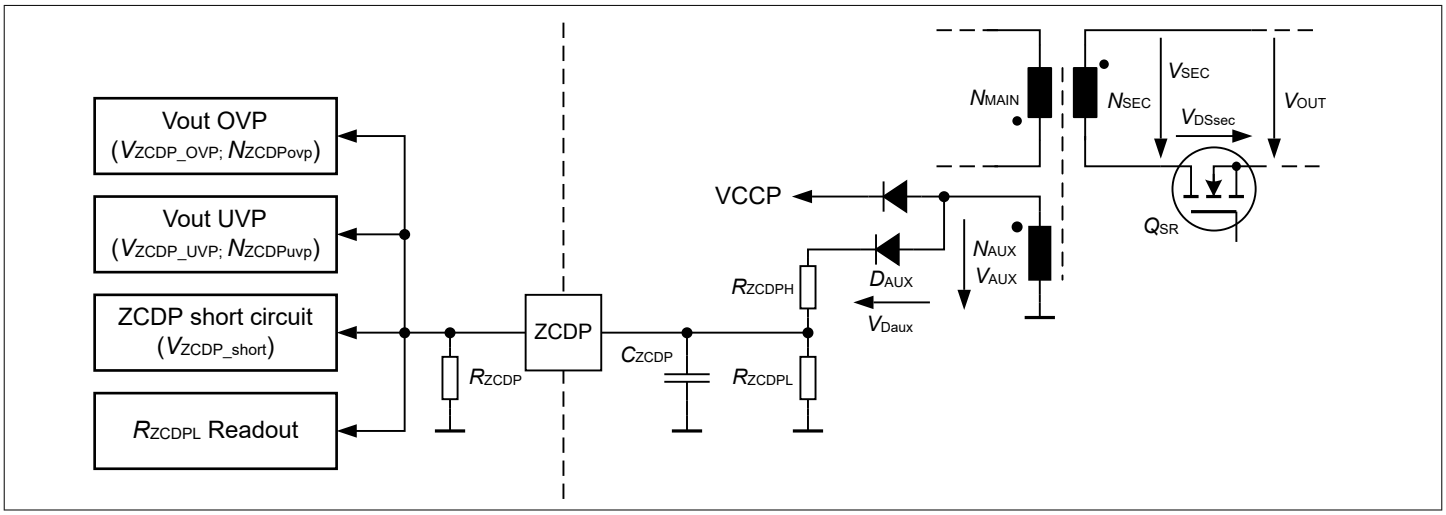


Figure 6 Primary ZCDP pin sensing

3.3.5 Primary soft-start control

As shown in Figure 7, the controller starts to operate with a soft-start by only increasing step by step the peak current limit. The soft-start implemented in the controller is a digital time-based function. The preset soft-start time is t_{SS} with four intermediate steps. If not limited by other functions, the peak voltage on the CS pin increases step by step by V_{SS_Step} from V_{SS1} to V_{CSOCP1} finally. During the first t_{ss_s} of soft-start, the ringing suppression time is set to t_{ZCDPrs_SS} to avoid a premature turn-off of the switching cycle due to oscillation noise.

During the first step of a soft-start, a maximum off-time is implemented. If the gate drive remains off for the period of t_{OffMax}, the gate drive is turned on again.

In addition, there is a maximum on-time t_{OnMax} limitation implemented in the controller. The limitation of maximum on-time and maximum off-time limits audible noise during startup and power down.

If control is not handed over successfully, the primary controller enters auto-restart mode if the secondary side fails to take over control within a timeout t_{pto} after soft-start has ended.

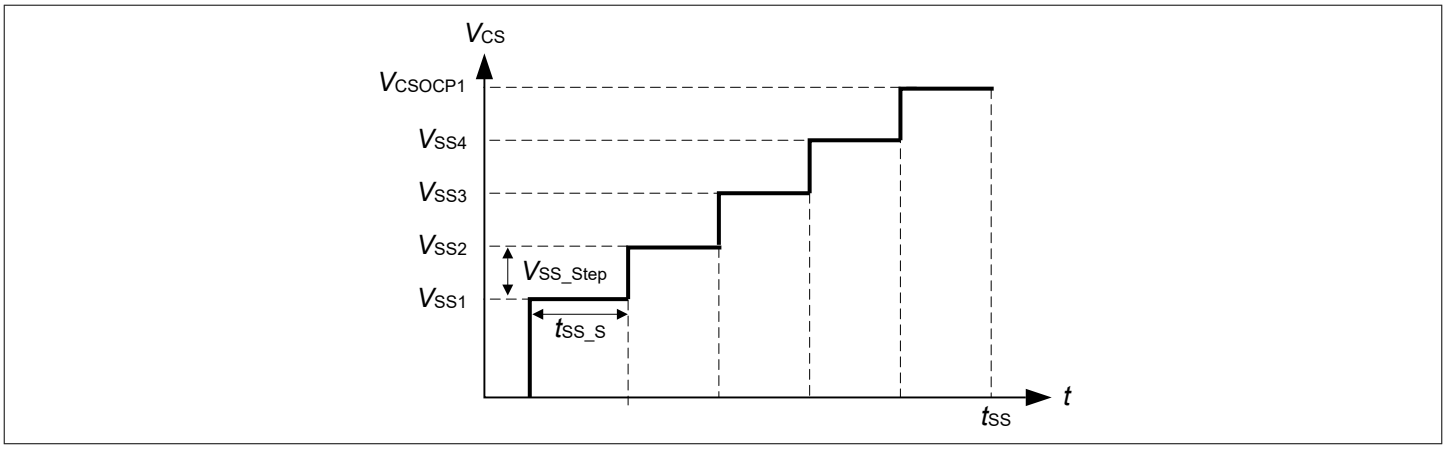


Figure 7 Maximum current sense voltage during soft-start

3.3.6 Normal operation

The following chapters describe the normal operation when secondary side has taken over the PWM control. This control is based on sensing the reflected voltage from primary side via the ZCDS pin. The control ensures that the timing of the SR power switch and the primary side power switch is synchronized under all conditions. A current injection function via the SR power switch enables ZVS operation on primary side. The control loop contains the integrated error amplifier and voltage reference together with the external configurable RC-network.

3.3.6.1 Secondary take-over of control

Once the output voltage exceeds the threshold V_{VCCSon}, the secondary side controller starts monitoring the voltage at the FB pin. As soon as the voltage at the FB pin exceeds a level of $V_{FBstart}$, the secondary side controller takes over control from the primary side controller. This is done in two steps:

- The secondary side controller signals to the primary side to stop switching.
- After a timeout of t_{ho}, the secondary side starts the closed loop operation.

3.3.6.2 Secondary ZCDS sensing

The controller senses the ZCDS pin for SR operation as well as for valley and peak detection.

During the primary side turn-on phase, the controller clamps the ZCDS pin to the voltage at the VCCS pin. As a consequence, the flowing current represents only the reflected input voltage and is determined by the external resistor in this sensing path. This information is used for a feedforward compensation of the input voltage variation by adjusting the on-time for fast line transient response during the turn-on phase.

3.3.6.3 Synchronous rectifier

The controller integrates a synchronous rectifier (SR) controller, which senses the voltage across the secondary side external switch at drain via the ZCDS pin. The sensed signal is compared with two threshold voltages to turn on at V_{NSN} and turn off at $V_{ZCDS\_SROFFslow}$ the external switch to achieve optimum efficiency.

In hysteretic mode, the SR operation is disabled.

3.3.6.4 Self-adapting current injection for zero voltage switching

An additional SR turn-on pulse before turning on the primary side power switch is introduced, to inject current into the transformer for achieving ZVS condition at the primary switch. This occurs when the reflected input voltage on the secondary side is higher than I_{ZCDS_mid} at the ZCDS pin. The controller activates the SR gate driver close to the target valley on the secondary side to insert a ZVS pulse. After the ZVS pulse, the transformer voltage swings to the opposite side.

The controller turns on the primary switch close to the lowest point of the primary drain voltage.

3.3.6.5 Closed loop operation

The controller senses the output voltage via the FB pin and compares it to an internal reference voltage V_{FBref}. An integrated operational transconductance amplifier (OTA) amplifies the error signal for external compensation at the EA pin.

In closed loop operation, the controller creates a primary gate pulse with a duration based on the EA voltage. The pulse generated uses a feedforward-path from the reflected input voltage, which is sensed at the ZCDS pin, to compensate for the effect of a varying input voltage on the pulse width.

3.3.7 Multi-mode operation

The controller optimizes efficiency by multiple operation modes. During normal operation, continuous switching is taking place according to the QR control law. The QR switching is limited by frequency limits for specific operating conditions (for example very high and very low loads). At light-load skip operation is introduced first before the hysteretic mode is entered.

3.3.7.1 QR operation with frequency limits

During normal QR operation, the controller works with a digital signal processing circuit composing a target valley counter, a valley counter and a comparator, and an analog circuit composing a PWM generation unit. The three digital parts are key to implement a digital frequency reduction with decreasing load. The switch-on and -off time points are each determined by the digital circuit and the analog circuit, respectively. The input information of the zero-crossing signal and the target valley are needed to determine the switch-on while the error amplifier signal V_{EA} is necessary for the switch-off determination.

Target valley determination

The target valley number determines when to initiate a new switching cycle. This value depends on the error amplifier voltage V_{EA}, which represents the output power. A high output power results in a high V_{EA}, and a low output power leads to a low V_{EA}. Hence, according to V_{EA}, the target valley is changed to vary the off-time according to the output power.

The voltage V_{EA} is compared with three threshold voltages V_{EA_LHC}, V_{EA_HLC} and V_{EA_R} at each clock period of $t_{valleyupdate}$. The target valley is increased by one, is kept unchanged or is decreased by one, as shown in the table below.

Table 2 Update of target valley

V_{EA}	Target valley action
Always lower than V_{EA_LHC}	Increase by one till $N_{valley\_max\_lowline}$ (low-line) or $N_{valley\_max\_highline}$ (high-line)
Once higher than V_{EA_LHC}, but always lower than V_{EA_HLC}	Stop counting, no value changing
Once higher than V_{EA_HLC}, but always lower than V_{EA_R}	Decrease by one till 1 (low-line) or $N_{valley\_min\_highline}$ (high-line)
Once higher than V_{EA_R}	Set target valley immediately to 1 (low-line) or $N_{valley\_min\_highline}$ (high-line)

The target valley is limited to minimum and maximum values and therefore, the counter varies between 1 to $N_{valley\_max\_lowline}$ (for low-line) or $N_{valley\_min\_highline}$ to $N_{valley\_max\_highline}$ (for high-line). When V_{EA} exceeds V_{EA_R} voltage, the target valley is reset to the lowest possible value (with respect to line voltage) to allow the system to react rapidly to a sudden load increase. The target valley is also reset to the lowest possible value (with respect to line voltage) at the startup time to ensure an efficient maximum load startup. The use of two different thresholds V_{EA_LHC} and V_{EA_HLC} to count upward or downward is to prevent frequency jittering when the error amplifier voltage is close to a threshold.

Minimum target valley determination

To reduce the switching frequency difference between low- and high-line, a minimum valley is implemented. The minimum valley is set to 1 if the ZCDS current during the primary side pulse is below I_{ZCDS_mid} - ΔI_{ZCDS_mid}, which represents low-line. For high-line, the minimum valley is set to $N_{valley\_min\_highline}$ after the ZCDS current during the

primary side pulse is above I_{ZCDS_mid}. ΔI_{ZCDS_mid} determines a hysteresis with certain blanking time t_{ZCDS_mid} to ensure stable AC line selection between low- and high-line.

Valley counting

The controller senses peaks and valleys at the secondary side at the ZCDS pin:

- If ZVS is disabled, the valley counter is increased with every secondary side peak
- If ZVS is enabled, the valley counter is increased with every secondary side valley

Initiation of a new switching cycle

A new switching cycle is initiated when the valley of the valley counter is equal to the target valley number. If the oscillation damps very quickly and the controller cannot detect any further valley, an internal timer generates internal events to increase the valley counter to achieve a frequency foldback.

Avoidance of audible noise

Audible noise is avoided especially at light-load operation and overload condition by limiting the pulse width modulation (PWM) for minimum switching frequency f_{sw_min}. During valley-switching operation, the frequency is foldback by increasing the number of valleys before triggering the next primary turn-on switching cycle.

A new switching cycle is started at the latest when the minimum switching frequency f_{sw_min} is reached, regardless of the valley counter and V_{ZCDS}.

When operating at heavy load, the switching frequency is getting reduced by increasing the demagnetization time. If a maximum period of $t_{CCMperiod}$ is hit, immediately the SR gate driver is turned off and a next primary switch turn-on cycle is triggered.

Both methods ensure that, for both light and heavy loads, the switching frequency stays above the defined level to avoid audible noise.

Maximum switching frequency limitation

The maximum allowable switching frequency is limited internally. If the switching frequency is higher than f_{sw_max}, the primary side PWM gate is only allowed to turn on at the next valley.

Frequency jittering

The frequency jittering function helps to reduce conducted electromagnetic interference (EMI). When the soft-start period is over and the controller enters normal mode operation, the frequency jittering is enabled by superimposing a frequency jitter on the switching period.

The frequency jittering function is determined by the jitter repetition frequency f_{JITper}, considered as fraction of the switching frequency, and the amplitude in delta frequency change Δf_{JITamp} , considered as percentage number in relation to the operating switching frequency.

3.3.7.2 Skip operation

When the error amplifier voltage drops below V_{EA_skip}, both primary side and SR switches remain in off-state. Switching resumes when the error amplifier voltage rises above V_{EA_skip} again.

3.3.7.3 Hysteretic mode operation

At continuous light-load condition, the controller enters hysteretic mode (HM) to minimize the average power consumption. The hysteretic mode entry level is targeted for low range of output power. For determination of entering hysteretic mode, three conditions apply (see Figure 8):

- The error amplifier voltage is lower than the threshold of V_{EA_EHM}
- The target valley is $N_{valley\_max\_lowline}$ for low-line or $N_{valley\_max\_highline}$ for high-line
- The above two conditions remain after a certain blanking time t_{HM}

After having entered the hysteretic mode, the error amplifier voltage rises as V_{out} starts to decrease due to the inactive PWM section. If the level V_{EA_HMon} is exceeded, one comparator observes the error amplifier voltage. In this case, the internal circuit is powered to resume switching. The turn-on of the primary side power MOSFET is triggered by the valley counter with a fixed target valley of $N_{valley\_max\_lowline}$ for low-line and $N_{valley\_max\_highline}$ for high-line. The turn-off is time-based with an input voltage compensation. If the output load is still low, the error amplifier voltage decreases as the switching transfers power from primary to secondary side. When the error amplifier voltage reaches the low threshold V_{EA_HMoff}, the internal circuit is reset again and switching is disabled until the next

time V_{EA} increases beyond the V_{EA_HMon} threshold. In hysteretic mode, the error amplifier voltage is changing like a saw tooth between V_{EA_HMoff} and V_{EA_HMon}.

The error amplifier voltage immediately increases after a high load jump occurs. This is observed by a comparator with threshold V_{EA_LHM}. As the voltage level for primary pulse generation is fixed to $V_{EA\_PWM\_HM}$ during hysteretic mode operation, a certain load is needed that the error amplifier voltage can exceed V_{EA_LHM}. After leaving hysteretic mode, continuous switching with regulation through V_{EA} is re-activated. In addition, the target valley is initialized to $N_{valley\_max\_lowhline}$ (low-line) or $N_{valley\_max\_highline}$ (high-line) immediately after leaving hysteretic mode.

If the load step increases, the error amplifier voltage even above V_{EA_R}, the target valley is immediately changed to 1 (low-line) or $N_{valley\_min\_highline}$ (high-line).

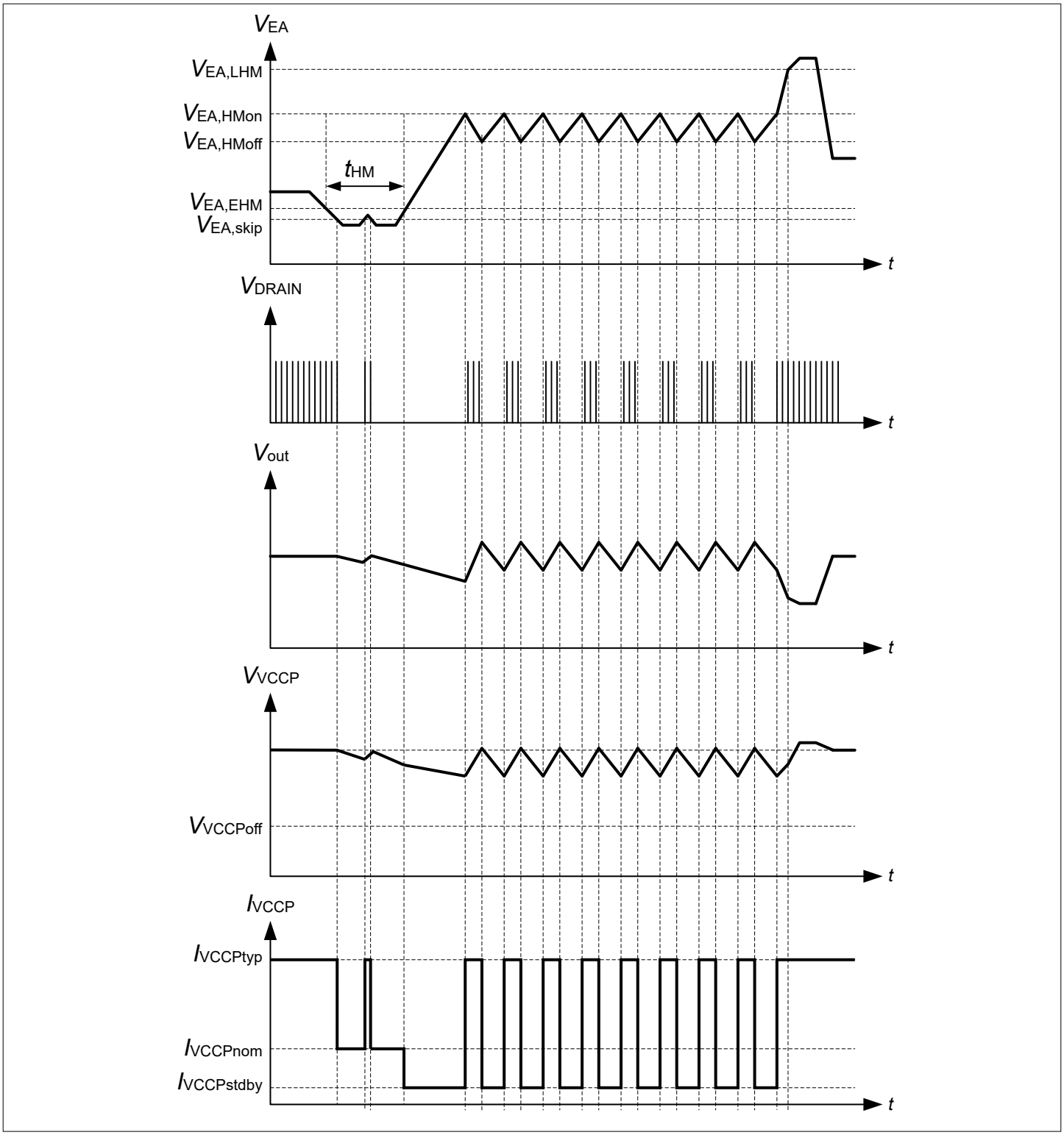


Figure 8 Typical signals for entering, during and exiting hysteretic mode

3.3.8 Enable output signal

This feature supports the ability to control a primary side external peripheral via the secondary side without the need for external isolation components such as an optocoupler (see Figure 9).

The following logic is used:

1. ENP logic = 1 if ENS logic = 1 during active mode
2. ENP logic = 0 if
   - ENS logic = 0 or
   - Controller is off due to low VCCP or protection trigger

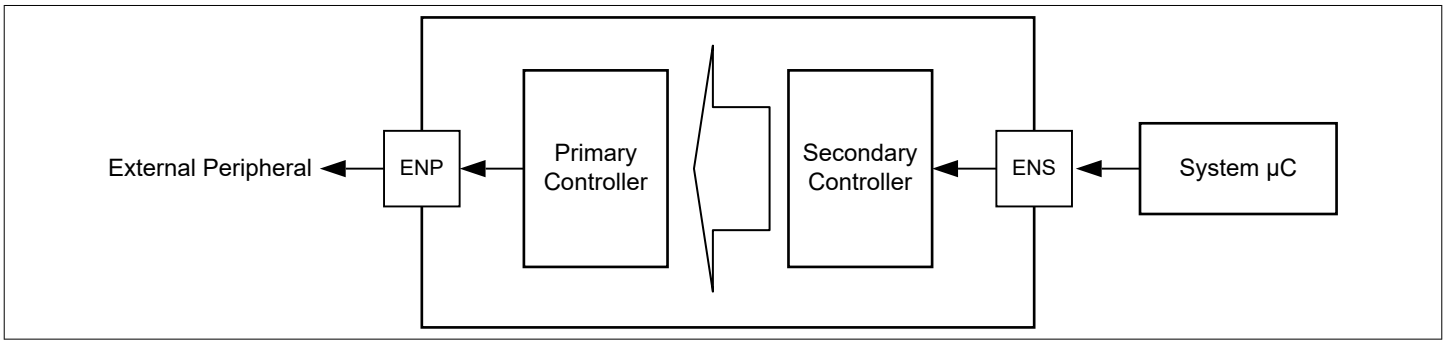


Figure 9 Enable signal via internal isolation path

3.4 Protection features

All protection features are forcing an auto-restart with a new soft-start sequence. After a protection is triggered, three different auto-restart modes apply.

1) Non-switch auto-restart mode

The non-switch auto-restart mode provides no switching activity during the auto-restart phase, when fault detection is again enabled. After fault detection, the controller stops operation and enters a power saving mode. In this inactive mode, the V_{VCCP} is toggling between the $V_{VCCPoff}$ and V_{VCCPon} thresholds controlled by the VCCP charging via the HV startup-cell. Every time when V_{VCCPon} threshold is exceeded, fault detection is triggered. If no further fault condition is detected, the controller starts with a soft-start sequence.

2) Auto-restart mode

The auto-restart mode activates a soft-start sequence when the V_{VCCPon} threshold is exceeded and starts detecting for fault conditions. The soft-start switching is then stopped immediately if the fault conditions is still detected.

3) Eight-skip auto-restart mode

The eight-skip auto-restart mode prolongs the inactive switching phase of the auto-restart mode by V_{VCCP} toggling eight times between the $V_{VCCPoff}$ and V_{VCCPon} thresholds before initiating a soft-start and detecting for fault conditions.

The protection features and assigned auto-restart modes are summarized in the following table.

Table 3 Protection features

Protection features	Startup phase	Continuous switching	Hysteretic mode		Protection mode
	(Open-loop operation)	(Closed-loop operation)	Switching	Non-switching	
Primary VCCP overvoltage and undervoltage protection	√	√	√	√[1)]	Auto-restart

(table continues...)

Table 3 (continued) Protection features

Primary VCCP short to GNDP protection	√	√	√	n.a	No status
Primary maximum peak current limitation (OCP1max)	√	√	√	n.a	HW reset state
Primary 2nd level overcurrent (OCP2) protection	√	√	√	n.a	Eight-skip auto-restart
Primary overtemperature protection	√	√	√	n.a	Non-switch auto-restart
Primary brownin and brownout protection	√	√	√	n.a	Non-switch auto-restart
Primary line overvoltage protection	√	√	√	n.a	Non-switch auto-restart
Primary output overvoltage protection	√	√	√	n.a	Eight-skip auto-restart
Primary output undervoltage protection	√	n.a	n.a	n.a	Eight-skip auto-restart
Primary ZCDP short to GNDP protection	√	n.a	n.a	n.a	Auto-restart
Primary closed-loop timeout protection	√	n.a	n.a	n.a	Eight-skip auto-restart
Secondary VCCS overvoltage	n.a	√	√	n.a	Auto-restart
Secondary VCCS undervoltage	n.a	√	√	n.a	Auto-restart
Secondary VCCS UVLO detection	√	√	√	√	Secondary side off/ powered down
Secondary overload / open-loop (EA pin overvoltage)	n.a	√	n.a	n.a	Auto-restart

1) Only VCCP undervoltage protection.

3.4.1 Primary side protection features

3.4.1.1 Primary VCCP overvoltage and undervoltage protection

During operation, if V_{VCCP} is either below $V_{VCCPoff}$ for $t_{VCCPoff}$ or above V_{VCCP_OVP} for $t_{VCCP\_OVP\_B}$, the primary side power MOSFET is kept off. After the VCCP voltage falls below the threshold $V_{VCCPoff}$, a new startup sequence is activated.

3.4.1.2 Primary VCCP short to GND protection

To limit the power dissipation of the startup circuit at V_{VCCP} short to GNDP condition, the V_{VCCP} charging current is limited to a lower level of $I_{VCCPCharge1}$. With such a low current, the power loss of the controller is limited.

3.4.1.3 Primary maximum peak current limitation (OCP1max)

A current limit comparator provides a cycle by cycle OCP1 maximum peak current limitation on primary side. The source current of the internal switch is measured via the external shunt resistor R_{CS} connected at the CS pin. If the voltage V_{CS} exceeds an internal dynamic voltage limit $V_{CSOCP1}(t)$, the comparator immediately turns off the primary side switch. The dynamic voltage threshold $V_{CSOCP1}(t)$ provides a propagation delay compensation by avoiding a higher limited maximum peak current at high-line condition.

3.4.1.4 Primary maximum power limitation

The minimum target valley increases for high-line condition to $N_{valley\_min\_highline}$, to reduce the delta between limiting the maximum power at low-line and high-line conditions.

3.4.1.5 Primary 2nd level overcurrent (OCP2) protection

A further comparator V_{CSOCP2} is implemented at the CS pin to detect an extremely high primary switch current, which can occur if transformer windings are shorted or if the secondary side is shorted. To avoid an accidental trigger, a spike blanking time t_{OCP2bl} is implemented.

A counter counts the number of occurrences of the short winding condition. If there is $N_{OCP2max}$ consecutive occurrence, the short winding condition is asserted, and the system enters the OCP2 protection mode.

3.4.1.6 Primary CS floating protection

If the CS pin is floating, the internal CS pull up current source $I_{CSpullup}$ charges up the CS pin and trigger the OCP2 protection.

3.4.1.7 Primary overtemperature protection

If the junction temperature of primary side controller exceeds T_{JPOTP}, the controller enters overtemperature protection (OTP) auto-restart mode. The controller can only recover from OTP if the controller's junction temperature drops below the overtemperature hysteresis trip point determined by T_{JPOTP_hys} lower than the overtemperature trigger point.

3.4.1.8 Primary brownin and brownout protection

When the controller is activated, the brownin monitoring is enabled at the HV pin. In addition, the primary side controller is checked for T_{JPOTP} condition. When the T_J temperature is below T_{JPOTP}, the HV startup-cell turns on comparing the current I_{HV} at the HV pin with the current threshold I_{HV_BI}. If one of two conditions is not met, the internal primary side power switch is not activated, and the primary side controller activates another round of auto-restart. This process continues until both conditions are met.

When the controller enters active mode, the V_{IN} voltage is sensed periodically with a sampling period $t_{DCHVsmper}$. The depletion cell is then activated for a fixed sampling time $t_{DCHVsmt}$.

If I_{HV} is less than the HV brownout current threshold I_{HV_BO} during sampling time, a brownout event is considered to be occurred. If the event occurs consecutively for N_{HVBO} times, the protection triggers auto-restart mode.

3.4.1.9 Primary line overvoltage protection

The AC line overvoltage protection (LOVP) is detected by the sensing bus capacitor voltage through the VINP pin via the voltage divider resistors, R_{VINH} and R_{VINL}. When the V_{VINP} voltage is higher than the line overvoltage threshold V_{VINP_LOVP}, the controller enters protection mode until V_{VINP} is lower than V_{VINP_LOVP}. This protection can be disabled by connecting the VINP pin to GNDP.

3.4.1.10 Primary output overvoltage protection

If the secondary side controller does not take over control, the primary side controller stops switching at an overvoltage of the reflected output voltage at V_{ZCDP_OVP} and triggers an auto-restart mode.

This protection is disabled once the secondary side controller has taken over control successfully.

3.4.1.11 Primary output undervoltage protection

The primary output undervoltage protection is enabled after the soft-start time and stops the primary side controller switching for an undervoltage of the reflected output voltage exceeding V_{ZCDP_UVP}. After $N_{ZCDPuvp}$ consecutive switching cycles with detecting undervoltage conditions, an auto-restart is triggered.

This protection is disabled once the secondary side controller has taken over control successfully.

3.4.1.12 Primary ZCDP short to GNDP protection

When the primary side controller is powered, the ZCDP pin is sensed for any short. During the system configuration phase, if ZCDP is less than the ZCDP short to GNDP threshold V_{ZCDP_short}, auto-restart mode is triggered. This protection is disabled after the primary side controller configuration loading is completed.

3.4.1.13 Primary close-loop timeout protection

After the primary side controller starts its open-loop operation, it starts the close-loop timeout t_{pto} counter. If no handshaking is detected from the secondary side controller at the end of the timeout, the primary side controller triggers eight-skip auto-restart mode.

3.4.2 Secondary side protection functions

3.4.2.1 Secondary VCCS undervoltage and overvoltage protection

When V_{VCCS} is below V_{VCCS_UVP} for $t_{VCCS\_UVP\_B}$ or exceeding V_{VCCS_OVP} for $t_{VCCS\_OVP\_B}$, an eight-skip auto-restart is initiated.

3.4.2.2 Secondary open-loop protection

If there is an open control loop or an output overload, the error amplifier voltage is pulled up. When V_{EA} exceeds V_{EA_OLP} after a blanking time of $t_{EA\_OLP\_B}$, the controller enters eight-skip auto-restart mode.

3.5 Hardware configuration by external resistor setting

The controller provides hardware (HW) configuration of the primary and secondary side via the readout of external resistors. After initial start, when the voltage at the VCCP pin and VCCS pin are exceeding the UVLO on-thresholds, the readout is performed on the primary side at the ZCDP pin and on the secondary side at the CONF0 and CONF1 pin.

3.5.1 Primary side configuration

Table 4 Primary side configuration options

Option	[$R_{ZCDL(min)}$; $R_{ZCDL(max)}$]	VINP brownin threshold	VINP brownout threshold
1	[1.00 kΩ ; 1.05 kΩ]	$V_{VINP\_BI\_OPT0}$	$V_{VINP\_BO\_OPT0}$
2	[1.87 kΩ ; 2.70 kΩ]	$V_{VINP\_BI\_OPT1}$	$V_{VINP\_BO\_OPT1}$
3	[4.30 kΩ ; 5.00 kΩ]	$V_{VINP\_BI\_OPT2}$	$V_{VINP\_BO\_OPT2}$
4	[9.20 kΩ ; 9.50 kΩ]	$V_{VINP\_BI\_OPT3}$	$V_{VINP\_BO\_OPT3}$

On primary side, the thresholds for brownin protection and brownout protection are configured by the resistor R_{ZCDPL} at the ZCDP pin. Four configurable options are supported for the paired brownin (BI) and brownout (BO) threshold.

BI and BO are observed by turning on the integrated HV startup-cell at the HV pin. The external HV startup resistor at the HV pin is then connected to the internal shunt resistor $R_{HVshunt}$ and building a resistor divider (see Figure 3).

The different thresholds for BI and BO on system level are set by adjusting $R_{HVshunt}$.

The following table shows the options that can be set by R_{ZCDL} connected between the ZCDP pin and ground.

Table 5 Primary side configuration options

Option	[$R_{ZCDL(min)}$; $R_{ZCDL(max)}$]	Brownin current threshold	Brownout current threshold	Internal $R_{HVshunt}$ for HV sensing
1	[1.00 kΩ ; 1.05 kΩ]	2.00 mA	1.40 mA	0.50 kΩ
2	[1.87 kΩ ; 2.70 kΩ]	1.00 mA	0.70 mA	1.00 kΩ
3	[4.30 kΩ ; 5.00 kΩ]	0.67 mA	0.47 mA	1.50 kΩ
4	[9.20 kΩ ; 9.50 kΩ]	0.50 mA	0.35 mA	2.00 kΩ

3.5.2 Secondary side configuration

The secondary side controller is configured using two resistors at the CONF0 and CONF1 pins.

***Note**: If the CONFx pin is short circuit or left open, auto-restart protection mode is entered. A connected capacitor should be < 100 pF.*

Hardware configuration for CONF0 pin

The CONF0 pin provides the configuration of six options depending on the connected resistor R_{SET0} for the transformer turns ratio N_{MAIN} / N_{SEC} between the main primary side input winding and the main secondary side output winding. This information is used for measuring the reflected input voltage via the ZCDS pin.

Hardware configuration for CONF1 pin

The CONF1 pin provides the configuration of six options depending on the connected resistor R_{SET1} for different parameter settings.

The following table shows the supported options for the resistor R_{SETx} at the CONFx pin:

Table 6 Options for R_{SET0} and R_{SET1}

Option	R_{SETx}	Turns ratio N_{MAIN} / N_{SEC} (R_{SET0})	Parameter set (R_{SET1})
1	3.9 kΩ	5	RSET1_1
2	6.8 kΩ	6	RSET1_2
3	12.0 kΩ	7	RSET1_3
4	18.0 kΩ	8	RSET1_4
5	27.0 kΩ	9	RSET1_5
6	39.0 kΩ	10	RSET1_6

Following parameter settings can be configured:

Table 7 RSET1_x parameter settings

Parameter	Symbol	RSET1_1	RSET1_2	RSET1_3	RSET1_4	RSET1_5	RSET1_6
Minimum valley for high-line	$N_{valley\_min\_highline}$	3	3	3	3	3	3
Minimum valley for low-line	$N_{valley\_min\_lowline}$	1	1	1	1	1	1
Maximum valley for high-line	$N_{valley\_max\_highline}$	10	10	10	10	10	10

(table continues...)

Table 7 (continued) RSET1_x parameter settings

Parameter	Symbol	RSET1_1	RSET1_2	RSET1_3	RSET1_4	RSET1_5	RSET1_6
Maximum valley for low-line	$N_{valley\_max\_lowline}$	8	8	8	8	8	8
EA threshold to enter hysteretic mode	V_{EA_EHM}	0.586 V	0.586 V	0.605 V	0.605 V	0.624 V	0.624 V
EA voltage for wakeup in hysteretic mode	V_{EA_HMOn}	1.20 V	1.20 V	1.20 V	1.25 V	1.20 V	1.25 V
EA voltage for off-phase in hysteretic mode	V_{EA_HMOff}	0.9 V	0.9 V	0.9 V	0.8 V	0.9 V	0.8 V
EA voltage during hysteretic mode	$V_{EA\_PWM\_HM}$	0.8 V	0.9 V	0.9 V	0.8 V	0.9 V	0.8 V

4 Characteristics

All signals are measured with respect to the GNDP or GNDS pin, respectively. The voltage levels are valid if other ratings are not violated.

4.1 Absolute maximum ratings

Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.

Table 8 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain voltage (ICE18xx)	V_{DRAIN}	–	–	800	V	T_J = 25 °C
Voltage at HV pin	V_{HV}	-0.5	–	950	V	Permanently applied as DC value
Current at HV pin	I_{HV}	–	–	10	mA	Internally limited by HV startup-cell
Voltage at VCCP pin	V_{VCCP}	-0.3	–	32	V	–
Voltage at VINP pin	V_{VINP}	-0.3	–	5.5	V	Permanently applied as DC value
Voltage at ZCDP pin	V_{ZCDP}	-0.3	–	5	V	Permanently applied as DC value
Voltage at ENP pin	V_{ENP}	-0.3	–	V_{VCCP} + 0.3	V	Permanently applied as DC value
Voltage at CS pin	V_{CS}	-0.3	–	3.6	V	Permanently applied as DC value
Current at CS pin	$-I_{CSclp}$	–	–	1.3	mA	Permanently applied as DC value. V_{CS} = -0.45 V
Voltage at VCCS pin	V_{VCCS}	-0.3	–	27	V	Permanently applied as DC value
Voltage at ZCDS pin	V_{ZCDS}	-0.3	–	17	V	Permanently applied as DC value
Current at ZCDS pin	I_{ZCDS}	–	–	8	mA	–
Voltage at GDSR pin	V_{GDSR}	-0.3	–	V_{VCCS} +0.3	V	Permanently applied as DC value
Voltage at FB pin	V_{FB}	-0.3	–	5	V	Permanently applied as DC value
Voltage at EA pin	V_{EA}	-0.3	–	5	V	Permanently applied as DC value
Voltage at ENS pin	V_{ENS}	-0.3	–	3.6	V	Permanently applied as DC value
Voltage at CONF0 pin	V_{CONF0}	-0.3	–	3.6	V	Permanently applied as DC value
Voltage at CONF1 pin	V_{CONF1}	-0.3	–	3.6	V	Permanently applied as DC value
Maximum DC current at any pins except for DRAIN and CS pin	–	-10	–	10	mA	–
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_{STORE}	-55	–	150	°C	–

(table continues...)

Table 8 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Soldering temperature	T_{Sold}	–	–	260	°C	Pb-free reflow soldering according to IPC/JEDEC J-STD-020
ESD HBM capability	V_{HBM}	–	–	2	kV	Human body model according to ANSI/ESDA/JEDEC JS-001-2012
ESD CDM capability	V_{CDM}	–	–	500	V	Charged device model according to JESD22-C101F
Latch-up capability	I_{LU}	–	–	100	mA	According to JESD78D, 125 °C (Class II) temperature

4.2 Package characteristics

Table 9 Package characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance from junction to ambient	R_{thJA1}	–	84.7	–	K/W	Setup according to the JEDEC standard JESD51 and using minimum drain pin copper area in a 2 oz copper single sided PCB. T_A = 50 °C, T_J = 125 °C for power switch
Thermal resistance from junction to ambient	R_{thJA2}	–	66.9	–	K/W	Setup according to the JEDEC standard JESD51 and soldering to 232 mm² (0.36 sq) drain pin copper area in a 2 oz copper single sided PCB. T_A = 50 °C, T_J = 125 °C for power switch
Creepage distance between HV to GNDP-related pins	CRP_{HV_GNDP}	1.57	–	–	mm	–
Creepage distance between DRAIN to GNDP-related pins	CRP_{DRAIN_GNDP}	3.52	–	–	mm	–
Creepage distance between isolated primary to secondary related pins	CRP_{PSiso}	8.19	–	–	mm	Pin 10 and pin 27 not connected

4.3 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Table 10 Operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction temperature	T_J	-40	–	125	°C	–
Supply voltage at VCCP pin	V_{VCCP}	$V_{VCCPoff(max)}$	–	$V_{VCCP\_OVP(min)}$	V	–
Supply Voltage at VCCS pin	V_{VCCS}	$V_{VCCS\_UVP(max)}$	–	$V_{VCCS\_OVP(min)}$	V	–
Voltage at HV pin	V_{HV}	-0.3	–	855	V	–
Voltage at CS pin	V_{CS}	-0.3	–	V_{CSOCP2}(max)	V	V_{CSOCP1} = 0.8 V, negative voltage lower needs to respect the negative maximum clamping current $-I_{CSclp}$
Clamp current of CS pin	$-I_{CSclp}$	–	–	2.5	mA	Permanently applied as DC value
Voltage at ENP pin	V_{ENP}	-0.3	–	13	V	–
Voltage at ZCDS pin	V_{ZCDS}	-0.3	–	$V_{VCCS\_OVP(min)}$ + 0.7 V	V	–
Voltage at GDSR pin	V_{GDSR}	-0.3	$V_{GDSRclmp}$	11	V	–
Voltage at all the pins except for DRAIN, HV, VCCP, VCCS, CS, ENP, ENS, ZCDS, and GDSR pin	–	-0.3	–	3.3	V	–
External capacitance at ZCDP pin	C_{ZCDPL}	–	–	100	pF	–
External bottom resistor tolerance at ZCDP pin	ΔR_{ZCDPL}	-5	–	+5	%	–
Current into ZCDS pin	I_{ZCDS}	0.8	–	6.0	mA	Clamp current during primary side pulse while $V_{ZCDS} > V_{VCCS}$
External capacitance at CONFx pin	C_{CONFx}	–	–	100	pF	–
External resistor tolerance at CONFx pin	ΔR_{SETx}	-1	–	+1	%	–
Flyback resonant period	t_{DCM}	600	–	5000	ns	–

4.4 Electrical characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -40 °C to 125 °C. Typical values represent the median values related to T_J = 25 °C. All primary side voltages refer to GNDP, and the assumed supply voltage is V_{VCCP} = 14 V if not otherwise specified. All secondary side voltages refer to GNDS, and the assumed supply voltage is V_{VCCS} = 12 V if not otherwise specified.

4.4.1 Power supply primary (VCCP pin)

Table 11 Electrical characteristics of power supply (VCCP pin)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCCP turn-on threshold	V_{VCCPon}	19	20	21	V	dV_{VCCP} / dt = 0.2 V/ms
VCCP turn-off threshold	$V_{VCCPoff}$	8.55	9.00	9.45	V	dV_{VCCP} / dt = -0.2 V/ms
VCCP turn-off blanking time	$t_{VCCPoff}$	30	50	70	µs	1), 1 V overdrive
VCCP off-state quiescent current	$I_{VCCPoff}$	–	165	340	µA	V_{VCCP} < $V_{VCCPon(min)}$ - 0.3 V
VCCP supply current without gate drive	$I_{VCCPnom}$	–	1.4	–	mA	1), IC self supply excluding gate drive currents
VCCP supply current in typical operation (ICE183xx)	$I_{VCCPtyp}$	–	2.50	2.90	mA	1), f_{swGDx} = 100 kHz
VCCP supply current in typical operation (ICE184xx)	$I_{VCCPtyp}$	–	3.20	3.60	mA	1), f_{swGDx} = 100 kHz
VCCP supply current in typical operation (ICE186xx)	$I_{VCCPtyp}$	–	3.54	3.94	mA	1), f_{swGDx} = 100 kHz
VCCP supply current in stand-by mode with ENP high	$I_{VCCPstdbyENP}$	–	380	450	µA	1), V_{ENS} > V_{ENS_H}, Sleep phase, T_J < 50 °C
VCCP supply current in stand-by mode	$I_{VCCPstdby}$	–	210	250	µA	1), Sleep phase, T_J < 50 °C
VCCP supply current in auto-restart mode (ARM)	$I_{VCCParm}$	–	200	500	µA	Sleep phase, T_J < 50 °C
VCCP overvoltage threshold	V_{VCCP_OVP}	28.9	30.4	31.9	V	–
VCCP overvoltage blanking time	$t_{VCCP\_OVP\_B}$	36	60	84	µs	1)

1) Not subject to production test - verified by design/characterization

4.4.2 High voltage (HV pin)

Table 12 Electrical characteristics of HV pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current at HV pin	I_{HVLK}	–	–	10	µA	V_{HV} = 800 V, HV startup-cell disabled
DC high voltage sampling time	$t_{DCHVsmt}$	18	20	22	µs	1)
DC high voltage sampling period	$t_{DCHVsmper}$	900	1000	1100	µs	1), During active phase
VCCP threshold for safe VCCP charging without short-circuit	$V_{VCCPstart}$	–	–	1.8	V	–
Initial VCCP charge current	$I_{VCCPCharge1}$	0.33	0.78	1.65	mA	$V_{VCCP} < V_{VCCPstart}$
Clamped VCCP charge current	$I_{VCCPCharge2}$	2.3	5.0	9.0	mA	$V_{VCCP} > V_{VCCPstart}$, R_{HV} = 50 kΩ, V_{IN} = 600 V
HV Brownin current threshold	I_{HV_BI}	1.88	2.00	2.12	mA	2), Option 1
HV Brownout current threshold	I_{HV_BO}	1.31	1.40	1.49	mA	2), Option 1
HV Brownin current threshold	I_{HV_BI}	0.94	1.00	1.06	mA	2), Option 2
HV Brownout current threshold	I_{HV_BO}	0.65	0.70	0.75	mA	2), Option 2
HV Brownin current threshold	I_{HV_BI}	0.63	0.67	0.71	mA	2), Option 3
HV Brownout current threshold	I_{HV_BO}	0.44	0.47	0.50	mA	2), Option 3
HV Brownin current threshold	I_{HV_BI}	0.47	0.50	0.54	mA	2), Option 4
HV Brownout current threshold	I_{HV_BO}	0.33	0.35	0.38	mA	2), Option 4
HV Brownout detection blanking	N_{HVBO}	–	4	–	cycle	3), Consecutive sampling cycles to trigger brownout protection

1) Not subject to production test - verified by design/characterization
2) Configurable, see Table 5
3) Not subject to production test - verified by design/characterization

4.4.3 Current sensing primary (CS pin)

Table 13 Electrical characteristics of CS pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CS pin pull-up current	$I_{CSpullup}$	0.8	1.0	1.2	uA	–
OCP1 maximum peak current limitation	V_{CSOCP1}	0.70	0.76	0.82	V	–
Leading edge blanking time	$t_{OCP1LEB}$	154	220	286	ns	–
OCP2 turn-off threshold	V_{CSOCP2}	1.04	1.10	1.16	V	–
OCP2 blanking time	t_{OCP2bl}	28	40	52	ns	1)
Max allowable OCP2 consecutive switching cycles	$N_{OCP2max}$	–	3	–	–	1)
Abnormal CS voltage sample period	$t_{CS\_STG\_SAM}$	4.5	5	5.5	µs	1)
Number of pulses used for CS pin short protection	N_{CS_STG}	–	3	–	–	1)
Soft-start time	t_{ss}	10.8	12.0	13.2	ms	1)
Soft-start time step	t_{ss_s}	2.7	3.0	3.3	ms	1)
Internal regulation voltage at CS pin for the first step	V_{SS1}	0.27	0.30	0.33	V	–
Internal regulation voltage step at CS pin for soft-start	V_{SS_Step}	0.135	0.150	0.165	V	–
Maximum on-time during open-loop operation	t_{OnMax}	31.5	35.0	38.5	µs	1)
Maximum off-time during open-loop operation	t_{OffMax}	38.2	42.5	46.8	µs	1)
Close-loop timeout time	t_{pto}	36	40	44	ms	1)

1) Not subject to production test - verified by design/characterization

4.4.4 Primary zero-crossing detection and output voltage measurement (ZCDP pin)

Table 14 Electrical characteristics of ZCDP pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ZCDP zero-crossing threshold	$V_{ZCDPthr}$	70	100	130	mV	Falling edge
ZCDP long ringing suppression threshold	V_{ZCDPRS}	0.27	0.30	0.33	V	–
ZCDP ringing suppression time	t_{ZCDPrs}	1700	2000	2300	ns	1), $V_{ZCDP} > V_{ZCDPRS}$
ZCDP long ringing suppression time	t_{ZCDPrs_SS}	22.5	25.0	27.5	µs	1), $V_{ZCDP} < V_{ZCDPRS}$
ZCDP output overvoltage threshold	V_{ZCDP_OVP}	2.05	2.20	2.35	V	–
ZCDP output overvoltage blanking	$N_{ZCDPovp}$	–	3	–	cycle	1)
ZCDP output undervoltage threshold	V_{ZCDP_UVP}	0.45	0.50	0.55	V	–
ZCDP output undervoltage blanking	$N_{ZCDPuvp}$	–	3	–	cycle	1)
ZCDP short to GNDP threshold	V_{ZCDP_short}	70	100	130	mV	

1) Not subject to production test - verified by design/characterization

4.4.5 Bus voltage sensing primary (VINP pin)

Table 15 Electrical characteristics of VINP pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Line overvoltage threshold	V_{VINP_LOVP}	2.68	2.80	2.92	V	–
Line overvoltage blanking	t_{VINP_LOVP}	225	250	275	µs	1)
VINP Input leakage current	I_{VINPLK}	-200	–	200	nA	–

1) Not subject to production test - verified by design/characterization

4.4.6 Primary output enable control (ENP pin)

Table 16 Electrical characteristics of ENP pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ENP output voltage level (High)	V_{ENP_H}	7.9	10.0	13.0	V	To on/off bus voltage sensing resistor ladder **1.** V_{VCCP} > 9 V **2.** R_{load} = 2.5 kΩ
ENP source current	I_{ENPsrc}	3.7	6.0	8.4	mA	V_{ENP} = 5 V, V_{VCCP} = 7.6 V to 32 V

4.4.7 Power switch

Table 17 Electrical characteristics of power switch

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DRAIN to CS breakdown voltage (ICE18xx)	$V_{(BR)DSS}$	800	–	–	V	T_J = 25 °C
DRAIN leakage current	I_{DSS}	–	–	1	µA	V_{DRAIN} = 800 V, T_J = 25 °C
DRAIN leakage current	I_{DSS}	–	10	–	µA	[1], V_{DRAIN} = 800 V, T_J = 150 °C
DRAIN to CS on-resistance (ICE183xx)	$R_{DS(on)}$	–	1.92	2.18	Ω	T_J = 25 °C, I_D = 1.4 A
DRAIN to CS on-resistance (ICE183xx)	$R_{DS(on)}$	–	3.67	–	Ω	T_J = 125 °C, I_D = 1.4 A
DRAIN to CS on-resistance (ICE184xx)	$R_{DS(on)}$	–	0.70	0.84	Ω	T_J = 25 °C, I_D = 1.6 A
DRAIN to CS on-resistance (ICE184xx)	$R_{DS(on)}$	–	1.48	–	Ω	T_J = 125 °C, I_D = 1.6 A
DRAIN to CS on-resistance (ICE186xx)	$R_{DS(on)}$	–	0.39	0.48	Ω	T_J = 25 °C, I_D = 2.0 A
DRAIN to CS on-resistance (ICE186xx)	$R_{DS(on)}$	–	0.80	–	Ω	T_J = 125 °C, I_D = 2.0 A
Effective output capacitance, energy related (ICE183xx)	C_{oer}	–	7	–	pF	[1], V_{DRAIN} = 0 V to 500 V
Effective output capacitance, energy related (ICE184xx)	C_{oer}	–	12	–	pF	[1], V_{DRAIN} = 0 V to 500 V
Effective output capacitance, energy related (ICE186xx)	C_{oer}	–	20	–	pF	[1], V_{DRAIN} = 0 V to 500 V

(table continues...)

Table 17 (continued) Electrical characteristics of power switch

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum on-time in closed loop	t_{ONmin_CL}	302	336	370	ns	1)
Maximum on-time in closed loop	t_{OnMax_CL}	31.5	35.0	38.5	µs	1)

1) Not subject to production test - verified by design/characterization

4.4.8 Power supply secondary (VCCS pin)

Table 18 Electrical characteristics of power supply (VCCS pin)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCCS turn-on threshold	V_{VCCSon}	–	–	5.7	V	–
VCCS HW reset hysteresis below turn-on threshold	$V_{VCCSres}$	350	–	1050	mV	–
VCCS undervoltage protection threshold	V_{VCCS_UVP}	6.6	7.0	7.4	V	1)
VCCS undervoltage protection blanking time	$t_{VCCS\_UVP\_B}$	40	–	–	µs	1)
VCCS overvoltage protection threshold	V_{VCCS_OVP}	14.6	15.5	–	V	1)
VCCS overvoltage blanking time	$t_{VCCS\_OVP\_B}$	40	–	–	µs	1), 1 V overdrive
VCCS supply current in normal mode without gate drive	$I_{VCCSnom}$	–	4.3	–	mA	1)
VCCS supply current during stand-by mode	$I_{VCCSstdby}$	–	360	600	µA	During non-switching time, T_J < 50 °C
VCCS supply current during protection mode	$I_{VCCSoff}$	–	4.3	–	mA	Protection mode entered

1) Not subject to production test - verified by design/characterization

4.4.9 Feedback (FB pin)

Table 19 Electrical characteristics of FB pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FB leakage current	I_{FBLK}	–	–	500	nA	1.0 V < V_{FB} < 2.4 V
FB reference voltage	V_{FBref}	1.176	1.200	1.224	V	–
FB startup voltage	$V_{FBstart}$	–	1.14	–	V	1)

1) Not subject to production test - verified by design/characterization

4.4.10 Multi-mode and error amplifier output (EA pin)

Table 20 Electrical characteristics of multi-mode and EA pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
EA voltage maximum clamp	$V_{EA\_maxclamp}$	2.2	2.3	2.4	V	–
EA voltage for maximum pulse width	V_{PWM_hclamp}	2.0	2.1	2.2	V	–
EA voltage offset for PWM generation	V_{PWM_lclamp}	0.35	0.40	0.45	V	–
Update interval for target valley	$t_{valleyupdate}$	45.6	48.0	50.4	ms	1)
Minimum valley for high-line	$N_{valley\_min\_highline}$	–	2)	–	–	1), Applies if $I_{ZCDS\_clamp} > I_{ZCDS\_mid}$
Minimum valley for low-line	$N_{valley\_min\_lowline}$	–	2)	–	–	1), Applies if $I_{ZCDS\_clamp} < I_{ZCDS\_mid} - \Delta I_{ZCDS\_mid}$
Maximum valley for high-line	$N_{valley\_max\_highline}$	–	2)	–	–	1), Applies if $I_{ZCDS\_clamp} > I_{ZCDS\_mid}$
Maximum valley for low-line	$N_{valley\_max\_lowline}$	–	2)	–	–	1), Applies if $I_{ZCDS\_clamp} < I_{ZCDS\_mid} - \Delta I_{ZCDS\_mid}$
EA voltage for immediate minimum target valley	V_{EA_R}	1.72	1.80	1.88	V	–
EA voltage for valley decrease	V_{EA_HLC}	1.15	1.20	1.25	V	1)
EA voltage for valley increase	V_{EA_LHC}	0.95	1.00	1.05	V	1)
DCM minimum switching frequency	f_{sw_min}	24	25	26	kHz	1)

(table continues...)

Table 20 (continued) Electrical characteristics of multi-mode and EA pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CCM fixed maximum period	$t_{CCMperiod}$	36	40	44	µs	1)
EA voltage skip threshold	V_{EA_skip}	0.45	0.50	0.55	V	
EA hysteretic mode entry threshold tolerance	ΔV_{EA_EHM}	-7	–	7	%	1) , 2)
Hysteretic operation entry blanking time	t_{HM}	18	20	22	ms	1)
EA voltage hysteretic mode on threshold tolerance	ΔV_{EA_HMon}	-9	–	9	%	2)
EA voltage hysteretic mode off threshold tolerance	ΔV_{EA_HMoff}	-7	–	7	%	2)
EA voltage for pulses during hysteretic mode tolerance	$\Delta V_{EA\_PWM\_HM}$	-7	–	7	%	2)
Target valley during hysteretic mode	N_{valley_HM}	–	N_{valley_max}	–	–	1) , Hysteretic mode operation
Wakeup time in hysteretic operation	t_{wkHM}	–	–	80	µs	1) , From EA voltage crossing V_{EA_HMon} until primary switch turn-on
EA voltage hysteretic mode exit threshold	V_{EA_LHM}	1.53	1.60	1.67	V	–
EA open-loop threshold	V_{EA_OLP}	–	$V_{EA\_maxclamp}$	–	V	–
EA open-loop protection blanking time	$t_{EA\_OLP\_B}$	20	–	–	ms	1)
Maximum switching frequency limitation	f_{sw_max}	–	–	150	kHz	1)

1) Not subject to production test - verified by design/characterization
2) Configurable, see Chapter 3.5.2

4.4.11 Jitter function

Table 21 Electrical characteristics of jitter function

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Jitter repetition frequency	f_{JITper}	3.6	4.0	4.4	kHz	1), Normal mode, f_{sw} = 64 kHz
Jitter frequency amplitude	Δf_{JITamp}	3.6	4.0	4.4	%	1), Normal mode

1) Not subject to production test - verified by design/characterization

4.4.12 Zero-crossing detection secondary (ZCDS pin)

Table 22 Electrical characteristics of ZCDS pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ZCDS clamped voltage level	$V_{ZCDSclmp}$	–	V_{VCCS}	–	V	V_{VCCS} = 12 V
ZCDS line voltage threshold for valley selection and ZVS enabling	I_{ZCDS_mid}	1.79	1.99	2.19	mA	1), N_{MAIN} / N_{SEC} = 8, R_{ZCDS} = 15 kΩ
ZCDS line voltage hysteresis for valley selection and ZVS enabling	ΔI_{ZCDS_mid}	242	269	296	µA	1), N_{MAIN} / N_{SEC} = 8, R_{ZCDS} = 15 kΩ
ZCDS line voltage blanking time for valley selection and ZVS enabling	t_{ZCDS_mid}	14.4	16.0	17.6	ms	1)
ZCDS SR turn-on threshold	V_{NSN}	75	100	125	mV	Falling edge
ZCDS SR turn-on propagation delay	$t_{SRONdel}$	–	100	130	ns	1), From V_{ZCDS} crossing V_{NSN} to GDSR reaching 2 V
ZCDS SR slow turn-off threshold	$V_{ZCDS\_SROFFslow}$	-13	-4	0	mV	Rising slope
ZCDS SR slow turn-off propagation delay	$t_{SROFFslow\_Delay}$	–	300	350	ns	1), From V_{ZCDS} to GDSR reaching 2 V

1) Not subject to production test - verified by design/characterization

4.4.13 SR gate driver (GDSR pin)

Table 23 Electrical characteristics of GDSR pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
GDSR pin clamped gate driver voltage	$V_{GDSRclmp}$	9	10	11	V	V_{VCCS} = 12 V
GDSR pin gate drive voltage at low VCCS	$V_{GDSRlow}$	8.5	–	–	V	V_{VCCS} = 10 V
Rise time (20% to 80%) of SR gate driver output for demagnetization period	$t_{GDSR\_demag\_rise}$	–	11	80	ns	1), C_{GDSR} = 3 nF, V_{VCCS} = 12 V
Fall time (80% to 20%) of SR gate driver output for demagnetization period	$t_{GDSR\_demag\_fall}$	–	25	50	ns	1), C_{GDSR} = 3 nF, V_{VCCS} = 12 V
Rise time (20% to 80%) of SR gate driver output for ZVS pulse current injection	$t_{GDSR\_zvs\_rise}$	–	26	90	ns	1), $I_{ZCDS} > I_{ZCDS\_mid}$, C_{GDSR} = 3 nF, V_{VCCS} = 12 V
Fall time (80% to 20%) of SR gate driver output for ZVS pulse current injection	$t_{GDSR\_zvs\_fall}$	–	33	70	ns	1), $I_{ZCDS} > I_{ZCDS\_mid}$, C_{GDSR} = 3 nF, V_{VCCS} = 12 V
Minimum GDSR on-time	t_{on_GDSR}	567	630	693	ns	1)

1) Not subject to production test - verified by design/characterization

4.4.14 Secondary side enable for primary enable output (ENS Pin)

Table 24 Electrical characteristics of ENS pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ENS voltage low threshold	V_{ENS_L}	–	–	1.0	V	1)
ENS voltage high threshold	V_{ENS_H}	2.0	–	–	V	1)
ENS blanking time for enabling and disabling	t_{ENSbl}	20	–	–	µs	1), Only during continuous switching. Not valid for skip and hysteretic mode operation.

1) Not subject to production test - verified by design/characterization

4.4.15 Secondary side configuration (CONF0 and CONF1 pins)

Table 25 Electrical characteristics of CONF0 and CONF1 pins

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sourcing sense current	I_{CONFx}	42.5	50	57.5	µA	–

4.4.16 Primary overtemperature sensing

Table 26 Electrical characteristics of primary overtemperature sensing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature threshold	T_{JPOTP}	129	140	150	°C	1)
Overtemperature reset hysteresis	T_{JPOTP_hys}	–	40	–	°C	1)
Overtemperature blanking time	t_{JPOTP}	–	48	–	ms	1)

1) Not subject to production test - verified by design/characterization

4.4.17 Common mode transient immunity (CMTI)

Table 27 Electrical characteristics for common mode transient immunity

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Common mode transient immunity	CMTI	50	–	–	V/ns	According to DIN V VDE V0884-17, static and dynamic test

4.4.18 Isolation specifications

Table 28 Isolation specifications

Parameter	Symbol	Value	Unit	Note or condition
External creepage	CRP	> 8	mm	Shortest distance over package surface from any input pin to any output pin according to IEC 60664-17
External clearance	CLR	> 8	mm	Shortest distance in air from any input pin to any output pin according to IEC 60664-1
Comparative tracking index	CTI	> 400	V	According to DIN EN 60112 (VDE 0303-11)
Material group	–	II	–	According to IEC 60112
Pollution degree	–	II	–	According to IEC 60664-1

(table continues...)

Table 28 (continued) Isolation specifications

Parameter	Symbol	Value	Unit	Note or condition
Overvoltage category (for reinforced isolation)	–	I - IV	–	Rated mains voltage ≤ 150 V_{RMS}
	–	I - IV	–	Rated mains voltage ≤ 300 V_{RMS}
	–	I - III	–	Rated mains voltage ≤ 600 V_{RMS}
Climatic category	–	40/125/21	–	
Input-to-output isolation according to UL1577				
Input-to-output isolation voltage	V_{ISO}	5700	V_{RMS}	$V_{TEST} = V_{ISO}$ for t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$ for t = 1 s (100 % productive tests)
Input-to-output isolation according to IEC 60747-17 (VDE 0884-17)				
Maximum impulse voltage	V_{IMP}	8000	V_{pk}	According to IEC 60664-1
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{pk}	$V_{TEST} = V_{IOTM}$ for t_{ini} = 60 s (type test and sample test) $V_{TEST} = 1.2 \times V_{IOTM}$ for t_{ini} = 1 s (routine test)
Maximum rated repetitive peak isolation voltage (ICE18xxx)	V_{IORM}	800	V_{pk}	According to time dependent dielectric breakdown (TDDB) test for reinforced isolation
Apparent charge	q_{PD}	< 5	pC	Method (b1) $V_{ini,b1} = 1.2 \times V_{IOTM}$ (routine test) $V_{ini,b1} = V_{IOTM}$ for t_{ini} = 1 s (type test preconditioning) $V_{PD(m)} = 1.875 \times V_{IORM}$ for t_m = 1 s
				Method (a) (type test, subgroup 1 final measurements) $V_{ini,a} = V_{IOTM}$ for t_{ini} = 60 s $V_{PD(m)} = 1.6 \times V_{IORM}$ for t_m = 10 s
				Method (a) (type test, subgroup 2, 3 final measurements) $V_{ini,a} = V_{IOTM}$ for t_{ini} = 60 s $V_{PD(m)} = 1.2 \times V_{IORM}$ for t_m = 10 s
Maximum surge isolation voltage	V_{IOSM}	11000	V_{pk}	V_{TEST} = 11 kV_{pk} ≥ 1.3 x V_{IMP} for reinforced isolation according IEC 60747-17
Isolation resistance	R_{IO}	> 10^{12}	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 25 °C
		> 10^{11}	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 125 °C
		> 10^{9}	Ω	V_{IO} = 500 V_{dc} for t = 60 s, $T_S = T_A$ = 150 °C
Isolation capacitance	C_{IO}	< 2	pF	f = 1 MHz

4.4.19 Safety supply power

Table 29 Reinforced isolation safety-limiting values as outlined in IEC 60747-17 (VDE 0884-17)

Parameter	Side	Value	Unit	Note or condition
Primary side power switch safe DC current (ICE183xM)	Power switch chip	0.50	A	Average current of PWM switching cycle, T_J = 140 °C
Primary side power switch safe DC current (ICE184xM)	Power switch chip	0.82	A	Average current of PWM switching cycle, T_J = 140 °C
Primary side power switch safe DC current (ICE186xM)	Power switch chip	1.10	A	Average current of PWM switching cycle, T_J = 140 °C
Safety supply currents	Primary chip	12	mA	$R_{thja(max)}$ = 66,9 K/W, VCCP = 20 V, T_A = 25 °C, T_J = 125 °C (Overtemperature protected)
	Secondary chip	20	mA	$R_{thja(max)}$ = 66,9 K/W, VCCS = 12 V, T_A = 25 °C, T_J = 125 °C
Safety power supply	Primary chip	0.24	W	$R_{thja(max)}$ = 66,9 K/W, T_A = 25 °C, T_J = 125 °C (Overtemperature protected)
	Power switch chip	1.27	W	$R_{thja(max)}$ = 66,9 K/W, T_A = 25 °C, T_J = 140 °C
	Secondary chip	0.24	W	$R_{thja(max)}$ = 66,9 K/W, T_A = 25 °C, T_J = 125 °C

5 Package information

5.1 Outline dimensions and footprint

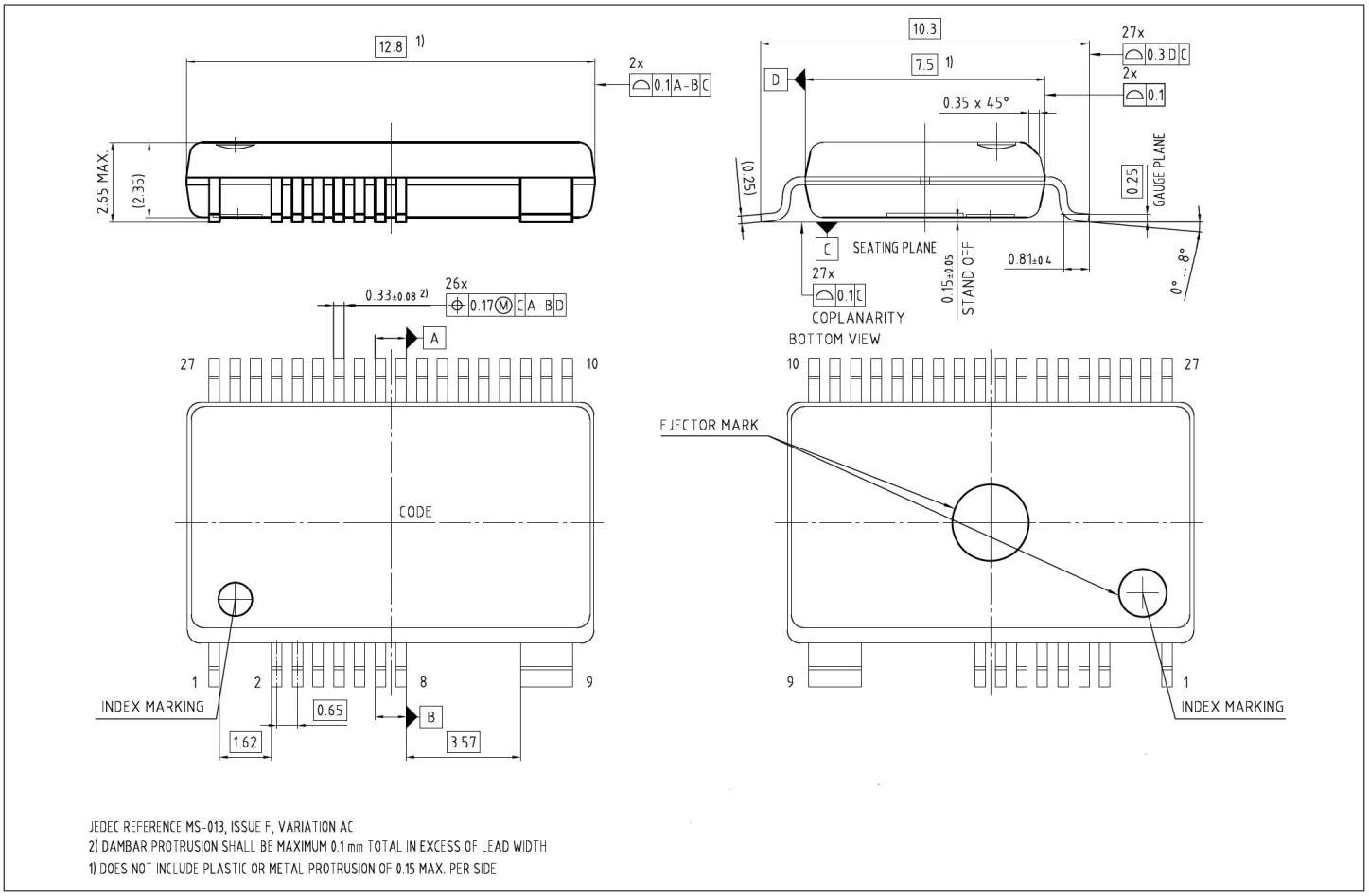


Figure 10 Outline dimensions PG-DSO-27-1

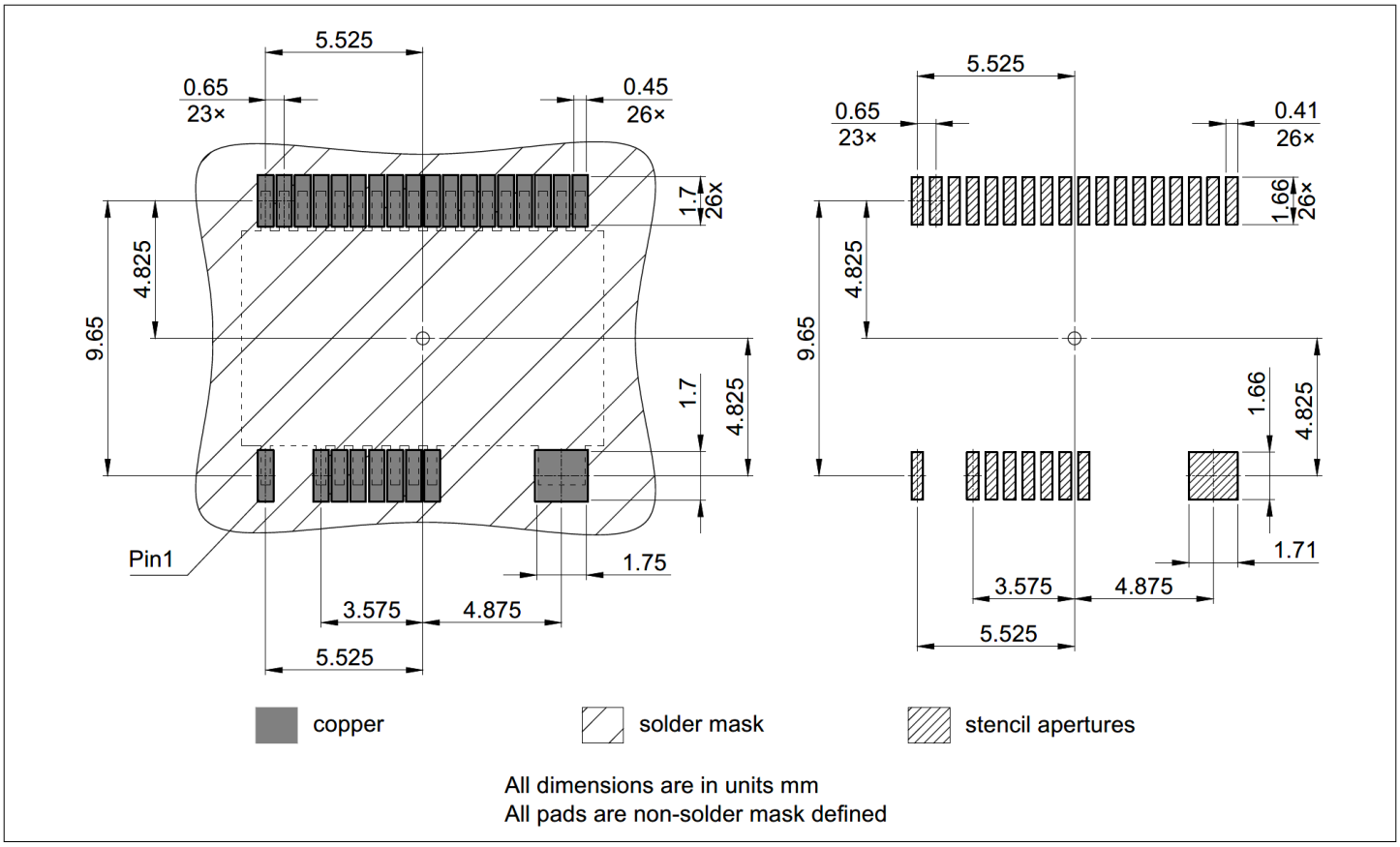


Figure 11 Footprint

5.2 Marking

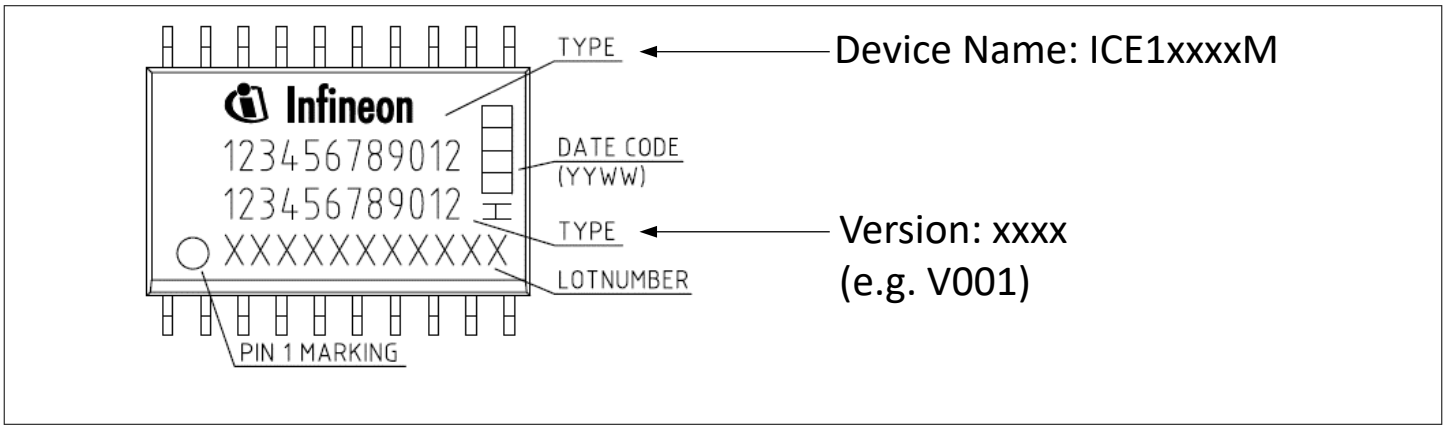


Figure 12

5.3 Green product (RoHS compliant)

Table 30 Green product and RoHS compliant

Package compliance	Description
Green product	For minimum environmental impact and compliance with government regulations, the package of the device fulfills the requirements of a green product. Green products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).
RoHS	The package of the device is RoHS-compliant.

6 Part ordering information

Part number	Ordering code	Package	Power FET	$R_{DS(on)}$(max)[1)]
ICE183EM-V001	SP006172815	PG-DSO-27-1	800 V CoolMOS™ P7	2.18 Ω
ICE184EM-V001	SP006172803	PG-DSO-27-1	800 V CoolMOS™ P7	0.84 Ω
ICE186EM-V001	SP006172807	PG-DSO-27-1	800 V CoolMOS™ P7	0.48 Ω

1) at T_J = 25 °C

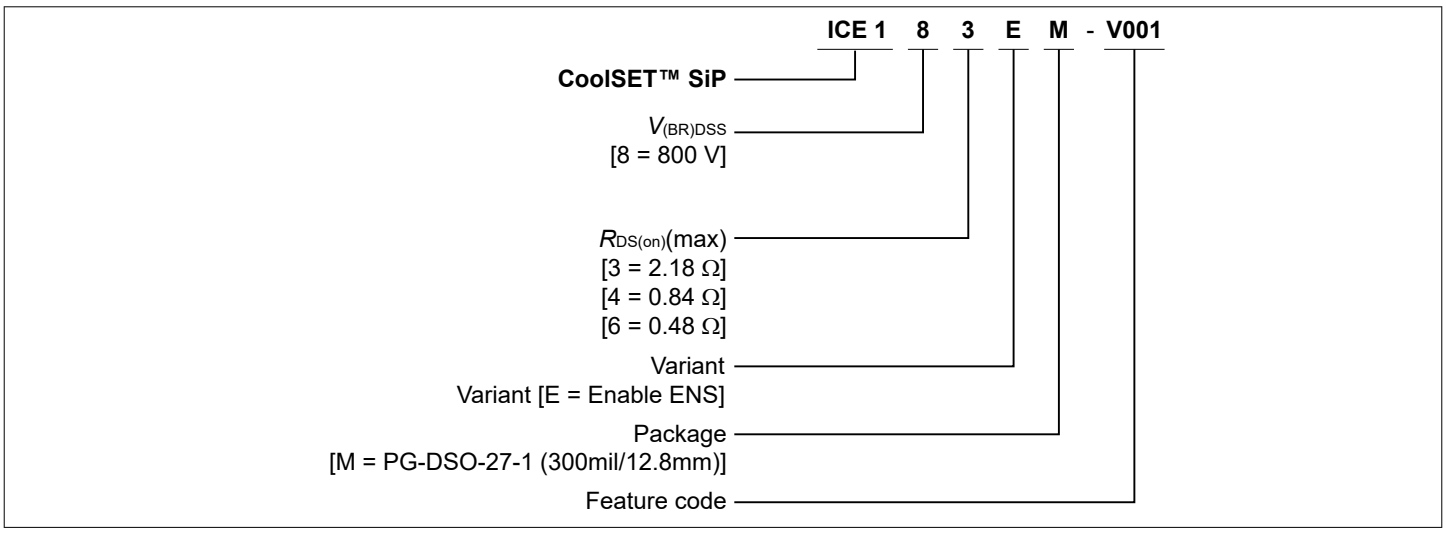


Figure 13 Part ordering information

7 Revision history

Document version	Date of release	Description of changes
Rev 1.0	2025-11-26	Initial release
Rev 1.1	2026-01-13	Updated protection feature table 3 on page 17

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-01-13

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2026 Infineon Technologies AG

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-vcn1740007606066

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.