EZ-USB™ HX2G3 USB 2.0 Hi-Speed Hub

Overview

EZ-USB™ HX2G3 is a USB 2.0 hub controller with a Cortex®-M0+ MCU, 32 KB of SRAM, and 32 KB of ROM. It includes programmable USB 2.0 PHYs and one serial communication block (SCB) that supports I2C or SPI. It can run from firmware (FW) on ROM, or an external I2C EEPROM/ SPI flash, or downloaded from an external I2C master.

EZ-USB™ HX2G3 is available in two packages for commercial or industrial applications:

- 40-QFN
- 36-LGA

Features

- USB 2.0 hub controller
  - Supports Hi-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) data rates
- Multiple port configuration options
  - One upstream port and four downstream ports (1:4)
  - One upstream port and two downstream ports (1:2)
- Integrated Arm® Cortex®-M0+ CPU
  - 32 KB RAM, 32 KB ROM
- Embedded eFuse to support trimming, VID/PID, and PHY configuration
- Optional configurable Full-Speed device function support
  - Optional CDC device class support
  - Firmware download and configuration supported through USB (CDC interface) to the I2C EEPROM/ SPI flash connected externally to EZ-USB™ HX2G3
  - Firmware download and configuration supported through I2C from an external I2C master, saving BOM for external SPI flash or I2C EEPROM for boot
- Individual and ganged port power control
- Support active and deep sleep power modes
- No power sequence needed
- Supports Hub Cascade mode
  - Configurable option to output the reference clock for the cascaded hubs to share the source clock and save crystal cost
- Extensive configuration support with EZ-USB™ HX2G3 configuration utility for
  - Vendor ID (VID)/Product ID (PID), manufacturer and product string descriptors
  - Enabling or disabling the DS ports
  - Setting removable and non-removable devices
  - Ganged or individual power switch enables for downstream ports
  - Polarity selection for power enable outputs and overcurrent inputs
  - USB 2.0 PHY parameters
  - Swap DP/DM signals for flexible PCB routing
- Multiple boot options to load configuration and firmware
  - ROM
  - External EEPROM
  - External I2C master
  - External SPI flash

Features

- Available in two packages[1]
  - 40-QFN, 5×5 mm, 0.4 mm pitch (–40°C to 85°C)
  - 36-LGA, 6×6 mm, 0.5 mm pitch (–40°C to 85°C)

Note
1. For more details on package information, see **Table 13**.

Block diagram

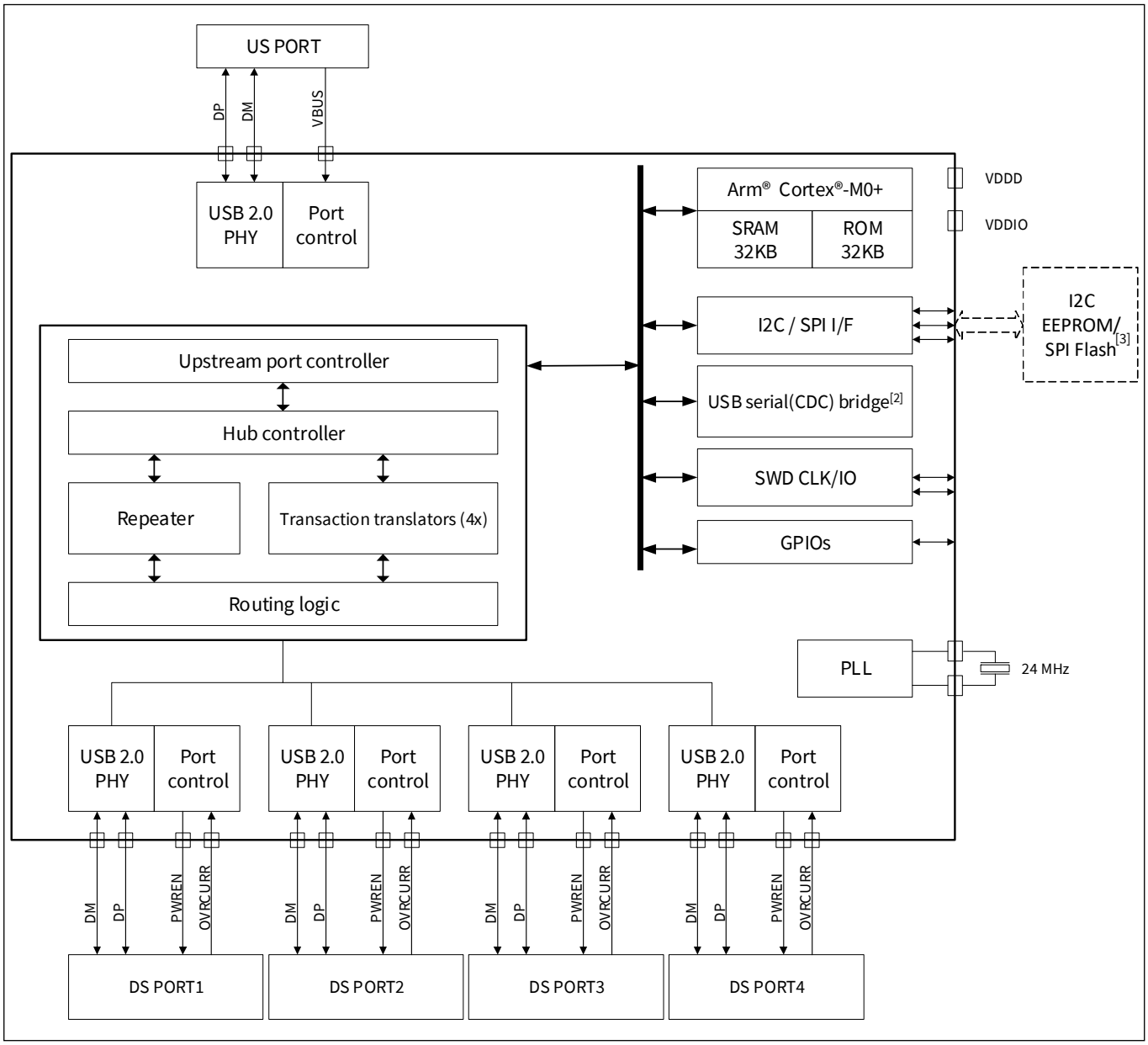


Figure 1 EZ-USB™ HX2G3 block diagram in 1:4 configuration

Notes

2. Enabling the embedded USB-serial (CDC) bridge device will reduce the number of externally available DS ports. The CDC bridge device will always get enumerated on DS Port1.
3. External I2C EEPROM/SPI flash is optional.

Table of contents

1 EZ-USB™ HX2G3 resources

Table 1 EZ-USB™ HX2G3 resources

Resources	Description
Application notes	EZ-USB™ HX2G3 hardware design guidelines
Development kits	KIT_HX2G3_40QFN
Infineon developer community	**Infineon Developer Community** enables connection with fellow EZ-USB™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated Infineon Community
EZ-USB™ HX2G3 Configuration Utility	A windows desktop application that guides users through the process of configuring and programming EZ-USB™ HX2G3 devices

2 Application

2.1 Consumer application

A typical consumer application in which EZ-USB™ HX2G3 is a self-powered hub with one upstream and four downstream (1:4), or one upstream and two downstream (1:2) configuration. EZ-USB™ HX2G3 acts as a generic hub for port extension.

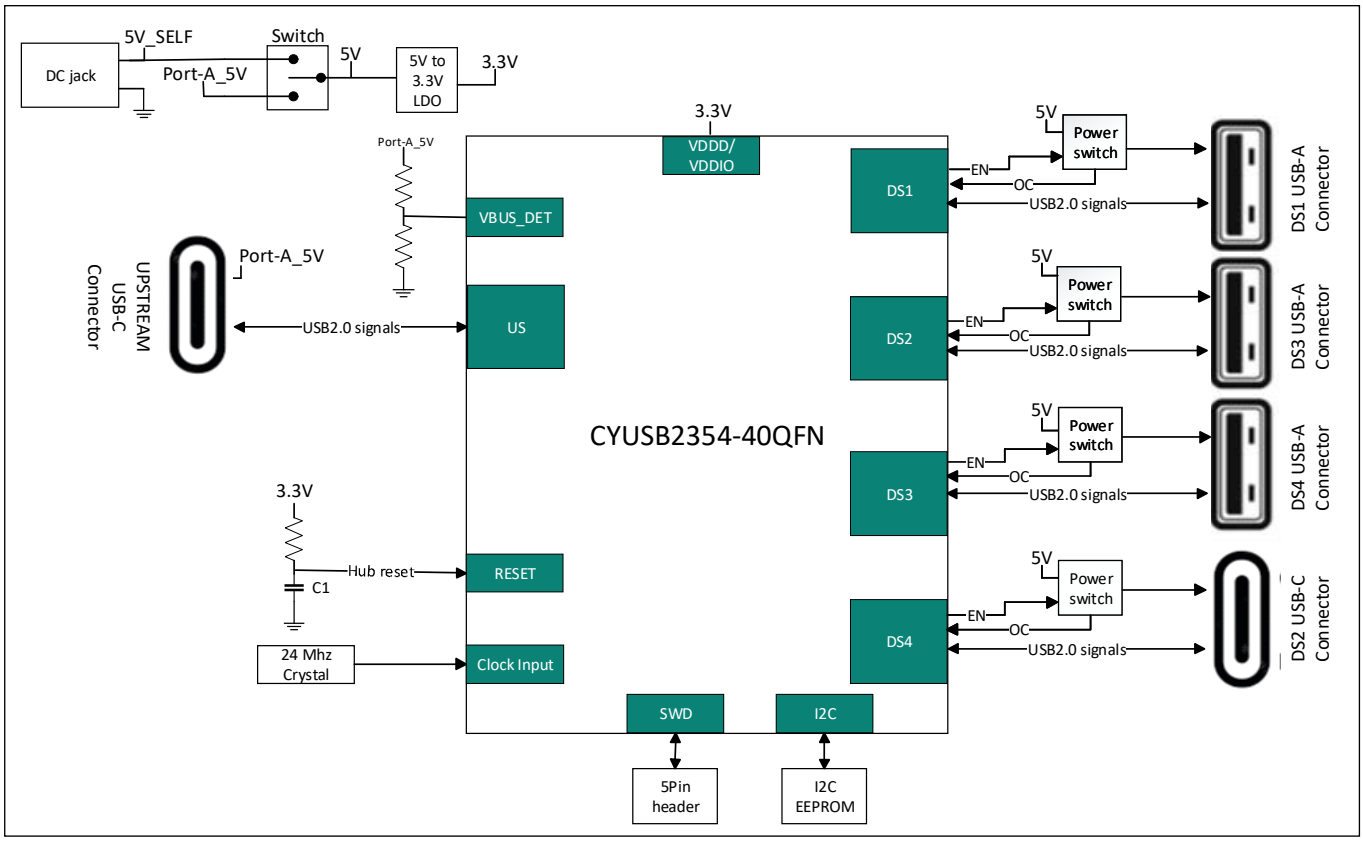


Figure 2 EZ-USB™ HX2G3 as 1:4 consumer hub

Application

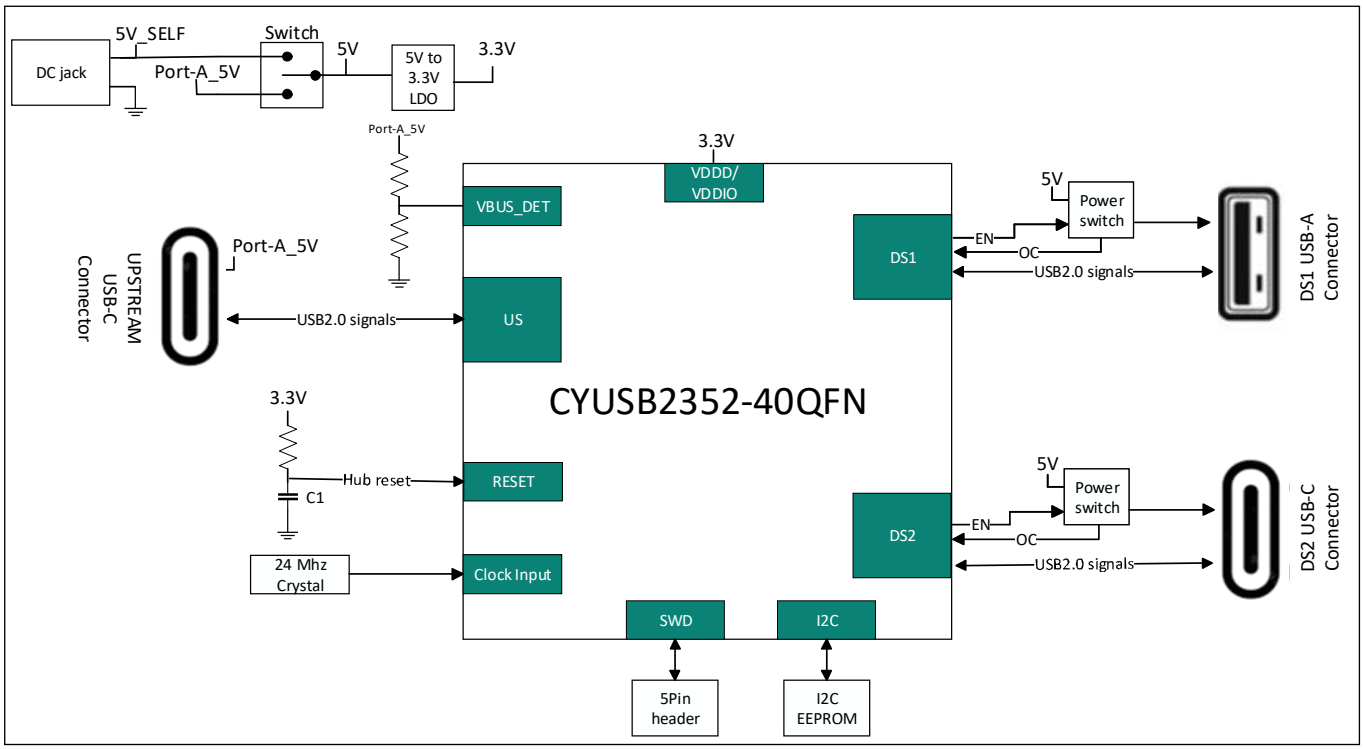


Figure 3 EZ-USB™ HX2G3 as 1:2 consumer hub

Application

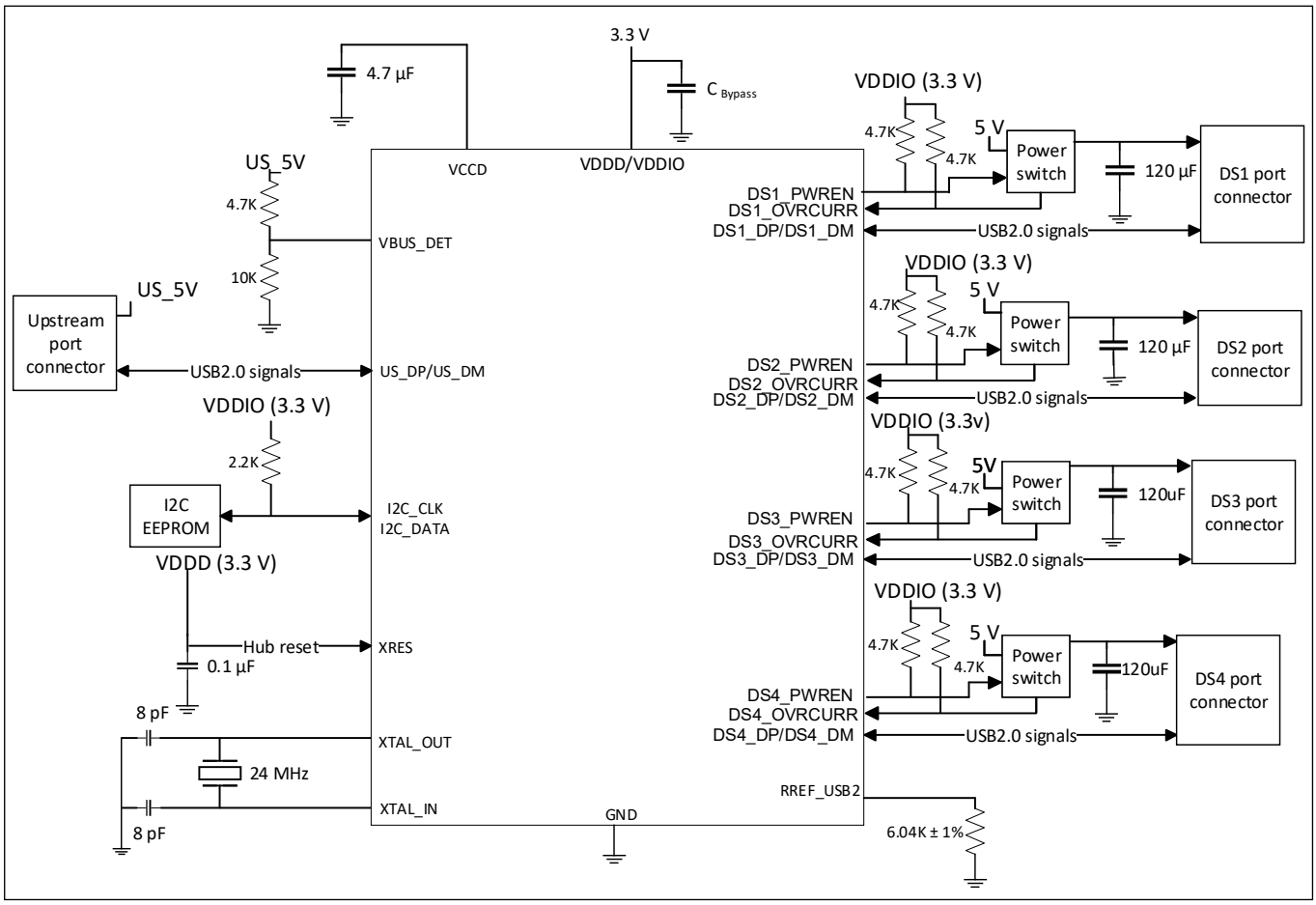


Figure 4 Generic application schematic for EZ-USB™ HX2G3

3 Product features

EZ-USB™ HX2G3 is a USB 2.0 hub controller that supports one upstream port and up to four downstream ports. It includes an optional composite Full-Speed (FS) device. EZ-USB™ HX2G3 includes the firmware in internal ROM to initialize the hub and can operate as a stand-alone hub controller. It can also run with FW downloaded from an external EEPROM, external I2C master, or an external SPI.

The following sections provide an overview of the features and capabilities of the EZ-USB™ HX2G3 device.

3.1 USB 2.0 hub

The USB 2.0 hub operates as defined by the **USB 2.0 specification** and based on the configuration settings in the EEPROM or eFuse settings.

3.1.1 Upstream port

The upstream port includes an integrated 1.5 KΩ pull-up resistor and termination resistors. Only one upstream port is supported in consumer/industrial application. See **Table 2** for possible port configurations.

3.1.2 Downstream port

Downstream ports have integrated 15 KΩ pull-down and termination resistors. The ports are disabled or enabled using configuration options through external I2C EEPROM or eFuse.

Note that enabling FS device in EZ-USB™ HX2G3 will reduce the number of DS ports by one. For example, if FS device is enabled with hub in 1:4 configuration, number of DS ports will be reduced to three. FS device is disabled by default for every consumer product. For more information, see **Table 2**.

Table 2 Downstream ports

EZ-USB™ HX2G3 configuration	Number of DS ports without FS device enabled	Number of DS ports with FS device enabled
1:2	2	1
1:4	4	3

3.2 Power management

EZ-USB™ HX2G3 internally implements control signaling for external power switching. The initial conditions of these signals are in disabled state in order to reduce inrush currents.

EZ-USB™ HX2G3 provides Active, Deep Sleep, and Reset modes to control power consumption at different operational states. The core logic operates at 1.1 V (LP). In conjunction with clock gating at peripheral and bus levels, this permits fine-grained optimization of energy usage over system life. The application ROM code will transition the chip to appropriate power states based on the repeater state.

3.3 CPU

The CPU supports initialization and power mode transitions. It is a single-core subsystem consisting of a 60-MHz Cortex® M0+.

3.4 Clocking

EZ-USB™ HX2G3 supports the following clock options as reference clocks for the USB 2.0 hub subsystem:

- 24-MHz crystal input
- 24-MHz external clock

In case of external clock, connect the output of the oscillator to XTAL IN and keep XTAL OUT floating.
The following are the recommended crystal parts:

- ECS-240-8-36CKM-TR (manufacturer: ECS)
- ABM10 W-24.0000 MHZ-6-B1U-T3 (manufacturer: Abracon)

The following is the recommended oscillator part:

- ECS-2520MV-240-DN-TR (Manufacturer: ECS)

See **Table 3** for crystal/clock specification.

Table 3 External XTAL/clock specification

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
EXT_CRY_RES_FREQ	Crystal resonator frequency	–	24	–	MHz	Resonator reference clock frequency. Fundamental oscillation mode
EXT_CRY_RES_FREQ_TOL	Crystal resonator frequency tolerance	–30	–	30	ppm	Resonator reference clock frequency
EXT_CRY_RES_CLOAD	Crystal resonator load capacitance	–	9.5	–	pF	PCB load
EXT_CRY_RES_CSHUNT	Crystal resonator shunt capacitance	–	0.4	1	pF	No ground connection
EXT_CRY_RESCMOTIONAL	Crystal resonator motional capacitance	–	–	3	pF	No ground connection
EXT_CRY_RES_ESR	Crystal resonator ESR	–	–	60	Ω	Equivalent sales resistance
EXT_CRY_RES_PDRIVE	Drive level for crystal oscillator	–	50	200	µW	Resonator drive level
EXT_CRY_RES_START	Crystal resonator start-up time	–	–	1.6	ms	Maximum start-up time required by resonator to meet the USB 2.0 timing requirements

3.5 Communication interfaces (I2C or SPI)

The communication interface bus is part of a serial communication block (SCB) that is controlled by the bootloader and is one of the optional methods for initializing the hub. It follows the I2C bus specification or SPI interface. This SCB can be configured as any of the below:

1. I2C Master: This is used when the EZ-USB™ HX2G3 is loaded with an external Configuration/FW from an I2C EEPROM or any I2C Slave device
2. I2C Slave: In this case external I2C master can write the Configuration/FW to the SRAM of the EZ-USB™ HX2G3, and EZ-USB™ HX2G3 shall boot with the new Configuration/FW
3. SPI Master: EZ-USB™ HX2G3 boots from the Configuration/FW from the external SPI flash

See the **EZ-USB™ HX2G3 Boot flow to load configuration/firmware** for more details.

3.6 Full-Speed device

The embedded USB serial device controller is internally connected to downstream port (DS1) of the EZ-USB™ HX2G3 hub. This is used for the programming the configuration/FW into the external memory devices connected to the EZ-USB™ HX2G3 hub over I2C or SPI. FS device is disabled by default for every consumer product.

3.7 Boot options

EZ-USB™ HX2G3 includes an integrated ROM that contains firmware such as the Bootloader, Hub controller code, and default configurations, enabling it to operate as a standalone hub. During startup, the CPU executes the ROM code to boot the device, load configurations, and run firmware to control GPIOs and enable downstream power.

In addition to internal boot, EZ-USB™ HX2G3 also supports booting from external devices, with the supported boot configurations are described in **EZ-USB™ HX2G3 Boot flow to load configuration/firmware**.

3.7.1 EZ-USB™ HX2G3 Boot flow to load configuration/firmware

EZ-USB™ HX2G3 provides multiple options to load configuration and firmware that includes accessing EEPROM, external I2C master, SPI flash or default option as ROM. To select source for the configuration and firmware, there are four possibilities:

- **EZ-USB™ HX2G3 SCB configured in I2C master mode**
  - In I2C master mode, the EZ-USB™ HX2G3 bootloader looks for a slave device such as EEPROM. If the device is found, the EZ-USB™ HX2G3 downloads the configuration, firmware, or both from the slave device and initiates the rest of the initialization from the newly downloaded firmware stored in RAM. If the image in the slave device is corrupted, the EZ-USB™ HX2G3 ignores this image and boot from ROM which holds the default firmware and configuration
- **EZ-USB™ HX2G3 SCB configured in I2C slave mode**
  - In I2C slave mode, the EZ-USB™ HX2G3 bootloader waits for an external I2C master (such as PD controller) to download the configuration, firmware, or both into the EZ-USB™ HX2G3 within a given configuration time. If the image is corrupted, the EZ-USB™ HX2G3 ignores this image and boot from ROM
- **EZ-USB™ HX2G3 SCB configured in SPI master mode**
  - In SPI master mode, the EZ-USB™ HX2G3 bootloader looks for a flash device. If the flash device is found, the EZ-USB™ HX2G3 downloads the configuration, firmware, or both from the flash device and initiates the rest of the initialization from the newly downloaded firmware stored in RAM. If the image in the SPI flash device is corrupted, the EZ-USB™ HX2G3 ignores this image and boot from ROM
- **ROM as source for configuration and firmware**
  - If the firmware is not available from any external device, ROM is the last option the EZ-USB™ HX2G3 bootloader looks for available configuration and firmware. The rest of the system is initialized from the firmware that is available in the ROM

Figure 5 shows the overall flow of the boot sequence.

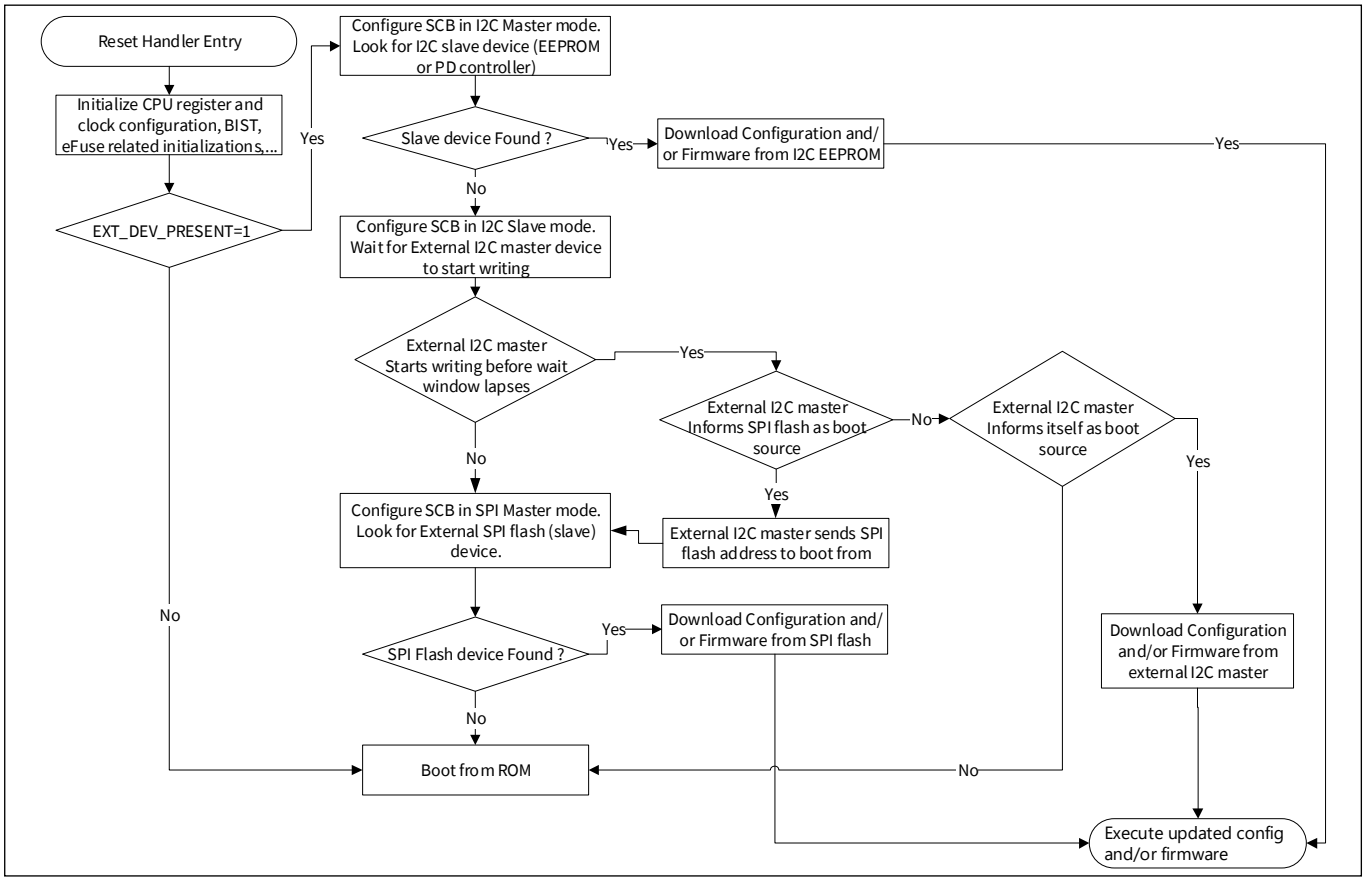


Figure 5 Boot flow[4]

3.8 EZ-USB™ HX2G3 configuration

EZ-USB™ HX2G3 can be configured using one of the following:

- External I2C master
- External I2C slave such as an EEPROM
- External SPI flash

On top of static configuration, EZ-USB™ HX2G3 also offers an I2C slave interface in the application firmware for reading status and some level of dynamic configuration.

3.8.1 Configuration table structure

For more details, refer to the **EZ-USB™ HX2G3 Configuration Utility**.

Note

To modify the PHY CONFIG parameters, contact **Infineon local support.**

Note

4. EXT_DEV_PRESENT - 'External device is present' is set in order to boot in I2C master mode, SPI master mode or I2C Slave mode.

Table 4 Parameter configuration table

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Header	0	7:0	bSignature LSB (“C”)	The first byte of the 2-byte signature initialized with “CY” ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device	0x43	0x43	0x43
	1	7:0	bSignature MSB (“Y”)	The second byte of the 2-byte signature initialized with “CY” ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device	0x59	0x59	0x59
	2	7:0	bImageCTL	Bits 3:0 ==> 0 Bits 5:4 ==> I2C clock frequency (0: 1 MHz, 1: 400 KHz, 2: 100 KHz, 3: 100 KHz) Bits 7:6 ==> SPI clock frequency (0: 10 MHz, 1: 7.5 MHz, 2: 5 MHz, 3: 1 MHz)	0x00	0x00	0x00
	3	7:0	bImageType	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code	0xD4	0xD4	0xD4
	4	7:0	wTableLength LSB	Lower byte of the length of the config table in bytes	–	–	–
	5	7:0	wTableLength MSB	Upper byte of the length of the config table in bytes	–	–	–
	6	7:0	wChecksum LSB	LSB of checksum calculated over bytes 8 to N of the config table	–	–	–
	7	7:0	wChecksum MSB	MSB of checksum calculated over bytes 8 to N of the config table	–	–	–
Hub config	8	7	I2CSlaveEnable	Enables I2C slave interface once application has booted up 0: I2C slave mode disabled 1: I2C slave mode enabled	1	1	1
		6:0	I2CSlaveAddr	I2C slave address (7-bit) to be used when Hub application is running	0	0	0
	9	7:6	Reserved	Reserved	–	–	–
		5	Reserved	Reserved	–	–	–
		4	Reserved	Reserved	–	–	–
		3	singleTTEnable	0: Multi-TT hub 1: Single-TT hub	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Hub config	9	2	compoundDevice	Gives information about presence of FS device 0: FS device not present 1: FS device present	0	0	0
		1:0	FSDevFunc	Select USBFS device function on DS1 port: 0: No function 1: CDC Serial bridge function enabled 2: Invalid 3: Invalid	1	1	1
	10	7:4	REMOVABLE_PORTS [3:0]	Indicates if the port is removable bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable	0xF	0xF	0xF
		3:0	PORT_PRESENT[3:0]	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active	0xF	0x3	0xF
	11	7	GANG_PWR_EN	Whether hub uses ganged power switching 0: Individual power enabled 1: Ganged power enabled	0	0	0
		6	BUS_POWER	Whether the hub is bus powered 0: Self powered 1: Bus powered	0	0	0
		5:2	PWR_EN_POLARITY[3:0]	POWER ENABLE polarity for the DS ports (DS4, DS3, DS2, DS1): 0: Power enable signals are active low 1: Power enable signals are active high	0	0	0
		1	OC_SUPPORT_DISABLE	Whether Overcurrent notifications are disabled for DS ports 0: OC support enabled 1: OC support disabled	0	0	0
		0	INDIVIDUAL_OC	0: Global over-current protection is supported 1: Individual port over-current protection is supported	1	1	1

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Hub config	12	7:4	OC_POLARITY[3:0]	Over Current Polarity for all DS ports (DS4, DS3, DS2, DS1): 0: OC indicators are active low 1: OC indicators are active high	0	0	0
		3	fwAvailable	Firmware is available and should be downloaded from external device: 0: Firmware Not available 1: Firmware available	0	0	0
		2:1	Reserved	Reserved	–	–	–
		0	pwrSwSupport	Power Switch Support: 0:Power switching not supported by HUB 1: Power switching supported by HUB	1	1	1
	13	7:5	UFP_CONFIG	These three bits are used to decide UFP config: 001: 1UFP + 4DFP	1	1	1
		4:3	Reserved	Reserved	–	–	–
		2	Reserved	Reserved	–	–	–
		1	IgnoreStringDescriptors	0: String descriptors will be updated based on values from config table 1: String descriptors as pre-defined by ROM will be used	0	0	0
		0	IgnorePhyConfig	0: PHY config registers will be updated based on values from config table 1: PHY config registers will be programmed based on eFUSE contents	1	1	1
	14	7:0	HUB_VID[7:0]	Custom Vendor ID - LSB	0xB4	0xB4	0xB4
	15	7:0	HUB_VID [15:8]	Custom Vendor ID - MSB	0x04	0x04	0x04
	16	7:0	HUB_PID [7:0]	Custom Product ID (PID) Default: 0x6560 Different PID values for different product numbers	0x10	0x10	0x10
	17	7:0	HUB_PID [15:8]	–	0x65	0x65	0x65
	18	7:0	DID [7:0]	LSB of bcdDevice field in Device Descriptor. Represents Silicon/ROM revision information B7:4 -> Major Revision B3:0 -> Minor Revision	0x0A	0x0A	0x0A
	19	7:0	DID [15:8]	MSB of bcdDevice field in Device Descriptor. Represents application firmware version when present.	0x50	0x50	0x50

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Hub config	20	7:0	MAX_POWER	USB Descriptor specific. bMaxPower -> Configuration Descriptor	0x32	0x32	0x32
	21	7:0	MAX_CURRENT	USB Descriptor specific bMHub-ContrCurrent -> Hub Descriptor	0x64	0x64	0x64
	22	7:0	powerGoodTime	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)	0x32	0x32	0x32
	23	7	PllRefClockSel	0: Use ECO to obtain 24-MHz reference clock for the PLL 1: Use external clock input as reference clock for the PLL	0	0	0
		6:4	SuspPinFunction	Select functionality of SUSPEND pin 0: No function 1: Connect to clk_eco (24-MHz) output for cascaded hubs 2: Indication of upstream suspend (L2) state: Active low 3: Indication of upstream suspend (L2) state: Active high 4: Use as external power present indicator input (active low) 5: Use as external power present indicator input (active high) 6: Reserved 7: Reserved	3	3	3
		3	VbusDetectEnable	Whether Vbus detection function is enabled: 0: Vbus detection is disabled 1: Vbus detection function is enabled on VBUS_DETECT_IO pin	1	1	1
		2	VbusDetectPolarity	Selects polarity of VBUS_DETECT_IO input pin: 0: Active low 1: Active high	1	1	1
		1	Reserved	Reserved	0	0	0
		0	Reserved	Reserved	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
	27:24	31:0	USB2EXTATTR	Bit map encoding of supported device level features (Refer USB 2.0 ECN Errata for LPM) Bit 0 - Reserved. Must be zero Bit 1 - LPM. A value of one in this bit location indicates that this device supports LPM Bit 2 - BESL & Alternate HIRD definitions supported. The LPM bit must be set to a one when this bit is one Bit 3 - Recommended Baseline BESL valid Bit 4 - Recommended Deep BESL valid Bit 11:8 - Recommended Baseline BESL value. Field shall be ignored by system software if bit[3] is a zero Bit 15:12 - Recommended Deep BESL value. Field shall be ignored by system software if bit[4] is zero Bit 31:16 - Reserved. Must be set to zero	0x0006	0x0006	0x0006
	29:28	15:0	bcdUSB	bcdUSB -> Device Descriptor	0x210	0x210	0x210
Hub config	30	7:0	iMANUFACTURER	Offset of Hub Manufacturer string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	31		iPRODUCT	Offset of Hub product string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	32		iSERIAL_NUM	Offset of Serial Number string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	33	7:0	iCFG_HS	Offset of HS configuration string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	34		iCFG_FS	Offset of FS configuration string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	35		iINTF_FS	Offset of FS interface string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	36		iINTF_HS_AS0	Offset of HS alt setting 0 string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	37		iINTF_HS_AS1	Offset of HS alt setting 1 string descriptor stored in variable part of configuration table	0x00	0x00	0x00

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Hub config	38	7:4	OC_TIMER	Time in milliseconds for which the overcurrent inputs will be filtered	8	8	8
		3	I2cIntrDisable	Disable support for I2C_INT pin: 1: I2C_INT function is not supported 0: I2C_INT function is supported	0	0	1
		2	I2cIntrPinSelect	Select pin used for I2C_INT function: 0: I2C_INT pin (40-QFN) or XGPIO1 pin (36-LGA) is used 1: I2C_INT pin (36-LGA) is used	0	0	0
		1	I2cIntrConfig	Configuration for I2C_INT pin: 0: Active low with internal pull-up enabled 1: Active low in open drain mode	1	1	1
		0	I2CArbitrationEnable	Whether I2C_INT pin should be used for I2C master (PD Controller)	0	0	0
UUID	39	7	SpiMasterEnable	Whether SPI interface is supported on this part	0	0	0
		6	SpiBootConfigEnable	Whether boot loader should wait for I2C based config update before attempting to boot from SPI flash	0	0	0
		5:4	SpiSsnPinSelect	Select pin to be used for SPI_CS function: 0: Invalid 1: DS4_PWREN/SPI_CS pin (40-QFN CYUSB2354 only) 2: SWDDIO/SPI_CS/I2C_ARB pin (40-QFN) 3: Invalid	2	2	2
		3:2	SpiClkPinSelect	Select pin to be used for SPI_CLK function: 0: Invalid 1: DS3_PWREN/SPI_CLK pin(40-QFN CYUSB2354 only) 2: VBUS_DETECT_IO (40-QFN) 3: Invalid	1	0	0
		1	DieSpecificUUIDEnable	Enable generation of die specific UUID (Container ID) for both Hub and USBFS device	1	1	1
		0	DieSpecificSerial-Number Enable	Enable generation of die specific Serial Number string for the hub	1	1	1

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
UUID	55:40	127:0	UUID (Container ID)	Unique serial number to be used Container IDs/UUIDs. When provided as part of boot, will provide the default values to be used. Bytes 2 to 15 can be over-ridden with die specific values generated by ROM based on DieSpecificUUIDEnable setting. When config table is read after application is running, will reflect the UUID actually in use (with generated bytes)	Die ID	Die ID	Die ID
PHY0 CONFIG (US Port)	56	7:4	PHY0_HS_TX_AM-PLITUDE	HS driver amplitude control (0x0 to 0xF)	5	5	5
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0
	57	7	PHY0_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction 0: disabled 1: enabled	0	0	0
		6	PHY0_HS_T-ED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY0_HS_DRIVER_FINE_SLEW_SEL	HS driver fine slew rate control (0x00, 0x01, 0x10, 0x11)	0	0	0
		2:0	PHY0_HS_TX_PRE_EMPHASIS	HS driver pre-emphasis amplitude (0x0 to 0x7)	4	4	4
	58	7:6	PHY0_FS_DRIVER_SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	Reserved	Reserved	0	0	0
		2:0	PHY0_HS_CTLE	HS receiver CTLE control (0x0 to 0x7)	0	0	0
	59	7	PHY0_DIS_PRE_EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet.	0	0	0
		6:5	PHY0_HS_TX-_PRE_EMP_DURATION	Selects pre-emphasis phase 2: pll phase 4	2	2	2
		4	Reserved	Reserved	0	0	0
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
PHY2 CONFIG (DS1 Port)	64	7:4	PHY2_HS_TX_ AMPLITUDE	HS driver amplitude control (0x0 to 0xF)	5	5	5
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0
	65	7	PHY2_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction. 0: disabled 1: enabled	0	0	0
		6	PHY2_HS_TED_ LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY2_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control (0x00, 0x01, 0x10, 0x11)	0	0	0
		2:0	PHY2_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude (0x0 to 0xF)	4	4	4
	66	7:6	PHY2_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	Reserved	Reserved	0	0	0
		2:0	PHY2_HS_CTLE	HS receiver CTLE control (0x0 to 0xF)	0	0	0
	67	7	PHY2_DIS_PRE_ EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet.	0	0	0
		6:5	PHY2_HS_TX_PRE_ EMP_DURATION	Selects pre-emphasis phase 2: pll phase 4	2	2	2
		4	Reserved	Reserved	0	0	0
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
PHY3 CONFIG (DS2 Port)	68	7:4	PHY3_HS_TX_ AMPLITUDE	HS driver amplitude control (0x0 to 0xF)	5	5	5
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0
	69	7	PHY3_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction. 0: disabled 1: enabled	0	0	0
		6	PHY3_HS_ TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY3_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control (0x00, 0x01, 0x10, 0x11)	0	0	0
		2:0	PHY3_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude (0x0 to 0xF)	4	4	4
	70	7:6	PHY3_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	Reserved	Reserved	0	0	0
		2:0	PHY3_HS_CTLE	HS receiver CTLE control (0x0 to 0xF)	0	0	0
	71	7	PHY3_DIS_PRE_ EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet.	0	0	0
		6:5	PHY3_HS_TX_PRE_ EMP_DURATION	Selects pre-emphasis phase 2: pll phase 4	2	2	2
		4	Reserved	Reserved	0	0	0
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
PHY4 CONFIG (DS3 Port)	72	7:4	PHY4_HS_TX_ AMPLITUDE	HS driver amplitude control (0x0 to 0xF)	5	5	5
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0
	73	7	PHY4_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction. 0: disabled 1: enabled	0	0	0
		6	PHY4_HS_TED_ LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY4_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control (0x00, 0x01, 0x10, 0x11)	0	0	0
		2:0	PHY4_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude (0x0 to 0xF)	4	4	4
	74	7:6	PHY4_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	Reserved	Reserved	0	0	0
		2:0	PHY4_HS_CTLE	HS receiver CTLE control (0x0 to 0xF)	0	0	0
	75	7	PHY4_DIS_PRE_ EMPHASIS_ HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet	0	0	0
		6:5	PHY4_HS_TX_ PRE_EMP_ DURATION	Selects pre-emphasis phase 2: pll phase 4	2	2	2
		4	Reserved	Reserved	0	0	0
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
PHY5 CONFIG (DS4 Port)	76	7:4	PHY5_HS_TX_ AMPLITUDE	HS driver amplitude control (0x0 to 0xF)	5	5	5
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0
	77	7	PHY5_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction. 0: disabled 1: enabled	0	0	0
		6	PHY5_HS_TED_ LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY5_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control (0x00, 0x01, 0x10, 0x11)	0	0	0
		2:0	PHY5_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude (0x0 to 0xF)	4	4	4
	78	7:6	PHY5_FS_DRIVER_SR_ SEL_1	FS driver slew rate control	0	0	0
		5:3	Reserved	Reserved	0	0	0
		2:0	PHY5_HS_CTLE	HS receiver CTLE control (0x0 to 0xF)	0	0	0
	79	7	PHY5_DIS_PRE_ EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet.	0	0	0
		6:5	PHY5_HS_TX_PRE_ EMP_DURATION	Selects pre-emphasis phase 2: pll phase 4	2	2	2
		4	Reserved	Reserved	0	0	0
		3:2	Reserved	Reserved	0	0	0
		1:0	Reserved	Reserved	0	0	0
Full-Speed Dev [5] Parameters	80	7:2	laneSwapEnable	This field decides LAN-SWAP parameter from external config is applicable or not.	–	–	–
		1:0	Reserved	Reserved	–	–	–
	83:81	23:0	Reserved	Reserved	–	–	–
	85:84	15:0	FSDEV_VID	Vendor ID to be used for USBFS device	0x04B4	0x04B4	0x04B4
	87:86	15:0	FSDEV_PID	Product ID to be used for USBFS Device	0X6520	0X6520	0X6520
	89:88	15:0	FSDEV_VERS	bcdDevice used for USBFS device	0x0001	0x0001	0x0001
	90	7:0	BB_NumberOfAlterna-teOrUSB4vModes	Number of Alternate Modes supported by Device Container It takes values from 1 to 8	1	1	1

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Full-Speed Dev [5] Parameters	91	7:0	BB_PreferredAlternate-OrUSB4Mode	Index of the preferred Alternate mode. (bPreferredAlternate OrUSB4Mode of BB capability decriptor) It takes values from 0 to 7 for setting the preferred mode. If USB4 mode is supported, that is the preferred mode (Mode 0). 0xFF - indicates no preference	0xFF	0xFF	0xFF
	107:92	127:0	FSDEV_UUID	Unique serial number to be used Container IDs/UUIDs. When provided as part of boot, will provide the default values to be used. Bytes 2 to 15 can be over-ridden with die specific values generated by ROM based on DieSpecificU-UIDEnable setting. When config table is read after application is running, will reflect the UUID actually in use (with generated bytes)	–	–	–
	109:108	15:0	BB_SVID_0	SVID for the first Alternate Mode or USB4 mode	0	0	0
	110	7:0	BB_AUM_0	Index of AUM for SVID #0	0	0	0
	111	7:0	BB_AM_STRING_0	Offset of string descriptor for Alternate Mode #0	0	0	0
	113:112	15:0	BB_SVID_1	SVID for the second Alternate Mode or USB4 mode	0	0	0
	114	7:0	BB_AUM_1	Index of AUM for SVID #1	0	0	0
	115	7:0	BB_AM_STRING_1	Offset of string descriptor for Alternate Mode #1	0	0	0
	117:116	15:0	BB_SVID_2	SVID for the third Alternate Mode or USB4 mode	0	0	0
	118	7:0	BB_AUM_2	Index of AUM for SVID #2	0	0	0
	119	7:0	BB_AM_STRING_2	BB_AM_STRING_2 Offset of string descriptor for Alternate Mode #2	0	0	0
	121:120	15:0	BB_SVID_3	SVID for the fourth Alternate Mode or USB4 mode	0	0	0
	122	7:0	BB_AUM_3	Index of AUM for SVID #3	0	0	0
	123	7:0	BB_AM_STRING_3	Offset of string descriptor for Alternate Mode #3	0	0	0
	125:124	15:0	BB_SVID_4	SVID for the fifth Alternate Mode or USB4 mode	0	0	0
	126	7:0	BB_AUM_4	Index of AUM for SVID #4	0	0	0
	127	7:0	BB_AM_STRING_4	Offset of string descriptor for Alternate Mode #4	0	0	0
	129:128	15:0	BB_SVID_5	SVID for the sixth Alternate Mode or USB4 mode	0	0	0
	130	7:0	BB_AUM_5	Index of AUM for SVID #5	0	0	0

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

Table 4 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for consumer CYUSB2354	Default value for consumer CYSUB2352	Default value for consumer CYSUB2364
Full-Speed Dev [5] Parameters	131	7:0	BB_AM_STRING_5	Offset of string descriptor for Alternate Mode #5	0	0	0
	133:132	15:0	BB_SVID_6	SVID for the seventh Alternate Mode or USB4 mode	0	0	0
	134	7:0	BB_AUM_6	Index of AUM for SVID #6	0	0	0
	135	7:0	BB_AM_STRING_6	Offset of string descriptor for Alternate Mode #6	0	0	0
	137:136	15:0	BB_SVID_7	SVID for the eighth Alternate Mode or USB4 mode	0	0	0
	138	7:0	BB_AUM_7	Index of AUM for SVID #7	0	0	0
	139	7:0	BB_AM_STRING_7	Offset of string descriptor for Alternate Mode #7	0	0	0
	143:140	31:0	BB_AM_VDO_0	dwAlternateModeVdo value for Alternate Mode #0	0	0	0
	147:144	31:0	BB_AM_VDO_1	dwAlternateModeVdo value for Alternate Mode #1	0	0	0
	151:148	31:0	BB_AM_VDO_2	dwAlternateModeVdo value for Alternate Mode #2	0	0	0
	155:152	31:0	BB_AM_VDO_3	dwAlternateModeVdo value for Alternate Mode #3	0	0	0
	159:156	31:0	BB_AM_VDO_4	dwAlternateModeVdo value for Alternate Mode #4	0	0	0
	163:160	31:0	BB_AM_VDO_5	dwAlternateModeVdo value for Alternate Mode #5	0	0	0
	167:164	31:0	BB_AM_VDO_6	dwAlternateModeVdo value for Alternate Mode #6	0	0	0
	171:168	31:0	BB_AM_VDO_7	dwAlternateModeVdo value for Alternate Mode #7	0	0	0
	172	7:0	iManufacturer_FSDEV	Offset of FSDEV manufacturer string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	173	7:0	iProduct_FSDEV	Offset of FSDEV product string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	174	7:0	iSerNum_FSDEV	Offset of FSDEV product string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	175	7:0	iConfig_FSDEV	Offset of FSDEV product string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	176	7:0	iCDCCtrlIntf	Offset of CDC control interface string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	177	7:0	iCDCDataIntf	Offset of CDC control interface string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	191:178	7:0	Reserved	Reserved	–	–	–

Note
5. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

3.8.2 I2C Slave register space

Table 5 lists I2C slave registers that exist in addition to the configuration table for status and dynamic configuration of EZ-USB™ HX2G3.

Table 5 I2C Slave registers

Register address	Bit range	Register/ Field name	Default value	Description	Access permission[7,8,9]
0xF000	31:0	DEVICE_STATE	"APPL"	Device state (boot mode or application) indication[6]	RO
0xF004	31:0	RESERVED	0	Reserved: Will read as zero	RO
0xF008	31:0	RESERVED	0	Reserved: Will read as zero	RO
0xF00C	31:0	UFP_DFP configuration with US port selection	0	This register is used for runtime selection of Upstream - Downstream configuration • Byte3(MSB) - Reserved • Byte2 - Reserved • Byte1 - 0 valid for 1UFP + 4DFP - 0,1 valid for 2UFP + 4DFP - 0,1,2 valid for 3UFP +3DFP • Byte0 - 001: For 1UFP + 4DFP Configuration - 010: For 2UFP + 4DFP Configuration - 100: For 3UFP +3DFP Configuration All invalid input leads to 1UFP +4DFP and US-0 configuration in system	W
0xF010	0	US_VBUS_STATUS	0	Upstream Vbus status. If Vbus detect is disabled, this bit will always be set to 1	RO
	6	US_VBUS_OVERRIDE_VALUE	0	If US_VBUS_OVERRIDE_ENABLE is set to 1, US_VBUS_STATUS will be overridden by the value of this register	RW
	7	US_VBUS_OVERRIDE_ENABLE	0	Whether US_VBUS_STATUS should be over-ridden 1: Override the US_VBUS_STATUS value 0: No override. Actual VBUS pin value will be considered	RW
0xF014	1:0	NUM_US_PORT_OPTIONS	1	Number of upstream port options available (1, 2 or 3). This value will get reflected based on the register configuration made in 0xF00C	RO
	3:2	CUR_US_PORT_ID	0	Currently selected upstream port 0: US_DP/US_DM 1: US_ALT_DP/US_ALT_DM 2: US_ALT1_DP/US_ALT1_DM This value will get reflected based on the register configuration made in 0xF00C.	RO
	6:4	NUM_DS_PORTS	3	Number of external DS ports supported. This value will get reflected based on the register configuration made in 0xF00C	RO
	7	FSDEV_PRESENT	1	Whether embedded FSDEV is enabled. This value is reflected as per the configuration table parameter	RO

Notes
6. In Boot mode only Firmware download is supported.
7. Read operation of I2C Slave register should be always in 4 bytes for one cycle.
8. Write operation of I2C Slave register should be always in 4 bytes for one cycle.
9. Read Only, Read & Write and Write Only are abbreviated as RO, RW and W respectively.

Table 5 I2C Slave registers *(continued)*

Register address	Bit range	Register/ Field name	Default value	Description	Access permission[7,8,9]
0xF018	1:0	MUXSEL_OVRD_VAL[1:0]	0	Value to override the MUXSEL1 and MUXSEL0 pin status	RW
	7	MUXSEL_OVRD_EN	0	Whether MUXSEL pin status is to be overridden. 1: Override the US_VBUS_STATUS value 0: No override. MUXSEL0 & MUXSEL1 GPIO pins will be used.	RW
0xF01C	3:0	DS_PWREN_STATUS[3:0]	0x0	Power enable status for each of the downstream ports. Each bit can be over-written with the value provided if the corresponding DS_PWREN_OVRD bit is set.	RW
	7:4	DS_PWREN_OVRD[3:0]	0x0	Whether to over-ride the DS_PWREN_STATUS bits for each downstream port with the value provided. 1: Override the US_VBUS_STATUS value 0: No override	RW
0xF024	3:0	OC_FAULT_STATUS[3:0]	0x0	Over-current fault status for each of the downstream ports	RW
	7:4	OC_FAULT_OVRD[7:4]	0x0	Whether to over-ride the OC_FAULT_STATUS for each downstream port with the value provided. 1: Override the OC_FAULT_STATUS value 0: No override	RW

Notes
6. In Boot mode only Firmware download is supported.
7. Read operation of I2C Slave register should be always in 4 bytes for one cycle.
8. Write operation of I2C Slave register should be always in 4 bytes for one cycle.
9. Read Only, Read & Write and Write Only are abbreviated as RO, RW and W respectively.

4 Functional overview

4.1 Initialization

Power up sequence is not required, the EZ-USB™ HX2G3 device will boot when input power is stable and reset pin is HIGH. It is not recommended to provide voltage in I/O pins before the chip is powered using VDDD and VDDIO.

4.1.1 Initialization

The EZ-USB™ HX2G3 power-ON behavior expectation during initialization requires the following:

- Logic initialization: Logic initializes and assumes “nominal” operation within 5 ms after power has reached “nominal” conditions. The oscillator is enabled and remains active during power-up and reset conditioning
- I/O initialization: All output drivers remain in the High-Z state until the power reaches “nominal” conditions
- Program Initialization: The CPU executes ROM code and loads configuration into the device’s registers from an external I2C EEPROM, I2C host, or eFuse

4.1.2 Reset sequence

EZ-USB™ HX2G3 includes an active-low reset pin. When asserted and released, the Hub registers are initialized, USB communication is stopped, and the bootloader reinitializes the Hub. EZ-USB™ HX2G3 continues to enumerate with the host and the available downstream devices.

4.2 Power modes

EZ-USB™ HX2G3 supports three power modes: Active, Deep Sleep, and Reset.

4.2.1 Active mode

Active mode is the normal operating power mode where all chip resources that are used by the system are active and all clocks are running.

4.2.2 Deep Sleep

In Deep Sleep mode, all states are retained and the high-speed clock (IMO, ECO, PLL) is disabled. The low-speed clock (ILO) remains enabled and low-speed peripherals can remain active (for example, allowing wake up on I2C). This mode allows operation to resume at the same program counter value and will be the most frequently used mode when fast wake-up and operation restart is required. The device state is fully retained in this mode and SRAM is retained. Stack and critical parameters can be retained while allowing memory holding temporary and scratch pad variables to be powered off to reduce the leakage. The USB 2.0 PHYs are in suspend state but can be used for wake-up.

4.2.3 Reset

XRES pin is used for reset operation. Pulling XRES pin LOW resets the device.

5 Pin configurations

5.1 Pinout diagram

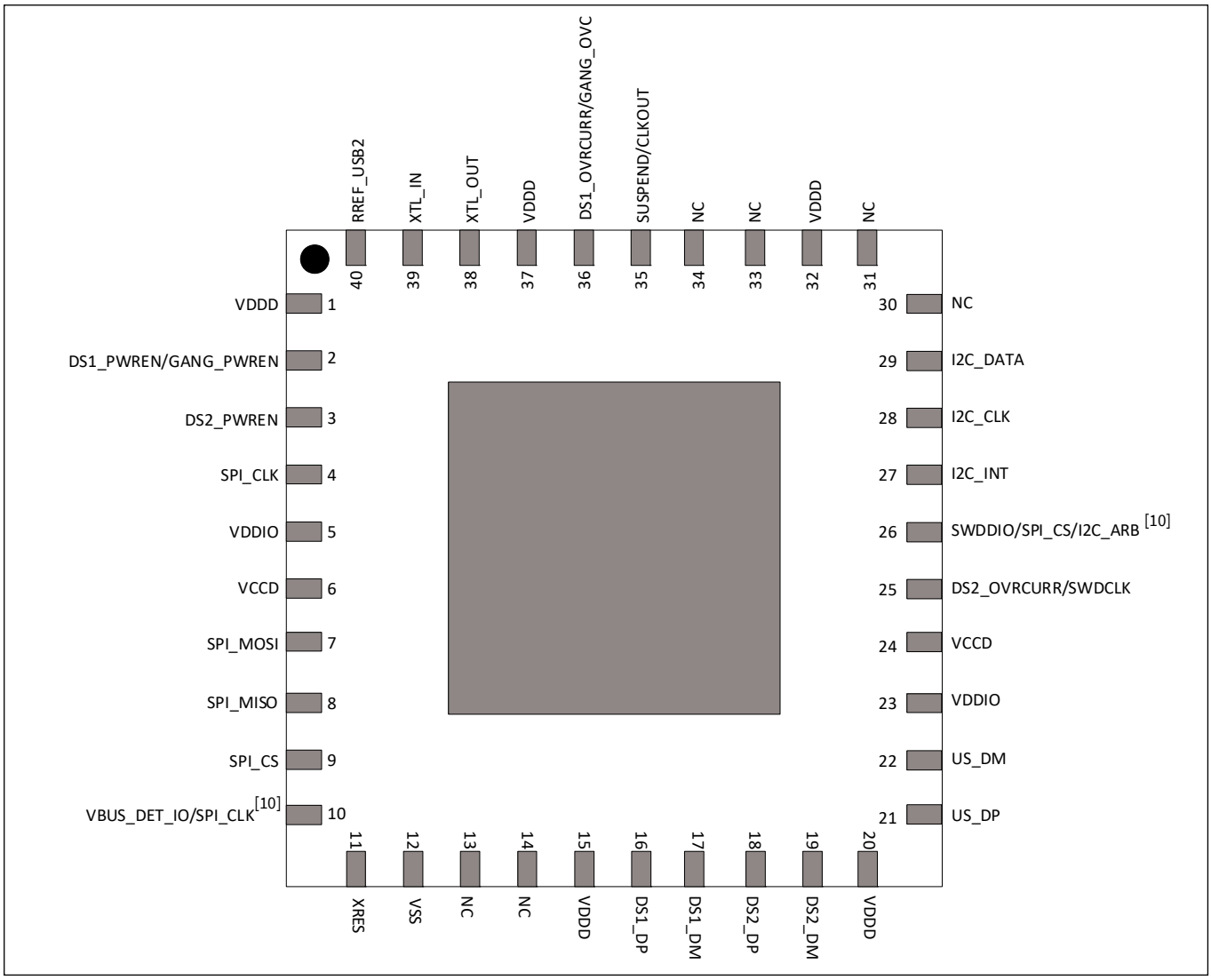


Figure 6 CYUSB2352-40LTXI (40-pin QFN) pinout (top view)

Note

10. By default, Pin 4 and pin 9 are SPI_CLK and SPI_CS respectively. Pin 10 and Pin 26 need to configured in the external config table to be used as SPI_CLK and SPI_CS respectively.

Pin configurations

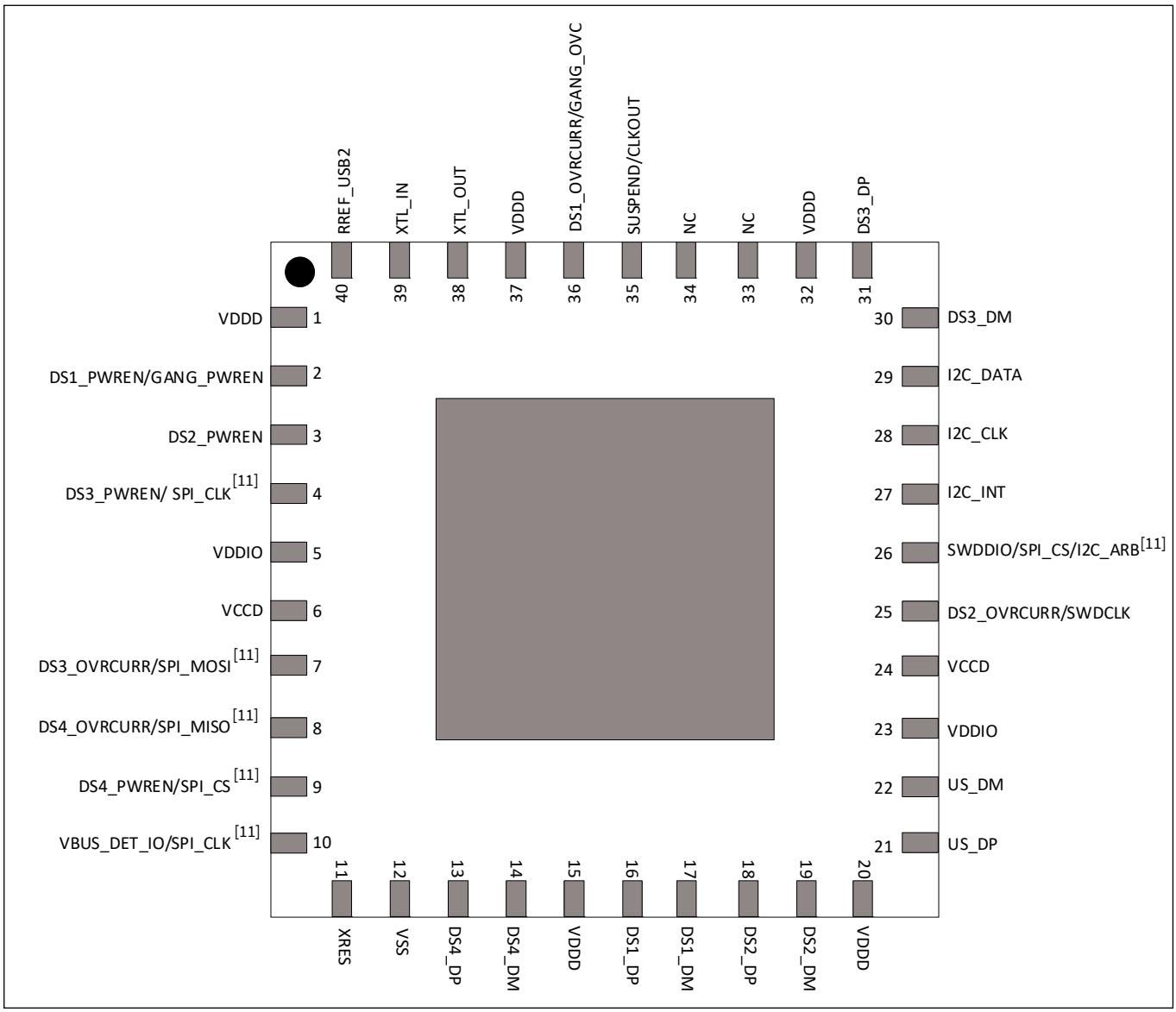


Figure 7 CYUSB2354-40LTXI (40-pin QFN) pinout (top view)

Note

11. By default SPI is not enabled. Enable SPI and the pins through external config table. Ensure that kit device is in ganged power mode and ganged over current mode to use SPI.

Pin configurations

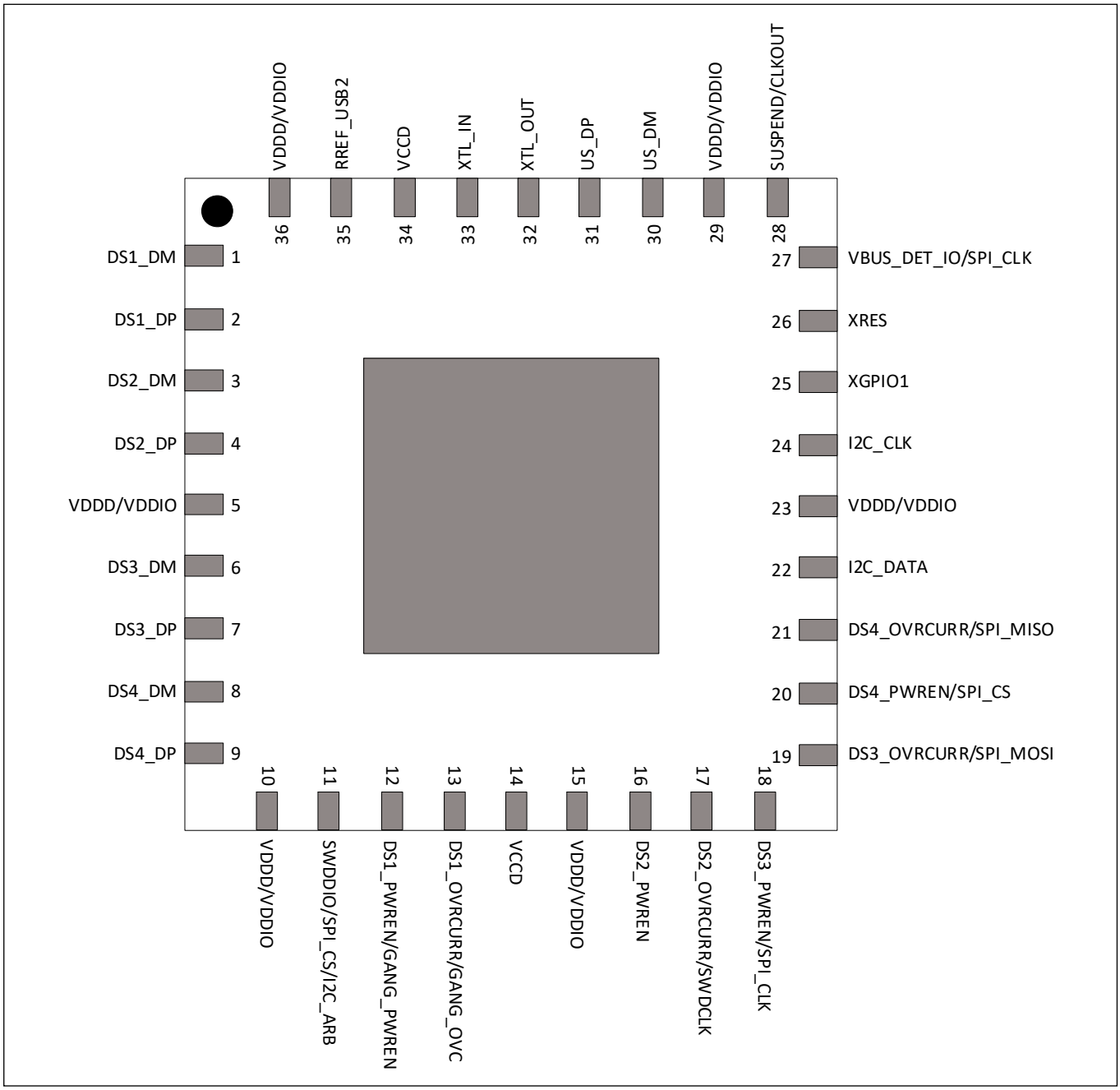


Figure 8 CYUSB2364-36BFXI (36-pin LGA) pinout (top view)

5.2 EZ-USB™ HX2G3 product pin list

Table 6 EZ-USB™ HX2G3 Consumer product pin list

Pin type	Pin name	CYUSB2352-40	CYUSB2354-40	CYUSB2364-36	Pin description
A	RREF_USB2	40	40	35	Reference resistor for USB 2.0 current generator (The recommended resistor value is 6.04 KΩ 1%)
PWR	VCCD	6,24	6,24	14,34	Internal core logic supply, VCCD, needs to be decoupled externally. See **Table 9** for the recommended capacitor specification. This is not to be used as an input or output power supply
	VDDD	1,15,20,32,37	1,15,20, 32,37	5,10,15, 23,29,36	Main digital supply input. It provides the inputs for the internal regulators. Also the power supply for the USB 2 HS PHY
	VDDIO	5,23	5,23	5,10,15,23,29,36	GPIO input power supply
	NC	13,14,30, 31, 33, 34	33, 34	–	No Connection
GND	VSS	12	12	EPAD	Ground for the entire chip
	EPAD	EPAD	EPAD	EPAD	Exposed pad connected directly to Ground
I/O	DS1_DM	17	17	1	USB 2.0 Data Minus - DS Port 1
	DS1_DP	16	16	2	USB 2.0 Data Plus - DS Port 1
	DS1_OVERCURR /GANG_OVC	36	36	13	GPIO, programmable as overcurrent detect for the DS1. By default Overcurrent pin is active LOW
	DS1_PWREN/GA NG_PWREN	2	2	12	GPIO, programmable as VBUS power enable output for port DS1. By default power enable pin is active low.When the port is not active, the default state for the pin is tristate
	DS2_DM	19	19	3	USB 2.0 Data Minus - DS Port 2
	DS2_DP	18	18	4	USB 2.0 Data Plus - DS Port 2
	DS2_OVRCURR/ SWDCLK	25	25	17	GPIO, programmable as overcurrent detect for the DS2.By default Overcurrent pin is active LOW. This pin is used as clock pin for SWD interface
	DS2_PWREN	3	3	16	GPIO, programmable as VBUS power enable output for port DS2. By default power enable pin is active low. When the port is not active, the default state for the pin is tristate
	DS3_DM	–	30	6	USB 2.0 Data Minus - DS Port 3

Table 6 EZ-USB™ HX2G3 Consumer product pin list *(continued)*

Pin type	Pin name	CYUSB2352-40	CYUSB2354-40	CYUSB2364-36	Pin description
I/O	DS3_DP	–	31	7	USB 2.0 Data Plus - DS Port 3
	DS3_OVRCURR	–	–	19	GPIO, programmable as overcurrent detect for the DS3. By default Overcurrent pin is active LOW
	DS3_PWREN/ SPI_CLK	–	4	–	GPIO, programmable as VBUS power enable output for port DS3. By default power enable pin is active low.When the port is not active, the default state for the pin is tristate. Alternatively, can be used for SPI clock pin
	DS3_PWREN	–	–	18	GPIO, programmable as VBUS power enable output for DS3. By default, power enable pin is active low. When the port is not active, the default state for the pin is tristate
	SPI_CLK	4	–	–	SPI clock
	DS4_DM	–	14	8	USB 2.0 Data Minus - DS Port 4
	DS4_DP	–	13	9	USB 2.0 Data Plus - DS Port 4
	SPI_CS	9	–	–	SPI Chip select
	DS4_OVRCURR	–	–	21	GPIO, programmable as overcurrent detect for the DS4.By default Overcurrent pin is active LOW
	DS4_PWREN/ SPI_CS	–	9	–	GPIO, programmable as VBUS power enable output for port DS4. By default power enable pin is active low. When the port is not active, the default state for the pin is tristate. Alternatively, can be used for SPI clock pin
	DS4_PWREN	–	–	20	GPIO, programmable as VBUS power enable output for DS4. By default, power enable pin is active low. When the port is not active, the default state for the pin is tristate
	I2C_CLK	28	28	24	I2C clock, used as GPIO when the I2C interface is not supported
	I2C_DATA	29	29	22	I2C data, used as GPIO when the I2C interface is not supported
	I2C_INT	27	27	–	I2C interrupt, used as GPIO when the I2C interface is not supported

Pin configurations

Table 6 EZ-USB™ HX2G3 Consumer product pin list *(continued)*

Pin type	Pin name	CYUSB2352-40	CYUSB2354-40	CYUSB2364-36	Pin description
I/O	DS3_OVRCURR/ SPI_MOSI	–	7	–	GPIO, programmable as overcurrent detect for the DS3. By default Overcurrent pin is active low. Additionally, programmable as SPI data from an external source to the hub SPI master/slave. In Master mode, it is an output. In Slave mode, it is an input
	SPI_MOSI	7	–	–	Master out Slave In pin for SPI
	SPI_MISO	8	–	–	Master In Slave Out Pin for SPI
	DS4_OVRCURR/ SPI_MISO	–	8	–	GPIO, programmable as overcurrent detect for the DS4.By default Overcurrent pin is active low. Also programmable as SPI data from the hub to an external SPI master/slave. In Master mode it is an input. In Slave mode it is an output
	SUSPEND/ CLKOUT	35	35	28	GPIO, programmable as HUB Suspend indication. This pin is asserted if the USB 2.0 hub is in suspend state and is deasserted when the hub comes out of the Suspend state. Alternatively, can be used as clock output for cascading the Hub
	SWDDIO/ SPI_CS/I2C_ARB	26	26	–	SWDIO pin for SWD interface. Programmable as SPI Chip Select. I2C_ARB functionality is used during I2C Multimaster environment [12]
	SWDDIO/ I2C_INT/ I2C_ARB	–	–	11	GPIO, SWDDIO pin for SWD interface. I2C interrupt. I2C_ARB functionality is used during I2C Multimaster environment
	US_DM	22	22	30	USB 2.0 Data Minus - US Port
	US_DP	21	21	31	USB 2.0 Data Plus - US Port
	VBUS_DET_IO	–	–	27	VBUS detect
	VBUS_DET_IO/ SPI_CLK	10	10	–	VBUS detect, also programmable as SPI Clock. **Note**: In CYUSB2354-40, SPI is enabled by default, and SPI_CLK is routed to Pin 4 (DS3_PWREN/SPI_CLK) to preserve the VBUS_DET_IO pin. Consequently, since the DS3_PWREN function on Pin 4 is unavailable, CYUSB2354-40 operates in gang-powered mode by default

Table 6 EZ-USB™ HX2G3 Consumer product pin list *(continued)*

Pin type	Pin name	CYUSB2352-40	CYUSB2354-40	CYUSB2364-36	Pin description
I/O	XGPIO1	–	–	25	GPIO
	XRES	11	11	26	Active LOW Reset input
	XTAL_IN	39	39	33	Crystal IN
	XTAL_OUT	38	38	32	Crystal OUT

6 Electrical specifications

EZ-USB™ HX2G3 meets all USB-IF electrical compliance specifications.

6.1 Electrostatic discharge (ESD)

EZ-USB™ HX2G3 has a built-in ESD protection on all pins. The system-level ESD on all pins is the standard ±2 KV human-body model (HBM) and 500 V charged-device model (CDM).

On the DP and DM pins, the system-level ESD is HBM+CDM and IEC61000-4-2 to support ±8 KV contact and ±15 KV air discharge.

6.2 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit
VDD_ABS	Analog or digital supply relative to Vss (Vssd = Vssa)	–0.3	–	4	V
VDDIO_ABS	Max voltage on VDDIO	–0.3	–	4	V
VGPIO_OVT_ABS	OVT GPIO voltage	–0.5	–	4	V
IGPIO_ABS_DS0	Current per GPIO at Drive Strength = 0	–7.5	–	7.5	mA
IGPIO_ABS_DS1	Current per GPIO at Drive Strength = 1	–5.6	–	5.6	mA
IGPIO_ABS_DS2	Current per GPIO at Drive Strength = 2	–3.8	–	3.8	mA
IGPIO_ABS_DS3	Current per GPIO at Drive Strength = 3	–1.9	–	1.9	mA
ESD_HBM	Human body model (HBM) robustness according to ANSI/ESDA/JEDEC JS-001-2024	–2000	–	2000	V
ESD_CDM	Charged device model (CDM) robustness according to ANSI/ESDA/JEDEC JS-002-2022; voltage level refers to test condition (TC) mentioned in the standard	–500	–	500	V
LU	Pin current for latchup free operation	–100	–	100	mA
T_J	Junction temperature	–	–	125	°C
TSTG	Storage temperature	–65	–	150	°C
T_A	Operating temperature	–40	–	85	°C

Note

12. EZ-USB™ HX2G3 arbitration feature: In a multi-master system, this feature allows the EZ-USB™ HX2G3 to perform a synchronization with the other I2C master on the bus to request/release control of the bus. This is done by sending a fixed length pulse on the I2C_ARB pin.

6.3 Device-level specification

6.3.1 DC specifications

Table 8 DC specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDDD	Main analog supply	–	2.97	3.3	3.63	V
VDD_EFUSE	VDDD supply when programming eFuse	E-Fuse programming	2.38	2.5	2.62	V
VDDIO	Power supply voltage for IO	–	2.97	3.3	3.63	V
VCCD	Core logic supply	–	–	1.1	–	V
V_{IH_I2C}	I2C input voltage high threshold	–	0.7 × VDDIO	–	–	V
V_{IL_I2C}	I2C input voltage low threshold	–	–	–	0.3 × VDDIO	V
V_{IH_GPIO}	Input voltage HIGH level	–	0.65 × VDDIO	–	–	V
V_{IL_GPIO}	Input voltage LOW level	–	–	–	0.35 × VDDIO	V
V_{HYST_I2C}	Input hysteresis GPIO	–	0.1 × VDDIO	–	–	V
I_{IL}	Input leakage current (absolute value)	–	–1	–	1	µA
$I_{OH\_V3P3\_0}$	3.3 V pullup current, Drive Strength =0	–	–4.24	–	–11.76	mA
$I_{OL\_V3P3\_0}$	3.3 V pulldown current, Drive Strength =0	–	4.24	–	11.76	mA

Table 9 lists the decoupling capacitor information recommended for VCCD.

Table 9 VCCD decoupler capacitor specification

Parameter	Description	Min	Typ	Max	Unit
CDEC1	Decoupling capacitor on VCCD	1.88	4.7	6.58	µF

6.4 Power consumptions

Table 10 provides the power consumption values for EZ-USB™ HX2G3 under different conditions and combinations of active ports. All specification are valid for –40°C ≤ TA ≤ 85°C and 3.63 V except where noted.

Table 10 Power consumption with VDDD supply at 3.3 V

Parameter	Description	Min	Typ	Max	Unit
HX2G3_SUSPEND	Hub in Suspend and DS devices connected	–	1.1	2.5	mW
HX2G3_L0_SUSPEND	Hub in Suspend and No DS devices	–	1.1	2.5	
HX2G3_L0_1HS1	Hub in L0 and 1 HS device connected	–	210	250	
HX2G3_L0_2HS2	Hub in L0 and 2 HS device connected	–	225	260	
HX2G3_L0_3HS3	Hub in L0 and 3 HS device connected	–	240	270	
HX2G3_L0_4HS4	Hub in L0 and 4 HS device connected	–	255	285	
HX2G3_L0_1HS_RW	1 HS device connected with Read / Write	–	270	310	
HX2G3_L0_2HS_RW	2 HS device connected with Read / Write	–	390	440	
HX2G3_L0_3HS_RW	3 HS device connected with Read / Write	–	500	580	
HX2G3_L0_4HS_RW	4 HS device connected with Read / Write	–	600	665	
Power Down	XRES(RESET_N) asserted	–	200	-	µW

7 Package information

7.1 Package details

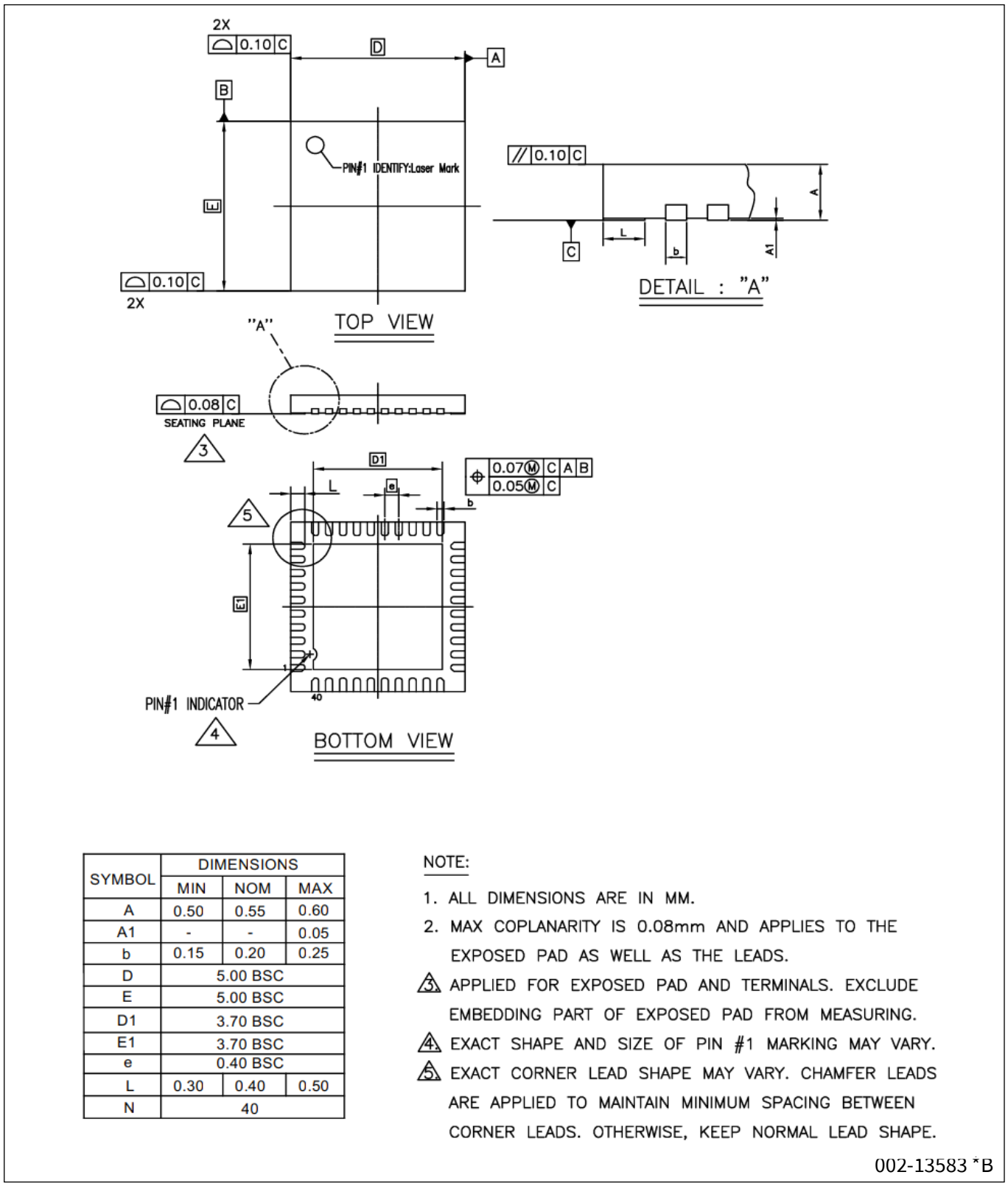
Table 11 40-QFN commercial package details

PKG_1	Package 1: type	Min	Typ	Max	Unit
PKG_1Z	Package 1: height	–	–	0.6	mm
PKG_1W	Package 1: width	4.9	5	5.1	mm
PKG_1L	Package 1: length	4.9	5	5.1	mm
PKG_1PTCH	Package 1: pin / bump pitch	–	0.4	–	mm
PKG_1CNT	Package 1: Total signal pins	–	40	–	–
PKG_1TJA	Package 1: Theta-JA	–	21.7	–	°C/W
PKG_1TJC	Package 1: Theta-JC	–	19.9	–	°C/W
–	Solder reflow	–	–	260	°C
–	MSL	3	–	–	–
–	T_A	–	85	–	°C
–	T_J	–	97.5	–	°C

Table 12 36-LGA commercial package details

PKG_1	Package 1: type	Min	Typ	Max	Unit
PKG_1Z	Package 1: height	–	–	0.9	mm
PKG_1W	Package 1: width	5.9	6	6.1	mm
PKG_1L	Package 1: length	5.9	6	6.1	mm
PKG_1PTCH	Package 1: pin / bump pitch	–	0.5	–	mm
PKG_1CNT	Package 1: Total signal pins	–	36	–	–
PKG_1TJA	Package 1: Theta-JA	–	63.87	–	°C/W
PKG_1TJC	Package 1: Theta-JC	–	36.79	–	°C/W
–	Solder reflow	–	–	260	°C
–	MSL	3	–	–	–
–	T_A	–	85	–	°C
–	T_J	–	108	–	°C

7.2 Package diagram



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	-	-	0.05
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
D1		3.70 BSC	
E1		3.70 BSC	
e		0.40 BSC	
L	0.30	0.40	0.50
N		40	

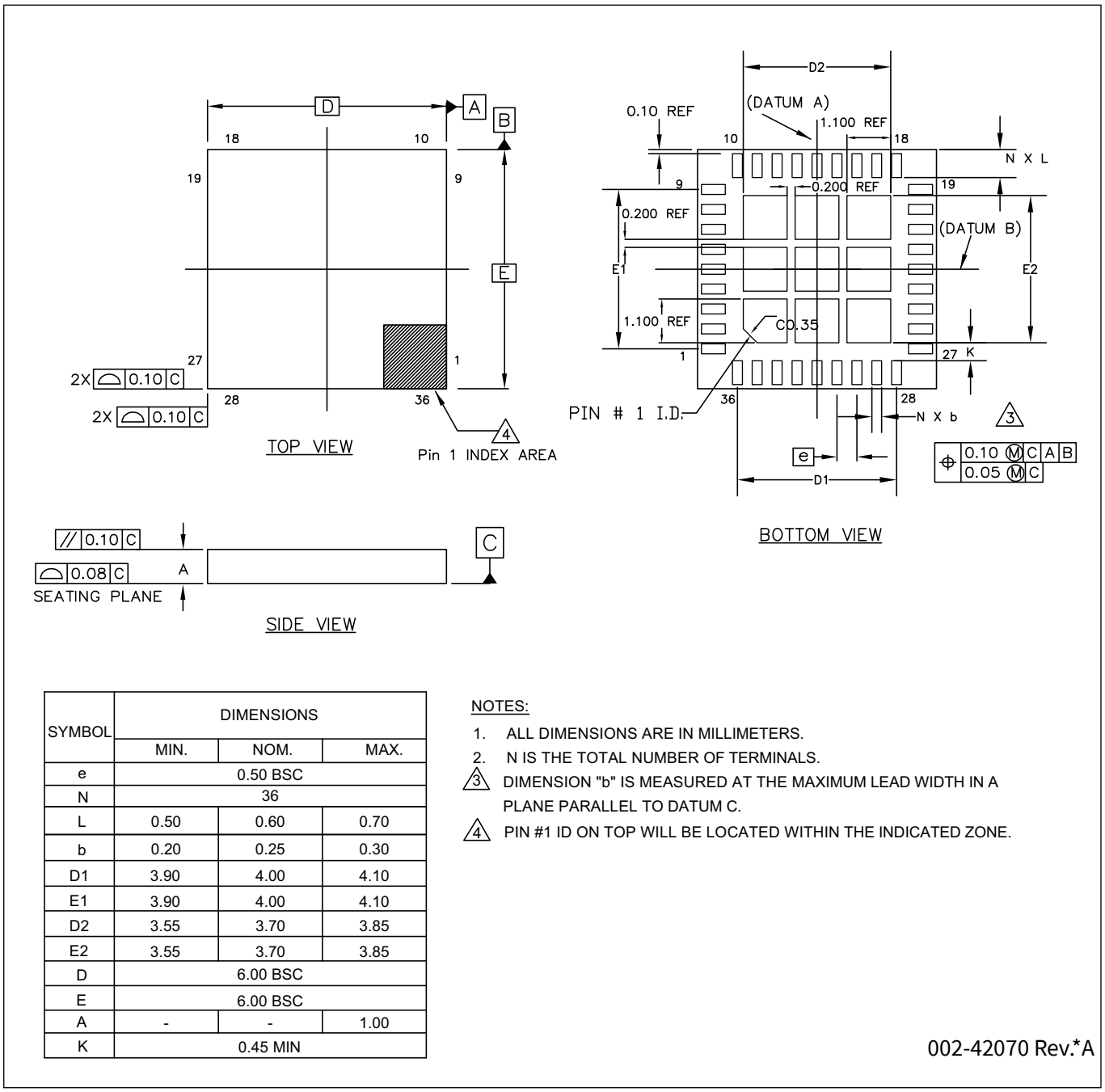
NOTE:

1. ALL DIMENSIONS ARE IN MM.
2. MAX COPLANARITY IS 0.08mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY.
5. EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

002-13583 *B

Figure 9 40-pin QFN (5.0 × 5.0 × 0.60 mm) LQ40D/LQ40E (PG-VQFN-40)

Package information



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.50 BSC	
N		36	
L	0.50	0.60	0.70
b	0.20	0.25	0.30
D1	3.90	4.00	4.10
E1	3.90	4.00	4.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
D		6.00 BSC	
E		6.00 BSC	
A	-	-	1.00
K		0.45 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM LEAD WIDTH IN A PLANE PARALLEL TO DATUM C.
4. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.

002-42070 Rev.*A

Figure 10 36-pin LGA (6.0 X 6.0 X 1.0 mm) L1A036

7.3 Package layout guidelines

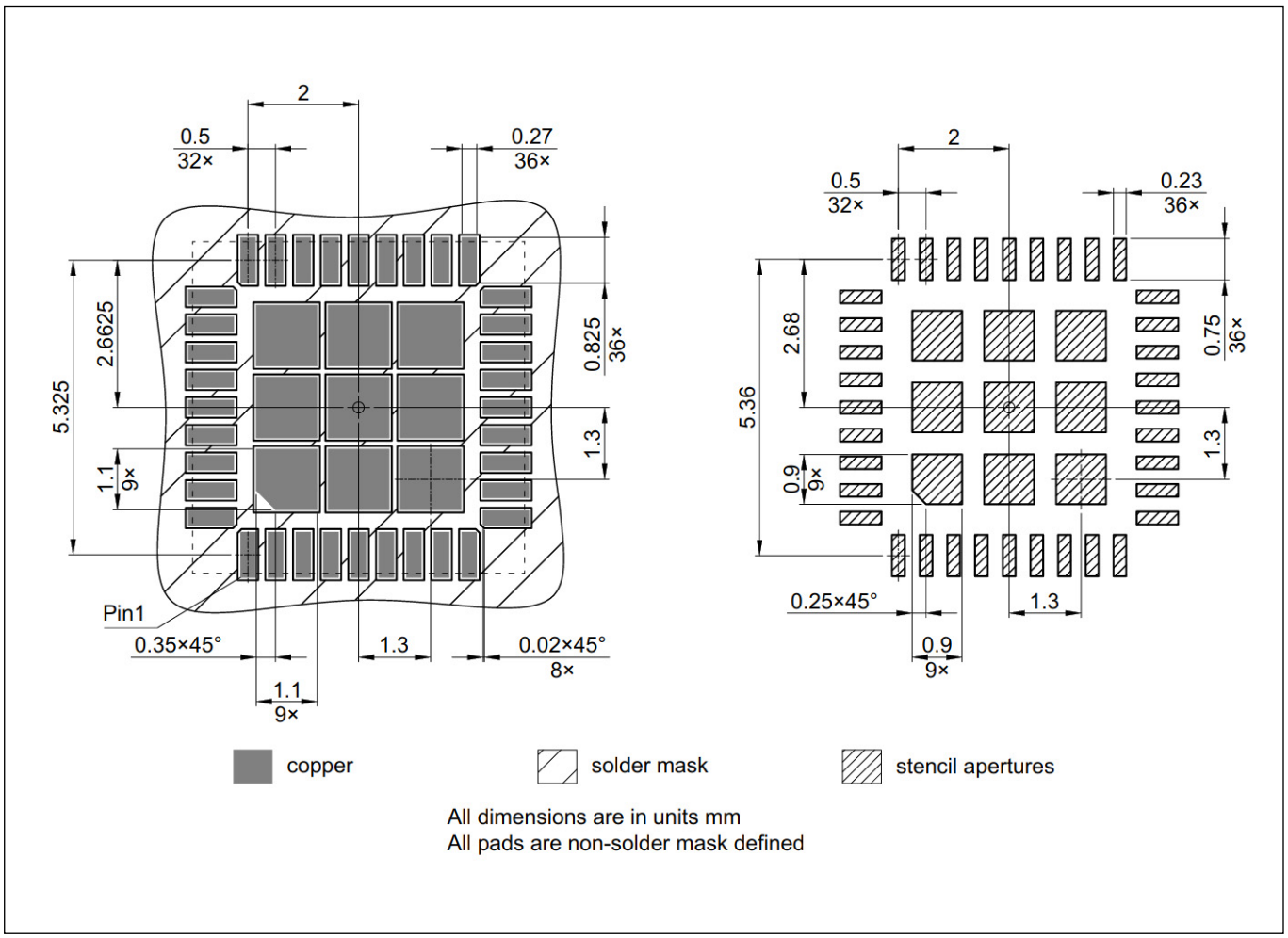


Figure 11 PG-VFLGA 36-LGA boardpads and apertures

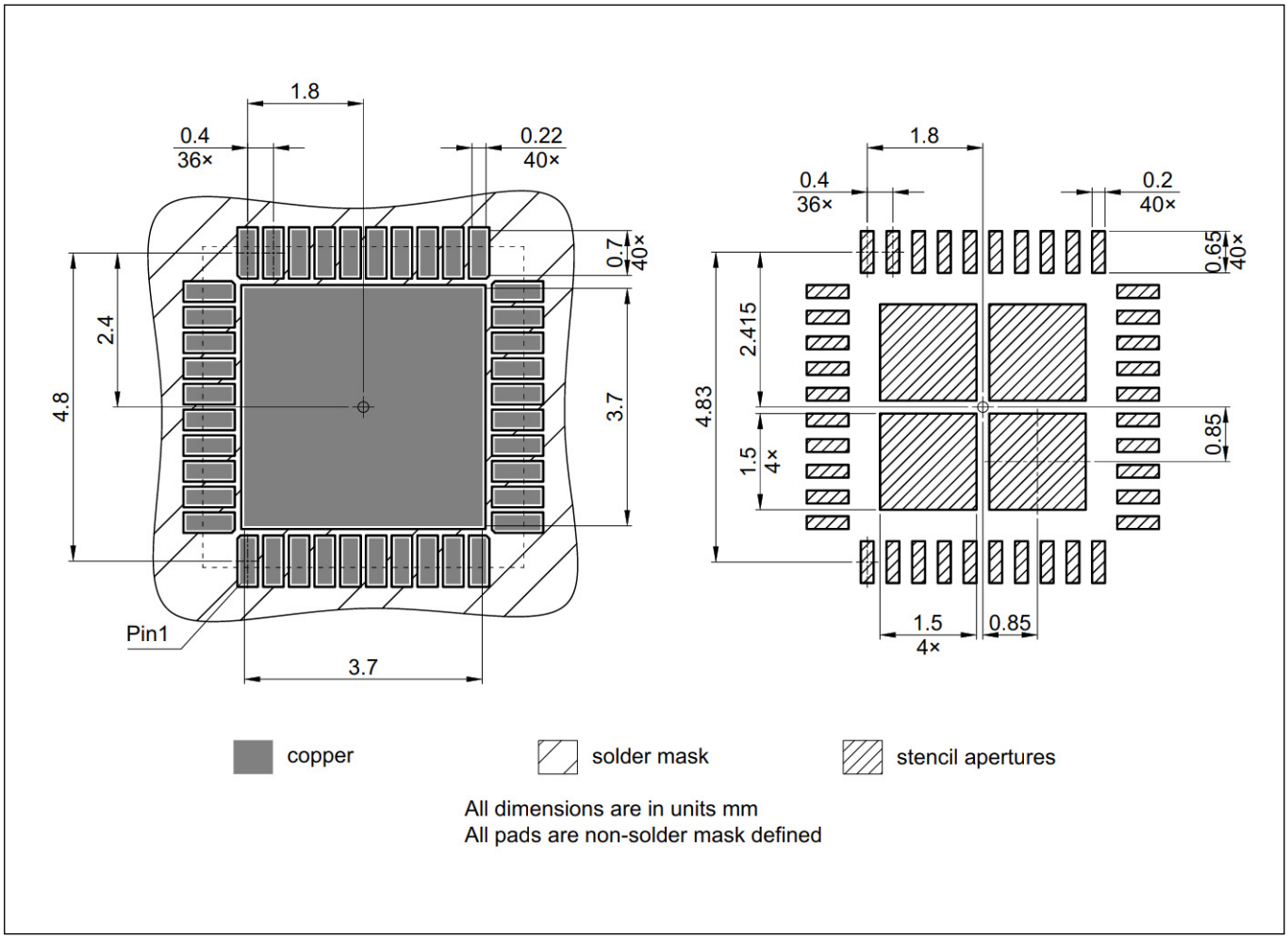


Figure 12 PG-UQFN 40 boardpads and apertures

8 Ordering information

Table 13 Ordering information

Product	Description	No. of DS ports	No. of US ports	Application	TID	Package
CYUSB2354-40LTXI	USB 2.0 hub with four downstream ports	4 DS	1 US	Consumer/Industrial application (–40°C to 85°C)	–	40-QFN, 5 × 5 mm, 0.4 mm pitch
CYUSB2352-40LTXI	USB 2.0 hub with two downstream ports	2 DS	1 US	Consumer/Industrial application (–40°C to 85°C)	–	40-QFN, 5 × 5 mm, 0.4 mm pitch
CYUSB2364-36BFXI	USB 2.0 hub with four downstream ports	4 DS	1 US	Consumer/Industrial application (–40°C to 85°C)	15589	36-LGA, 6 × 6 mm, 0.5 mm pitch

Note

13. EZ-USB™ HX2G3 is also available in a Auto package for Automotive application. Contact **technical support** for the Infineon EZ-USB™ HX2G3 Auto USB 2.0 Hi-Speed Hub datasheet.

8.1 Ordering code definition

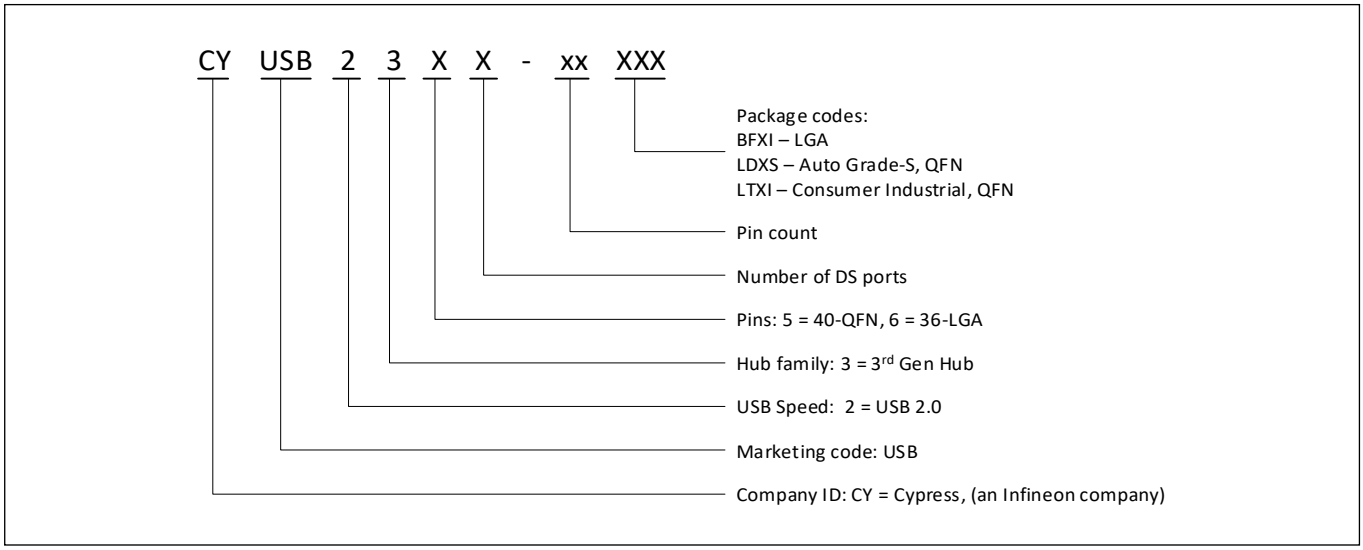


Figure 13 Ordering code definition

8.2 Silicon IDs

Table 14 Silicon IDs

Product	Package	Silicon ID	Family ID	Major/minor die rev ID
CYUSB2352-40LTXI CYUSB2352-40LTXIT CYUSB2352-40LTXIES CYUSB2352-40LTXIEST	40-QFN commercial	0xF060	0x121	0x1
CYUSB2354-40LTXI CYUSB2354-40LTXIT CYUSB2354-40LTXIES CYUSB2354-40LTXIEST	40-QFN commercial	0xF061	0x121	0x1
CYUSB2364-36BFXI CYUSB2364-36BFXIT CYUSB2364-36BFXIES CYUSB2364-36BFXIEST	36-LGA commercial	0xF063	0x121	0x1

9 Acronyms

Table 15 Acronyms used in this document

Acronym	Description
CFP	common footprint part
CLK	clock
DC	direct current
DFP	downstream facing port
DMC	dock management controller
DP	Display Port
DS	downstream
EC	embedded controller
EEPROM	electrically erasable programmable read-only memory
ESD	electrostatic discharge
FET	field effect transistor
FSDEV	Full-Speed device
FW	firmware
GPIO	general purpose input output
I/F	interface
I2C	Inter-Integrated Circuit
IoT	internet of things
LSB	least significant bit
MSB	most significant bit
MST	multi string transport
ms	millisecond
MUX	multiplexer
NC	no connection
NVIC	nested vector interrupt controller
PD	power delivery
PHY	physical layer
PID	product identifier
PLL	phase locked loop
ROM	read only memory
RX	receiver
SCB	serial communication block
SPI	Serial Peripheral Interface
SRAM	serial random access memory
SWD	serial wire debug
TX	transmitter
UART	universal asynchronous receive transmit
UFP	upstream facing port
US	upstream

Acronyms

Table 15 Acronyms used in this document *(continued)*

Acronym	Description
USB	Universal Serial Bus
UUID	universally unique identifier
VID	vendor identifier
WIC	wake up interrupt controller
XTAL	crystal

Revision history

Document revision	Date	Description of changes
*G	2026-08-26	Publish to web.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition: 2026-08-26

Published by
Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg Germany

Do you have a question about this document?
Email: erratum@infineon.com

Document reference
002-41112 Rev. *G

Important Notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

If this document is marked as 'Preliminary', 'Target', 'Draft' or 'Proposal', Infineon reserves the right to change all information given in this document at any time without notice. Subject to the development and release of a Product for series supply by Infineon, the technical specifications of the Product are set forth in the relevant datasheet provided by Infineon without such marking.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved.

Therefore, you may use the software only as provided in the software license agreement accompanying the software.

If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit https://www.infineon.com.